A Current Mode Cyclic A/D Converter with a 0.8μm CMOS Process

Masaki Kondo Hidetoshi Onodera Keikichi Tamaru

Department of Electronics, Kyoto University, Kyoto 606-01, JAPAN

Abstract - We have developed a current mode cyclic analog-to-digital converter using a 0.8μm CMOS process. Our circuit structure makes it possible to construct the converter without any precise analog components, hence, it is well compatible with submicron processes. The fabricated circuit has an area of 0.014mm^2 and performs 8-bit resolution at a sampling rate of 40kHz and average power dissipation of 370μW at 4V supply voltage.

I. Introduction

We present an analog-to-digital(A/D) converter which can be fabricated with submicron or deep-submicron processes at low cost. Many A/D converters require circuit areas proportional to their resolutions. The cyclic A/D conversion technique was developed to exclude the dependency on resolution. However, original cyclic converter relies on highly ratio-matched capacitors which is very costly in terms of area[1]. For further reduction of the circuit area, many cyclic converters were proposed[2]∼[4]. They, however, do not match with modern submicron processes because of the dependency on precise analog components. This is a serious problem especially for mixed signal circuits.

A current mode cyclic A/D conversion method[4] has been adopted. It is superior to other methods in terms of area and power. We have realized the converter using sample-and-hold(S/H) circuits based on regulated cascode(RGC)[5]. The RGC-based S/H circuit can achieve high output resistance and wide dynamic range simultaneously. Our architecture makes it possible to construct the A/D converter without any precise transistors nor ratio-matched capacitances. We have designed a test circuit using a 0.8μm CMOS process, which has an area of 0.014mm^2. It is examined to perform 8-bit resolution at a sampling rate of 40kHz and average power dissipation of 370μW at 4V supply voltage.

II. Architecture

The following recursive equation expresses the algorithm, in which I_{in}, I_{ref} and I_j represent the input, reference and j-th conversion currents respectively.

$$\begin{cases} I_1 &= I_{in} \\ I_{j+1} &= 2I_j - b_j I_{ref} \end{cases} \quad (1)$$

Coefficient b_j corresponds to the j-th resulting bit, being b_1 corresponding to the MSB. It is determined by

$$b_j = \begin{cases} 1 & \text{when} \quad 2I_j \geq I_{ref} \\ 0 & \text{when} \quad 2I_j < I_{ref}. \end{cases} \quad (2)$$

Fig.1 shows a block level diagram of our A/D converter. The circuit has three S/H circuits (S/H1∼S/H3), a current comparator and several analog switches. Both of S/H1 and S/H2 are composed of nMOSs, while S/H3 is composed of pMOSs. A D-flipflop is connected at the output terminal to store the conversion result.

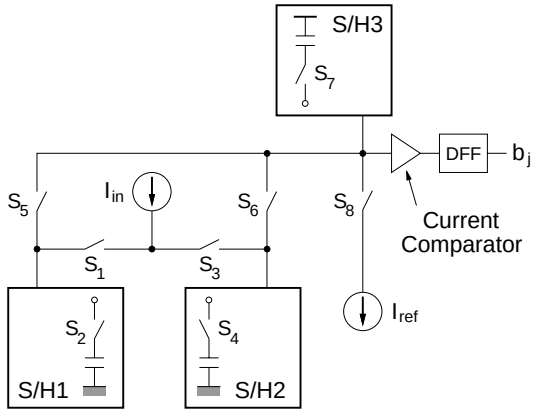

Fig. 1. The block level diagram.

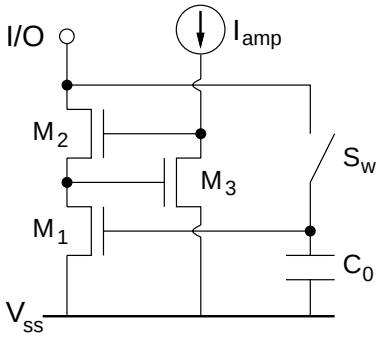

Fig. 2. The RGC-based S/H circuit(nMOS).

We briefly describe the conversion sequence below. First, the input current I_{in} is stored in S/H1 and S/H2 severally. At the next step, S/H3 stores $2I_{in}$ generated by both of S/H1 and S/H2. The comparator compares $2I_{in}$ with the reference current I_{ref}. The result b_1 determines the next state of S_W. It must be "ON" only when b_1 equals to "1". The next conversion current $2I_{in} - b_1 I_{ref}$ is stored in S/H1 and S/H2. We repeat above process until the LSB b_n is obtained.

We show the structure of RGC-based S/H circuit in Fig.2. Although Fig.2 shows an nMOS circuit for S/H1 and S/H2, a pMOS circuit for S/H3 also has an equal structure. The circuit consists of three MOS transistors $M_1 \sim M_3$, a capacitor C_0, an analog switch S_W and a constant current source I_{amp}. M_2, M_3 and I_{amp} compose a feedbacked amplifier which operates to fix the drain-source voltage of $M_1(V_D)$. A distinctive feature of the RGC-based S/H circuit is the high output resistance due to the fixed V_D. If M_2 operates in the saturation region and I_{amp} is enough small, the circuit can achieve high output resistance

ASP-DAC '97
0-89791-851-7$5.00

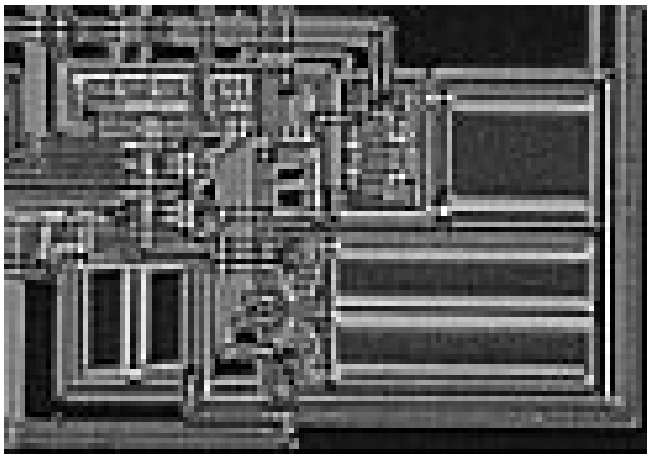

Fig. 3. The photograph of the test circuit.

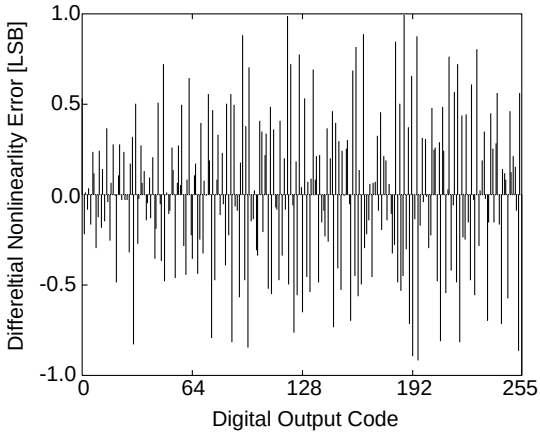

Fig. 4. Measured differential nonlinearity errors.

with short-channel transistors for all of $M_1 \sim M_3$.

III. Designed Circuit

We have designed a test circuit using a 0.8μm CMOS process with double metal and double poly-silicon layers. Before designing device sizes, we carefully characterized MOS transistors with several channel lengths. Transistor parameters were extracted from measured I-V data using our own extraction tool[6]. The g_{ds} and g_m characteristics were also considered. We used HSPICE for the circuit simulations and Cadence DFII for the layout design.

The test circuit was designed to achieve 8-bit resolution with 3.3V$\sim$5V power supply and 50μA reference current. In the S/H circuits, all of nMOSs have a size of W/L=4μm/0.8μm. Similarly, pMOSs have a size of 16μm/1.6μm. We chose 2pF for all of C_0s which were implemented by poly1 and poly2 layers. We applied a dummy switch technique[7] to reduce the switch induced charge injections. Analog switches were implemented by CMOS transmission gates with minimum sized transistors.

We show the microscopic photograph of the A/D converter in Fig.3. The three components in the right side correspond to capacitors of S/H circuits. The right half part includes all of the circuit core which consists of three S/H circuits. The core part occupies an area of 100μm$\times$140μm or 0.014mm^2. We also integrated current sources such as I_{ref} for the ease of performance measurement. They appear in the left half part of the photograph. The whole circuit including the current sources has an area of 0.024mm^2.

IV. Experiments

We examined the digital output code as a function of input current with a sampling rate of 40kHz. We defined the transition level from code $(i-1)$ to i as the input current at which code i appears with a probability of 50%. The measured static differential nonlinearity error(DNLE) for each digital code is shown in Fig.4. Although the DNLEs vary from -0.9LSB to 1.0LSB, there are no missing codes and non-monotonicities.

We also measured the power dissipation. The power dissipations at minimum and maximum input currents are 290μW and 450μW, respectively. If the input levels are uniformly distributed, the average power dissipation is 370μW.

V. Conclusion

We presented a A/D converter that matches submicron fabrication processes. The converter realizes the current mode cyclic A/D conversion algorithm. We achieved small circuit area using S/H circuits with high output resistances and wide output swing. The test circuit has an area of 0.014mm^2 using a 0.8μm CMOS process. The measured performances are 8-bit resolution, 40kHz sampling rate and 370μW average power dissipation. These results show that the A/D converter can be applied to parallel intelligent image sensors, for example.

Acknowledgements

We would like to thank *NTT Electronics Technology Corporations* for the fabrication of out test circuit.

References

[1] R.H.McCharles and D.A.Hodges, ''Charge Circuits for Analog LSI'', IEEE Tran. on Circuits and Systems, vol.25, no.7, pp.490-497, 1978.

[2] H.Onodera, T.Tateishi and K.Tamaru, ''A Cyclic A/D Converter that does not require ratio-matched components,'' IEEE J. Solid State Circuits, vol.SC-23, pp.152-158, 1988.

[3] P.W.Li, M.J.Chin, P.R.Gray and R.Castello, ''A Ratio-Independent Algorithmic Analog-To-Digital Conversion Technique,'' IEEE J. Solid State Circuits, vol.SC-19, pp.828-836, 1984.

[4] D.G.Nairn and C.A.T.Salama, ''A Ratio-Independent Algorithmic Analog-To-Digital Converter Combining Current Mode and Dynamic Techniques,'' IEEE Tran. on Circuits and Systems, vol.37, no.3, pp.319-325, 1990.

[5] E.Sackinger and W.Guggenbuhl, ''A High-Swing, High-Impedance MOS Cascode Circuit,'' IEEE J. Solid State Circuits, vol.SC-25, pp.289-298, 1990.

[6] , Masaki Kondo, Hidetoshi Onodera and Keikichi Tamaru, ''Model-Adaptable Parameter Extraction System for MOSFET Models,'' IEICE Trans. on Fundamentals of Electronics,vol.E78-A, no.5, pp.569-572, 1995.

[7] R.E.Suarez, P.R.Gray and D.A.Hodges, ''All MOS Charge Redistribution Analog-to-Digital Conversion Techniques Part II,'' IEEE J. Solid State Circuits, vol.SC-10, pp.379-385, 1975.