A CMOS Delayed Locked Loop (DLL) for Reducing Clock Skew to Under 500ps

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Abstract

This paper presents a variable delay line DLL circuit implemented in a 0.8 μm CMOS technology. A phase detector and two charge pump circuits calibrate the delay per stage of the delay line using push-pull type clock synchronization scheme. The delay line can be programmed 6 to 18 stages. The DLL circuit is capable of reducing clock skew from 1-3ns to below 500ps for clock frequencies from 50Mhz to 150Mhz.

1 Introduction

As silicon fabrication technology develops, the chip size gets bigger and bigger, and number of logic gates and chip operating frequency increase, clock skew becomes more and more important in ensuring proper functioning of VLSI chips. With a synchronous communication protocol, it is impossible to further increase the communication clock speed without reducing the clock skew on chip.

The clock skew is caused by different RC delay of clock interconnects along different clock signal paths and different delays of clock buffers due to process variations, temperature differences on the same chip, and power supply differences due to power rail IR drop. To reduce clock skew, the clock distribution network should be carefully designed. In addition, circuit techniques such as Phase Locked Loop (PLL) and Delay Locked Loop (DLL) may become necessary to reduce the total clock skew by employing them in several critical places of the clock distribution structure. DLL has advantage over PLL for low-voltage applications where it is difficult to obtain acceptable noise-induced jitter performance as supply voltage drops. In addition, acquisition time is often larger in PLL than in DLL due to the time PLL takes to drive the VCO to the correct frequency[1]

2 Design of a Sub-500ps DLL

Fig.1 shows the block level structure of the DLL circuit. The phase detector output is proportional to the input signals' phase difference, i.e. clock skew. The increase/decrease of the phase detector output then controls the delay line A and B so that clock at point A or B is delayed by an appropriate amount of time with respect to the other clock signal. In order to reduce the settling time of the loop, two charge pumps and delay lines have been used to make the clock synchronization a push-pull type.

A sequential logic phase/frequency detector (PFD), shown in Fig.2, is used with the reset function. Since it has a memory compare frequency as well as phase,

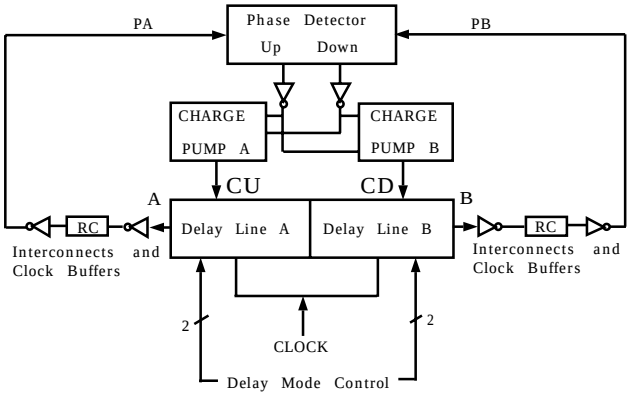

Fig.1 Block level structure of the DLL circuit.

it is fre from false locking to the second or third harmonic[2]. The phase detector output signals are connected to the charge pump circuit, shown in Fig.3, to convert the voltage pulse into a current pulse. The operation of this charge pump is similar to that of an analog up-down counter. The detected phase difference represented by the current pulse is integrated using the capacitor. The total voltage accumulated on the capacitor is used to 'program' the variable delay line. The daly line uses voltage-controlled delay line (VCDL). Because the output phase is proportional to the input control voltage, the transfer function is simple H(s) = K[3].

Table 1. Silicon Area of DLL block

Element	*Area(sq.μm)*
Phase detector	8,800
Charge pump	30,800
Delay line	4,400
Total	44,000

Before the DLL circuit was mapped on to a 0.8 μm CMOS process, a detailed analysis on the stability characteristics of the DLL loop was carried out to determine the component values in the circuit. The silicon area of each functional block in the circuit is summarized in Table 1. The microphotograph of the chip is shown in Fig.4.

The chip was tested by physically introducing clock skew from off-chip circuit. Figs.5 and 6 show the measured waveforms of the unsynchronized and synchronized clock signals, respectively. The unsynchronized clock signals were skewed 7.8ns by external circuits,

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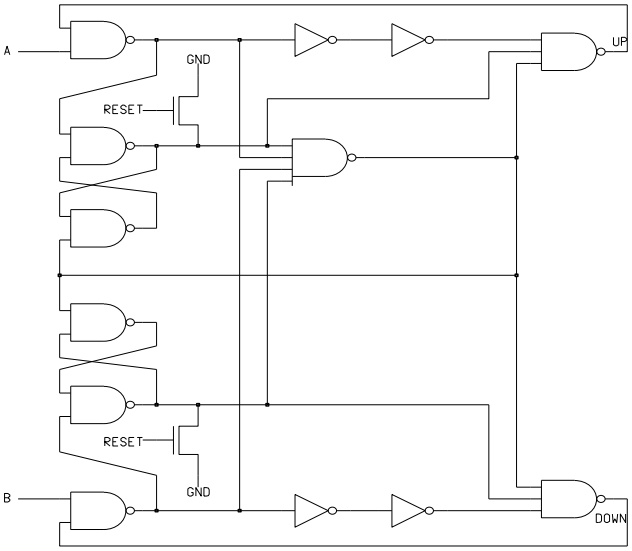

Fig.2 Sequential logic PFD

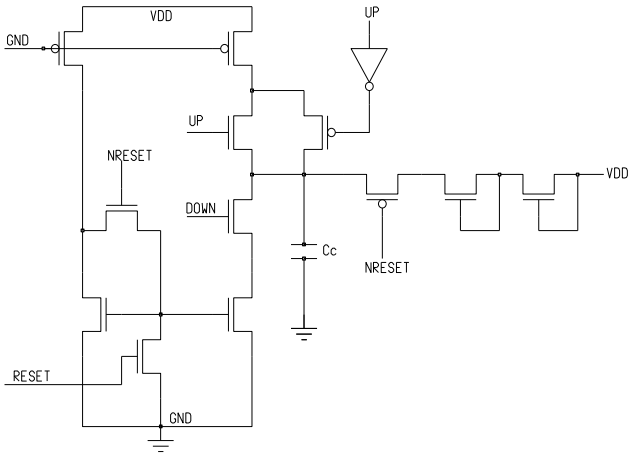

Fig.3 Charge pump circuit

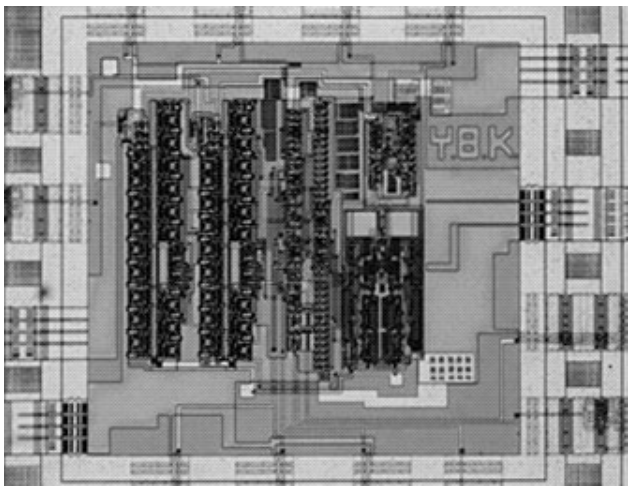

Fig.4 Microphotograph of the DLL chip.

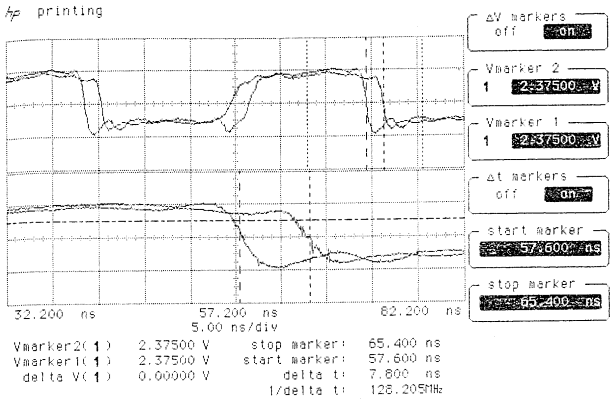

Fig.5 Unsynchronized input waveforms with 7.8ns skew.

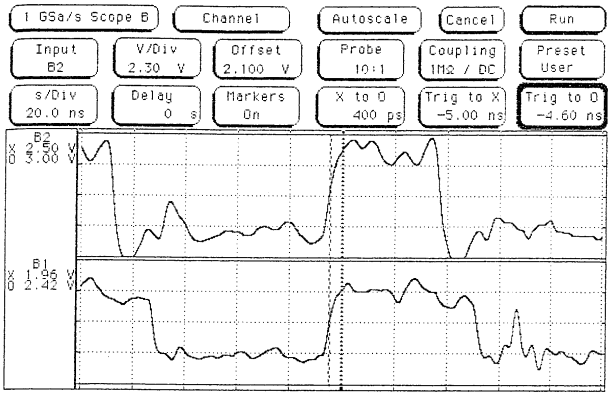

Fig.6 Corrected (deskewed) waveforms with 400ps skew.

and the clock skew after the DLL circuit has been reduced to 400ps as shown in Fig.6. The clock frequencies ranging from 50Mhz to 150Mhz were used during testing.

3 Conclusion

DLL circuits such as the one presented in this paper can be an effective circuit technique to reduce clock skew on a VLSI chip. For large silicon dies requiring multiple on-chip deskewing circuits, DLL is a better candidate. The programmable DLL presented in this paper is well suited for this type of applications.

Acknowledgment

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References

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