A Real-Time High Performance Edge Detector for Computer Vision Applications

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Abstract

We present a high performance edge detection architecture for real-time image processing applications. The architecture is finely pipelined. The proposed ASIC is capable of producing one edge–pixel every clock cycle. At a clock rate of 10 MHz, the architecture can process 30 frames per second, where the size of each frame is 640×480 8–bit pixels. The ASIC was laid out and fabricated using Samsung's 0.8μm double–metal CMOS process.

1 Introduction

One of the key stages of image processing and object recognition is edge detection. Many edge detection algorithms have been proposed [1,2,3]. Even though all these edge detection algorithms have succeeded in various degrees in detecting strong and weak edges, one of the common drawbacks of these algorithms is that the computational costs typically increases for algorithms with bettwe performance. Most of the existing algorithms have only been implemented in software. Only a few have been implemented in silicon [4,5] with limited ability to detect weak edges. We present a new edge detection algorithm based on the absolute difference mask (ADM). It was developed for efficient mapping in to hardware where the precision, cost, and speed are optimally balanced.

2 The Absolute Difference Mask

The absolute difference mask algorithm performs three stages of processing in order to detect edges. The produced edges are single–pixel wide and localized. The three stages are: (1)applying the semi–Gaussian filter to the image to reduce noise effect, (2)finding the edge strength and direction at each pixel, and (3)producing the final edge map that is used in the following computer vision stage.

The steps find both the edge strength and the edge direction are:

1. Preparing inputs to find the absolute differences for $p_{(i,j)}$:
   $V_u = V_u(1) + V_u(2)$, $V_l = V_l(1) + V_l(2)$
   $H_r = H_r(1) + H_r(2)$, $H_l = H_l(1) + H_l(2)$
   $Pd_u = Pd_u(1) + Pd_u(2)$, $Pd_l = Pd_l(1) + Pd_l(2)$
   $Nd_u = Nd_u(1) + Nd_u(2)$, $Nd_l = Nd_l(1) + Nd_l(2)$

2. Calculating all absolute differences for $p_{(i,j)}$:
   $V = |V_u - V_l|$, $H = |H_r - H_l|$
   $Pd = |Pd_u - Pd_l|$, $Nd = |Nd_u - Nd_l|$

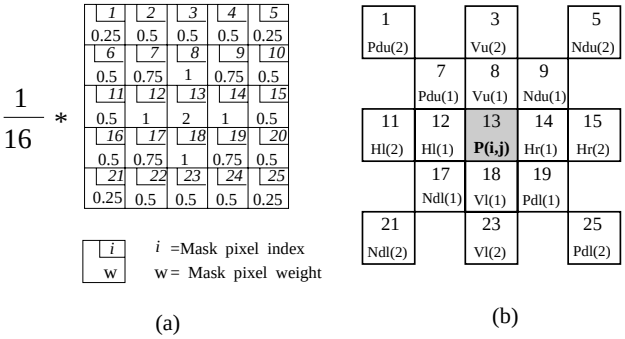

Fig.1: (a)The smoothing mask (b)The Absolute Difference Mask

3. Determining edge strength and direction:
   $S_e = max\{V, H, Pd, Nd\}/2$
   $dir_e = dir(min\{V, H, Pd, Nd\})$

Fig.1 shows the smoothing mask and the ADM mask. Once these three steps are completed, the edge at $p_{(i,j)}$ will be represented by its strength and its direction. Extensive comparisons were made between our algorithm and other well known algorithms. The performance of the ADM algorithm is comparable to that of Canny's algorithm, but with significantly less computational complexity and with significant amount of regularity, which is very important for mapping on to silicon. Due to the space limitation, readers can consult [6] for more details of the comparison.

3 VLSI Architecture and Silicon Implementation

Fig.2 shows the block diagram of the edge detector using the ADM algorithm. The edge detector is divided into three units: the smoothing unit, the edge strength unit, and the detection and localization unit. The detailed structure of these three units can be found in [6].

The latency of the architecture is $5n + 18$ clock cycles. 3460 gates and 38,600 latches are used. The VLSI architecture have been tested on many real–world images. The edges produced by the ADM VLSI architecture for both noise–free and noisy images are shown in Figure 3, where (a) and (c) show the original noise–free and noisy images, respectively, and (b) and (d) show edges detected by the ADM VLSI architecture. The threshold applied to the output of the noise–free edge map is 20 while the threshold of the noisy edge map is 30.

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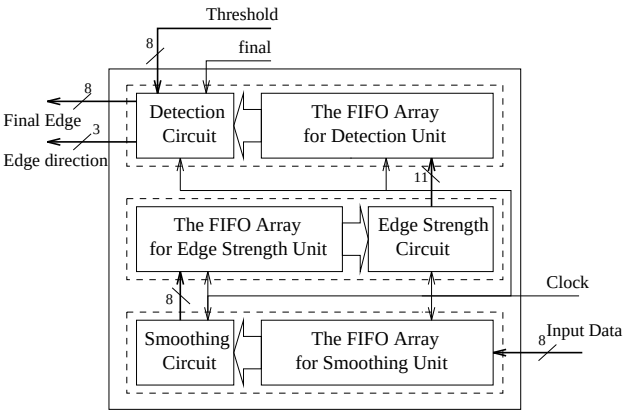

Fig.2: The block diagram of the edge detector.

The edge detection chip using the ADM algorithm was laid out using Samsung's 0.8 μm double metal N-well CMOS process. The die size is 12.4 × 12.2 mm^2. It has 64 I/O pads and 650,000 transistors. Fig.4 shows the microphotograph of the chip. Functional test was carried out on the chip using some simple images and the test results match the simulation results.

4 Conclusion

We presented a new edge detection algorithm based on ADM. The algorithm was mapped and verified on silicon. The VLSI chip is capable of processing 30 VGA-size frames/second using a clock frequency as low as 10Mhz. This chip is aimed at applications of real-time computer vision and pattern recognition tasks.

Acknowledgment

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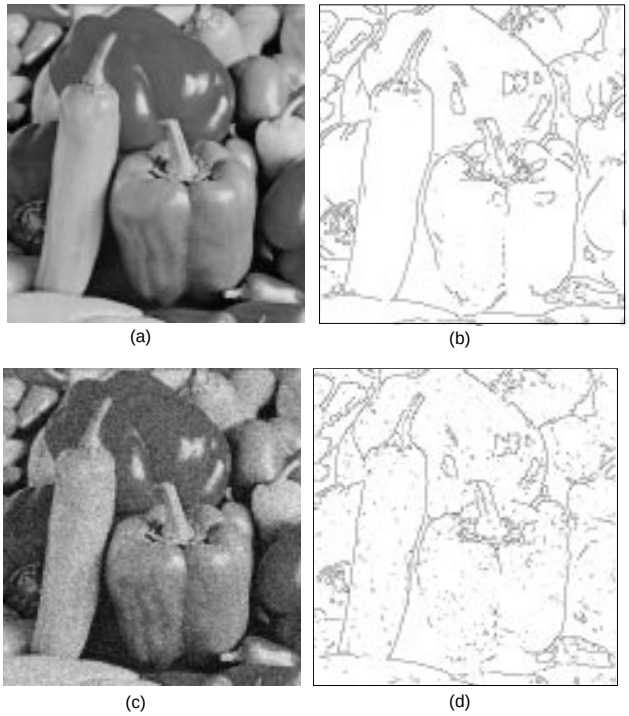

Fig.3: Detecting edges in 'Peppers': (a) and (c) original images, (b) and (d) edges detected by the ADM ASIC.

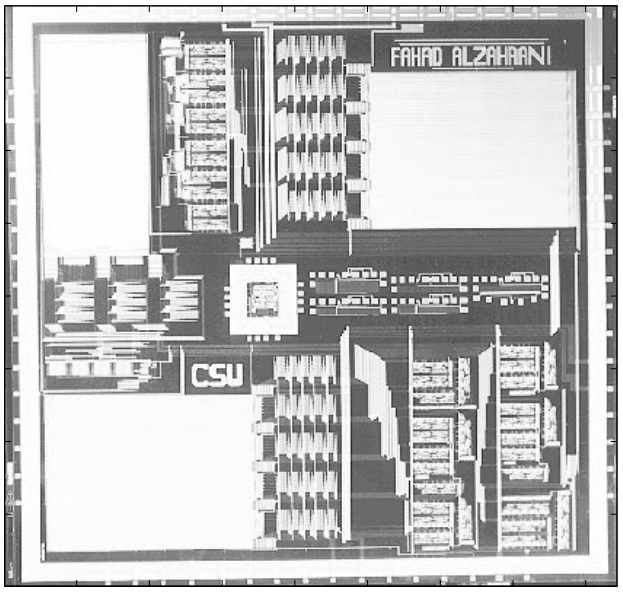

Fig.4: The microphotograph of the edge detection chip.