# High Speed Bit-Serial Parallel Processing on Array Architecture

Kazuhito Ito Takenobu Shimizugashira Hiroaki Kunieda

Dept. of Elec. and Elect. Syst.
Saitama University
Urawa, Saitama 338, Japan
Tel: +81-48-858-3731
Fax: +81-48-855-0940
kazuhito@elc.ees.saitama-u.ac.jp

Dept. of Elec. and Elect. Eng.
Tokyo Institute of Technology
Meguro-ku, Tokyo 152, Japan
Tel: +81-3-5734-2574
Fax: +81-3-5734-2911
{kashira,kunieda}@ss.titech.ac.jp

**Abstract— Word-parallel bit-serial processing is a solution to high speed processing suitable for VLSI. In this paper a new bit-serial parallel processing architecture is proposed. A VLSI chip for a digital filter is designed based on the proposed architecture and it is implemented on a gate array chip. Through the implementation, it is verified that bit-serial parallel processing on an array architecture achieves high speed processing and easy design.**

## I. Introduction

In the era of deep submicron technology, one solution to achieve higher processing speed is parallel processing, especially word-parallel bit-serial processing [1]. In general, bit-serial processing requires more clock cycles to execute an operation than bit-parallel processing. For example, an addition of two 16 bit words requires 16 clock cycles on a bit-serial adder while an addition can be done in only one clock cycle on a bit-parallel adder. However, if 16 bit-serial adders operate in parallel, the same processing rate, i.e., one addition per cycle, can be obtained. Moreover, a high speed clock can be easily achieved in bit-serial processing, since the critical path is shorter than bit-parallel processing. Consequently, word-parallel bit-serial processing achieves higher processing speed.

A new word-parallel bit-serial processing architecture is proposed here: the overall system is like a systolic array where each processing element (PE) executes word-level operations (not bit-level operations as in bit-level systolic arrays) and communicates data words with each other in bit-serial fashion over data communication links. In this architecture, data communication cost is relatively smaller than operations. Sending data to an adjacent PE is not overhead but the method to achieve higher parallelism in word-parallel bit-serial processing.

As a preliminary experiment toward the massively parallel bit-serial system, a VLSI chip which consists of six bit-serial 16-bit fixed point PEs is designed. All the six PEs are of an identical architecture consisting of a bit-serial multiplier and adder, a shifter with variable shift width, bit-serial registers, and data communication ports.

## II. Implemented Processing Algorithm

The implemented digital signal processing algorithm is a lowpass filter based on a complex allpass filter theory [2]. The cut-off frequency is $0.4\pi$ and the stop band gain is $-40$dB. Then, the processing algorithm is modularized so that every addition inputs one shifted data and one multiplied data by using a modularization technique proposed in [3]. This modification is intended to simplify the data path of PEs. Bit shift operations are introduced in order to make multiplication coefficients between $-1$ and 1 and maintain the dynamic range of the filter acceptable. Fig. 1 shows the modularized processing algorithm.

## III. Chip Design

### A. Target Parallel Architecture and Design Methodology

As the system level architecture suitable to VLSI implementation, the neo-systolic array architecture [4] was adopted. The design is divided into hierarchies as shown in Fig. 2. At the very beginning of the design, the specification of each design layer including the input/output interface of functional units in PE and communication protocol between PEs were fixed. Then one or two persons are assigned to each layer of design: i.e., scheduling, processor architecture design, multiplier, data I/O port, register, and controller designs. These design procedures have been done in highly parallel since interface between designs was fixed and therefore there was little interaction between designs.

One of the important feature of the neo-systolic array is scalability in size. When the chip design started, we estimated that 9 PEs could be implemented. However, the number of PEs was finalized as 6 to form a $2 \times 3$ array structure as illustrated in Fig. 2(a). Although the number of PEs has been changed, only scheduling, processor architecture (the number of registers), and controller were modified and there was no need to modify any other designs.

All the circuits are designed in logic level and entered schematically. Clock buffers are inserted manually so that the number of buffers from the clock input pad to each D flipflop is identical. Because of highly parallel design and scalability of the target architecture, all the design process was completed in three months.

### B. Scheduling

The modularized processing algorithm shown in Fig. 1 contains 18 multiplications. Each of six PEs executes three multiplications in an iteration period. Therefore, the lower bound of the iteration period is $32 \times 3 = 96$ clock cycles.

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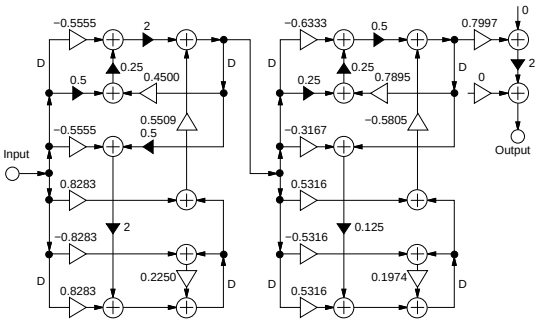


Fig. 1. Modularized processing algorithm.

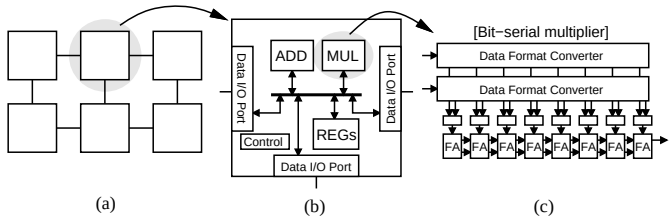


Fig. 2. Chip design hierarchy. (a) Multiprocessor layer. (b) Processor layer. (c) Functional unit layer.

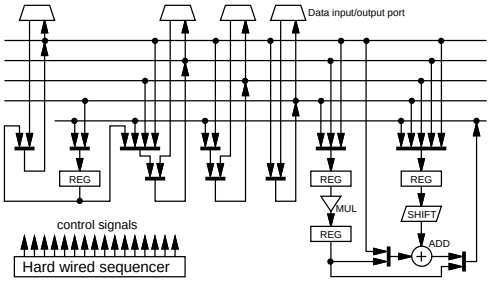


Fig. 3. Architecture of processing elements.

TABLE I
THE NUMBER OF GATES

| Component | # of gates |
|---|---|
| Multiplier | 1100 |
| Register | 150 |
| Data I/O port | 300 |
| Adder, Shifter, Mux | 200 per PE |
| Control | 550 per PE |
| Test | 100 per chip |
| Total | 19093 per chip |

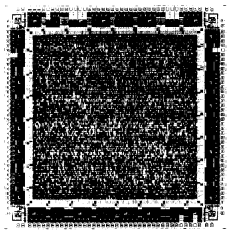

Fig. 4. A photo of the chip. The size is 7.5mm×7.5mm.

First, operations are scheduled to achieve the iteration lower bound by the scheduling technique mentioned in [3]. Then, the schedule was refined to minimize the required number of registers. In the final schedule, an identical datum is sent more than once from a sender PE to a receiver PE if the number of data to be stored can be reduced on the receiver PE. This refinement procedure is done without increasing the iteration period.

### *C. Processing Element*

Fig. 3 illustrates the data path of a PE used in this VLSI chip design. In Fig. 3 a thick line implies a multiplexor which is controlled by a hard wired sequencer in each PE. Since bit-serial processing is used, a bus implies a single wire. Therefore, we can use as many data buses as required to maximize resource usage and to resolve bus conflict without much area penalty.

## IV. CHIP EVALUATION

The final logic circuitry is mapped onto a 0.5$\mu$m two metal layered sea-of-gate style CMOS gate array chip where 19093 basic cells are used from 50K available cells. Table I summarizes the gate counts of the designed chip. Fig. 4 shows the photo of the fabricated chip. In this chip design, the layout design was done at a foundry and hence we did not participate in the cell placement and routing. The netlist is first flattened before layout design. Therefore, no particular pattern can be seen on the photo.

The fabricated chip is proven to run at 50MHz clock. We cannot check the chip with faster clock because of the upper limit of the IC tester's performance. Since the iteration period of the designed digital filter is 96 clock cycles, the filter operates at the sampling rate of at least 520kHz.

## V. CONCLUSIONS

We have designed a chip of word-parallel bit-serial processor array. Although the circuit designers did not participate in the layout design, the chip works at 50 MHz. This proves the effectiveness of the bit-serial parallel processing. Namely, the critical path of the bit-serial data path is inherently short and that since the PE array used in this design has many local communications and few global communications, the layout CAD tool generated a layout where every wire delay is reasonably short. In addition, we verified the high scalability of neo-systolic array architecture.

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## REFERENCES

[1] M. Hatamian and G. L. Cash, "Parallel Bit-Level Pipelined VLSI Design for High-Speed Signal Processing," *Proceedings of the IEEE*, vol. 75, pp. 1192–1202, Sept. 1987.

[2] T. Saramaki, T. H. Yu, and S. K. Mitra, "Very Low Sensitivity Realization of IIR Digital Filters using a Cascade of Complex Allpass Structures," *IEEE Trans. Circuit Syst.*, vol. CAS-34, pp. 876–886, Aug. 1987.

[3] K. Ito and H. Kunieda, "VLSI System Compiler for Digital Signal Processing: Modularization and Synchronization," *IEEE Trans. Circuit Syst.*, vol. 38, pp. 423–433, Apr. 1991.

[4] K. Ito, K. Hagiwara, and H. Kunieda, "Neo-Systolic Array: A Hardware Model for VLSI System Compiler VEGA," in *The Proceeding of 1992 IEEE Asia-Pacific Conference on Circuits and Systems*, Sydney, pp. 313–318, Dec. 1992.