Super Low Power 8-bit CPU with Pass-Transistor Logic

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Abstract— A very low power 8-bit CPU core has been designed based on an original pass-transistor logic family, SPL and SPHL. The instruction set and external timings are compatible with the Zilog Z80. Average supply current is 740μA at 3V with a 10MHz-clock, equivalent to 26% of that of the commercial CMOS Z80 CPU cores using the same design rules (0.8μm, w-metal).

I. Introduction

Recently developed portable electronic products such as portable phones, palm top computers and PDAs (portable digital assistants) are strongly in need of very low power LSIs. The authors have developed a new pass-transistor logic family named SPL (Single-rail Pass-transistor Logic) and SPHL (Single-rail Pass-transistors and Holders Logic) for this purpose [2]. SPL and SPHL are successful in very low power, which distinguishes them from other pass-transistor logic such as CPL and SRPL, that are concerned with high speed, low power operation. The low power Z80 is the first product of the system-level application of SPL and SPHL. Its design features and measurement results are reported.

II. Design Features

A. Specification Overview

(1) Full custom 8-bit microprocessor
(2) Microampere operation at 3V, 10MHz (max. clock)
(3) Z80 compatible instruction set
(4) Z80 compatible external operation timings
(5) Designed in pass-transistor logic SPL/SPHL
(6) 0.8 micron w-metal process

B. Basic Design Features

(1) The external specifications are fully compatible with original Z80. However, the internal structure and timing are newly designed for extremely low power operation.
(2) Most of the combinational circuits are designed based on SPL [2].
(3) Functional modules, involving SPL circuits, are connected in an SPHL-based connection structure [2]. These two features are the primary contributors to the power reduction. Additional low power features are shown below.
(4) ALU architecture is changed from 4-bit (original CMOS) to 8-bit, which results in higher speed operation with lower signal transition probability.
(5) Almost all clock lines are gated by control signals; in other words, clocked control signals are distributed to reduce the signal transition probability.

C. SPL and Combinational Circuits Design

SPL is principally characterized by the following two features. The first is the use of a long series of NMOS pass-transistors without intermediate buffers (Fig.1), or with a few intermediate buffers on critical paths. Comparatively, other pass-transistor logics, such as CPL, SRPL, and LEAP [3], have buffers located between every second or third series of NMOS pass-transistors. This reduction in the number of buffers reduces both the number of transistors and the short-circuit current at the buffers.

The second feature is the "single-rail" structure through which the pass-transistor logic does not generate a pair of complementary outputs, but rather a single output unlike CPL and SRPL.

The procedure for designing combinational circuits based on SPL is as follows. A description of the logic circuit is translated into a shared reduced ordered-BDD. In order to generate a small BDD, a partial diagram replacement technique [1] is used. The BDD is then mapped to a SPL circuit simply as a single BDD node to a pair of NMOS (Fig.1). When the signal delay does not fall within given constraints, buffers are incrementally inserted into the corresponding critical path until the delay meets specifications.

A dedicated logic synthesizer [1], using the procedure described above, produced the control logic, the logical operation unit and the shifter in the Z80. The arithmetic unit and the incrementer, that have repeating structure, are designed by hand. The number of the longest series of NMOS pass-transistors was 13 in the Z80 ALU.

D. SPHL and Data Path Design

SPHL is an extension of SPL used for design of the data path [2]. A single SPHL module includes a series of input data holders (registers), SPL combinational circuits (without output buffers) and tri-state output buffers (Fig.4). The tri-state output buffers hold two different roles, the output buffer of the SPL and the write control gate for input data holders in the next module.

SPHL modules are connected in cascade to construct a whole system. Each SPHL module includes a functional unit such as an adder.

In SPHL-based data path design, SPHL modules are connected individually without the use of common buses.

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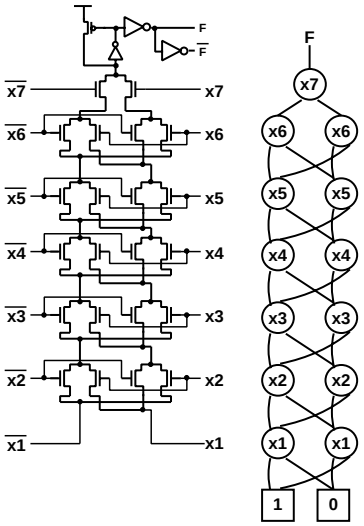

Fig. 1. Example of SPL circuit and corresponding BDD

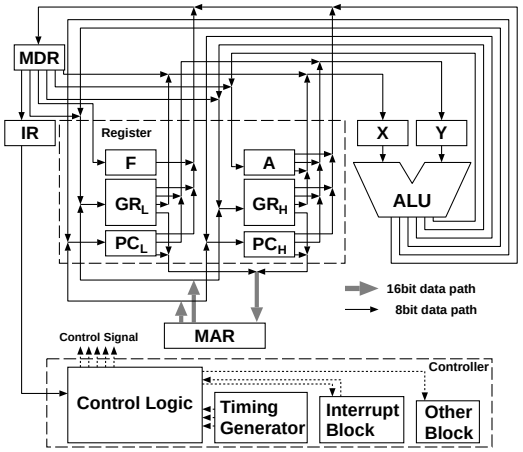

Fig. 2. Block diagram of low power Z80 based on SPHL

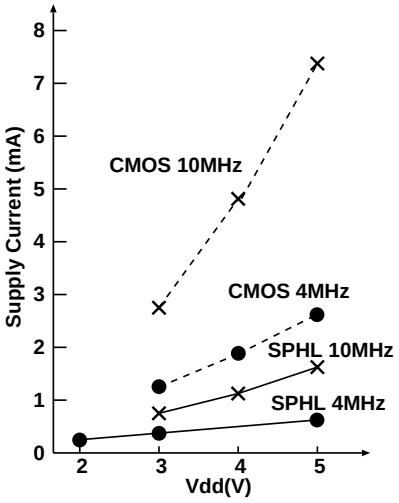

Fig. 3. Measurement results

This structure reduces both the probability of signal transition and the amount of common capacitance at each inter-module connection line.

The output of the tri-state output buffers is only enabled at data write time to the next module, i.e. after the slow signal transition of the buffer input (SPL output), which reduces the short circuit current of the output buffer.

A block diagram of the low power Z80 (SPHL-based design) is shown in Fig.2. A transistor-level layout synthesizer (LAS from Cadence Design Systems Inc.) was used for macro-block layout synthesis of each SPHL module.

III. Measurements and Conclusion

The experimental LSI chip consisted of 13,684 transistors[1], approximately 5 percent less than the number found in commercial CMOS Z80. The die size (effective area) is 3.1mm×2.8mm, not yet optimized.

Power dissipation was measured (Fig.3). Average power supply current was found to be 740μA at 3V with a 10MHz-clock, or 26% of that of commercial CMOS Z80 CPU cores using the same design rules(0.8μm, w-metal). The tested lowest operation voltage was 2V, where the average current was 200μA with a 4MHz-clock. The maximum clock frequency was comparable with that of the CMOS Z80, approximately 10MHz at 3V.

A very low power 8-bit CPU core was successfully developed based on a dedicated pass-transistor logic family, SPL and SPHL. A super low power 32-bit CPU will soon be attempted.

[1]Logical complexity increased at ALU and control logics in the Z80 because of structure changes from the CMOS Z80. This is a reason why the transistor counts did not decline much.

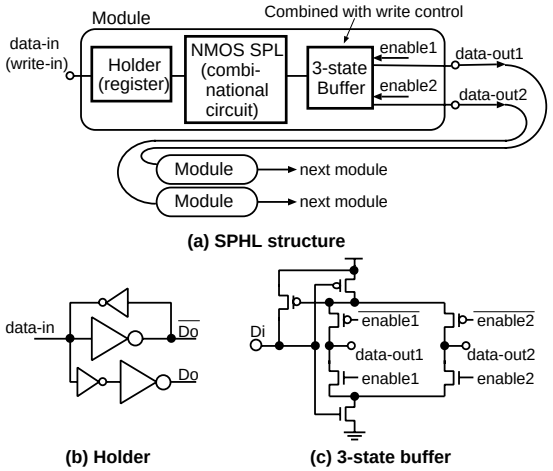

Fig. 4. SPHL structure overview

Acknowledgment

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