

EMC-Adequate Design of Printed Circuit Boards as a Part of the System Development

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Abstract— The EMC-adequate design of microelectronic systems includes all actions intended to eliminate electromagnetic interference in electronic systems. Challenges faced in the microelectronic area include growing system complexity, higher operating speed, denser design at all levels of integration (chip, printed circuit board, MCM and system).

Growing complexity, denser design and higher speed all lead to a substantial increase in EMC problems and design time. EMC is not commonly accepted in microelectronic design. Microelectronic designers have the opinion that EMC has to do with electrical and electronic systems and mandatory product regulations instead of requirements to the integrated circuit they are designing.

In this contribution a concept for an EMC-adequate design of electronic systems will be introduced. This concept is based on a generalized development process to integrate EMC-constraints into system design. A prototype of an environment to analyse signal integrity effects on PCB based on a workflow oriented integration approach will be introduced. Based on this approach the generation of user specific design and analysis environments including various set of EMC-tools is possible.

I. INTRODUCTION

The development and provision of for example communication techniques especially their connection to computer technologies for the presentation and processing of multi media information requires the use of electronic components with high processing speed. Moreover, there is a trend motivated by economic pressure that leads to the integration of components and subsystems to highly compact systems.

Also, this trend gains importance within other application areas (e.g. car industries, automation techniques).

The high processing speeds and integration densities lead to EMC-effects relevant on system as well as component level. These effects may be divided into 'internal' electromagnetic interactions (e.g. signal integrity effects) and 'external' electromagnetic influences (radiation, irradiation). Therefore, in addition to the designers of microelectronic components also their users are confronted with considerable change. Among others, the system complexity, integration density on all partitioning levels (component, subsystem, system) and the really necessary limitation of the number of design cycles ('first time right', 'time to market') are concerned.

Effects like crosstalk, reflections on transmission lines, delta-I-noise (ground bounce, simultaneous switching, current spike), electrostatic discharge (ESD) and electromagnetic radiation or irradiation have to be considered when applying microelectronic components. These EMC-effects can cause malfunctions on component-, subsystem- and system level. The mentioned interference effects are not separately occurring phenomena, but have to be seen as characteristics of a specific design. This means, EMC-effects are design relevant subjects. Therefore, with respect to the required system function it has to be viewed under EMC-constraints as well.

Especially because of the higher integration densities at system- and component level not all EMC-effects can be observed during the development process by measurement. Furthermore, measurement techniques for EMC-analysis are greatly limited by engineering and financial bounds.

Besides the consideration of international and national standards (legal requirements) the development of electronic products under EMC-constraints becomes more and more important with regard to their efficiency as well as a right time to market.

Because of this, many industrial users of microelectronic components have employed and trained their own EMC-experts. These experts support the circuit designer in order to ensure the meeting of the fundamental design standards. These requirements are usually based on experience and have been gained and documented within the company quite often over a period of many years. Hence, the circuit designers have to work closely together with the EMC-experts or acquire the extensive know-how by themselves.

Another approach is the introduction of development software into which EMC-relevant features are included and which makes expert knowledge available to the circuit designers in a way easy to understand and handle.

Therefore, the development of methods and tools for a complete system design considering the boundary conditions imposed by EMC constraints and their integration into user specific design processes will be a main challenge for industries in the following decade.

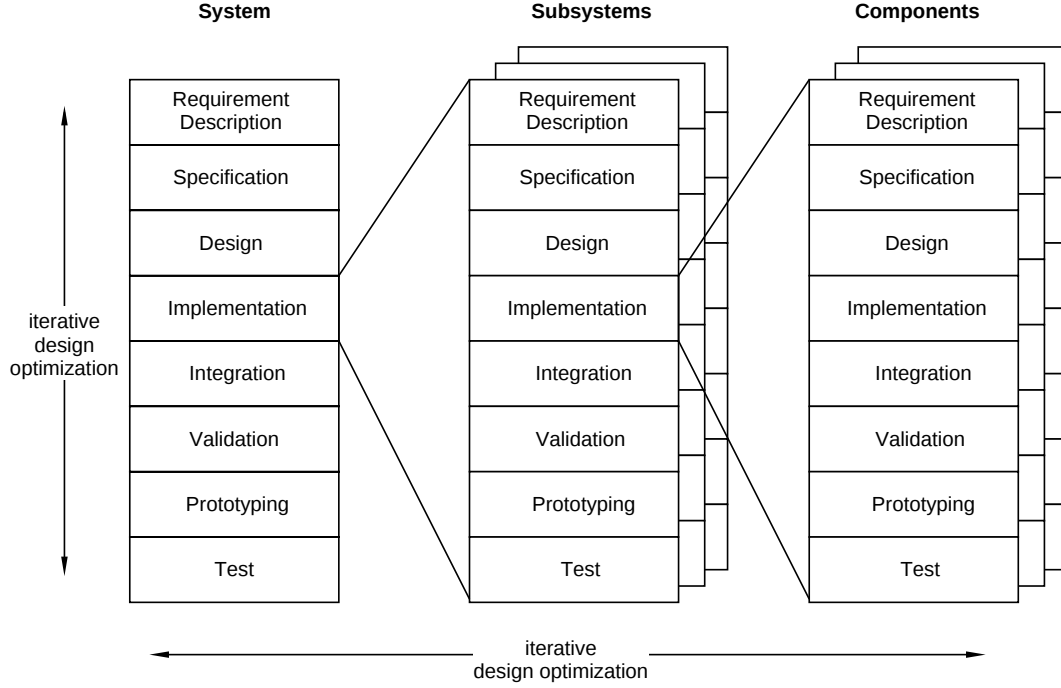


Fig. 1.: Generalized development process

II. EMC–ADEQUATE SYSTEM DESIGN

A. Motivation

The motivation to consider EMC constraints while designing an electronic system is first of all to ensure the functioning of the system under development within given ambient conditions. Compliance with relevant EMC standards is also an important issue. In addition, the quest for the minimization of costs and development time poses another quite important restriction. The compound of constraints one is confronted with can only be accounted for satisfactorily by a systematic consideration of EMC objectives at all design stages of a development process, which calls for the introduction of a model for its sufficient representation.

B. Integration of EMC-Constraints into System Design Process

A model based on the characteristic design stages has been developed in order to obtain a general approach in describing the integration of EMC constraints into the development process, as shown in Fig. 1.

Usually, the various design stages starting from system requirement description via system implementation up to the test procedures are passed several times. Only if the results in a particular design stage complies with previously defined specifications, the following stage will be entered. Otherwise the actual design stage, possibly even previous ones, will have to be passed again with modified parameters. In this way several versions of a product may exist in parallel within a certain stage.

The system to be developed is partitioned recursively into subsystems and components in order to obtain a set of manageable objects. After having defined a set of suitable interfaces in order to decouple the subsystems and components, they may be treated independently from each other. Therefore, a system hierarchy occurs almost naturally, which may be described via a tree structure.

The first design stage of the process model is called 'requirement description'. Its outcome will be a list also containing relevant EMC constraints. In the following 'specification stage' the requirement description is refined sufficiently until all the information is available to enter the next design stage. Now within the 'design stage', the interfaces between the subsystems and components are set up, for example.

The succeeding 'implementation stage' has been formed in a manner that the entire process model for a subsystem can be projected into this stage itself in order to describe the development of the subsystems as well as components in the same way as the system development process. Therefore, the model branches out into separate design processes for the subsystems and components. After having finished the design processes in each and every branch, the lower level objectives are viewed as met, component and subsystem data are transferred to the system level and integrated into its 'implementation stage'. Now, all EMC-specification data of the previous stages and processes should be available and one is led back to the target system level. At this point the system is fully described, geometrically as well as electrically. With these data sets it is possible to simulate the entire system and/or the subsystems and components also considering EMC constraints within the following stage 'validation'. Up to this design stage, which

might have to be passed several times, no hardware prototype was necessary. Accordingly, all of the data sets determined and validated in the previous design stages have to be converted now into manufacturing specifications to enter the process of prototyping. Finally, in the presented process model the development of an electronic system will be accomplished by the successful termination of the 'test phase', and all of the simulation and measurement data are now available to document the meeting of the previously determined and successively refined development objectives. Here again, several passes may be necessary. However, the 'outer cycle' will be minimized due to a rigorous application of the process model and the simulation results.

The presented process model is capable to describe the development of electronic systems including its subsystems and components completely, where the iterative optimization procedure represents a top-down as well as a bottom-up strategy (multiple level method).

Based on the generalised development process of this chapter, methods with regard to each particular stage can be specified.

Fig. 2 shows the development process and the various possibilities to integrate EMC objectives and methods, respectively. In the following this will be described in more detail.

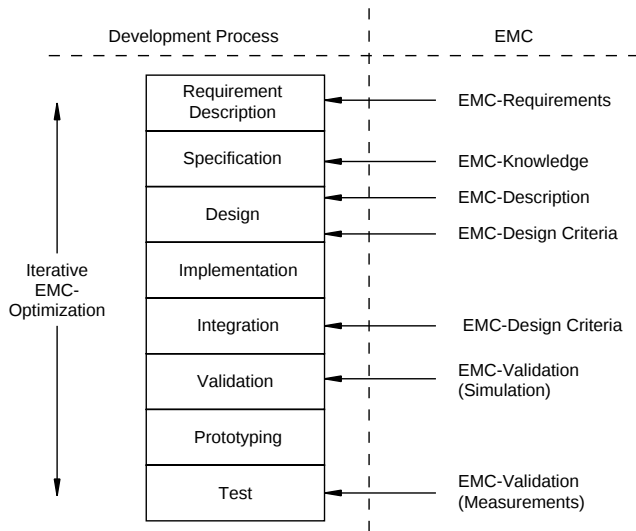


Fig. 2.: Development process and EMC objectives

• EMC-Requirements

The determination of the requirements on the to be developed system with respect to EMC is the starting point for an adequate design. Relevant decisions and objectives are set up. Within this phase, for instance, the basic technology is chosen and applicable directives are determined.

• EMC-Descriptions

The description of components with regard to their EMC status is necessary to determine their susceptibility as well as their emission potential. An EMC-description may contain a collection of EMC-relevant data of a component in

the form of a data sheet. The specifications of this phase are of great importance with respect to the choice of already existing components, too.

• EMC-Design Criteria

EMC-design criteria strongly have to be taken into consideration during placement and routing of the layout. They often can be formulated as rules which, in general, represent some fundamental empirical knowledge, being integrated into the design process in such a manner.

• EMC-Validation

The term 'validation' means to examine the compliance with previously defined EMC-specifications. In general, one has to distinguish between a validation via computer simulations and measurement. The latter presumes the existence of a prototype of a system or parts thereof. Because of cost and time, not to speak of the access to an adequate laboratory and equipment, it is intended to reduce measurement to an absolute minimum. This, in the extreme, can be understood to limit its employment just to document compliance with legal directives, while on the other hand, because of 'time and costs', validation in particular within the iterative EMC-optimization process has to rely on computer simulations. With regard to its capabilities, the EMC-validation by computer simulation has to be located between 'implementation' and 'prototyping' in the generalised design process (Fig. 1), since parasitic effects may not be accessed and therefore, recognised before.

From these specifications the following tasks may be deduced immediately:

- EMC-Analysis:
Determination of EMC-violations via modelling, simulation, EMC-rule checking;
- EMC-Diagnosis:
Assessment and interpretation of analysis results;
- EMC-optimization:
Successive deduction and integration of measures into the system in order to reach the compliance objectives.

As explained above the administration of all distributed design data by an integrated design and analysis environment is of great importance.

Consequently the approach in [1] needs to be augmented in such a way that the EMC-design steps and methodologies are fully integrated into the system design process and not only viewed as an attachment of it. So the use of EMC-aware simulations and measurements now become an integral part of the design process and cannot be viewed decoupled from it. With this merge the construction of an environment supporting EMC-adequate system design is much simpler. As the EMC-design and analysis tools are integrated in the design task an EMC-analysis, for instance, is not only an (optional) attachment but a necessary step.

III. LEAN INTEGRATION PLATFORM

The presented workflow and integration approach (Lean Integration Platform - LIP [2]) constitutes an extensible toolkit for the development of dedicated environments. These resulting environments present themselves as workflow-based approaches to solve certain problems in specific application areas. Although the concept of workflows is not new in the context of business processes and office automation [3, 4], and current standardization efforts are in progress [5] most available workflow-based systems lack the flexibility to integrate arbitrary tools. In the domain of hardware and system design processes this capability is badly needed because the environment has to cope with different tools interacting together.

The functionality of the LIP concentrates on a few basic components that are connected by a standard communication layer, the ITC (inter-tool communication) [7]. The use of this standard has contributed to a scalable modular architecture. In addition to the integration component which functionality has been described in the previous section in detail, the following components form the basic LIP system.

A. Components of the Lean Integration Platform

A.1 LIP Virtual Machine

Tool execution is handled by the LIP Virtual Machine (LVM). This virtual machine consists of distributed local tool launchers that manage tool executions on one particular hosts. The virtual machine supplies in fact the computational power of all allocated hosts. Enabling heterogenous hosts working together it is the basis for multi-platform workflow execution. The integrated tools in the environment are described by a standardized tool encapsulation language, the TES [6]. This format contains all informations like execution path, required and optional inputs and a specification of possible hosts for the execution. So the LVM can handle also requests for tools to execute on one particular host. This scenario is very common if designers are working with expensive licenced tools or tools that reside on special hosts like number-crunchers. If necessary the LVM provides automatic file transfer for the execution.

The LVM keeps all cumbersome details of tool invocation from the other LIP components and of course from the LIP user. Remote tool execution is in no way different from a local computation from this point of view. Of course, for each tool the appropriate parameters are required by the LVM. Otherwise the missing information is prompted from the user in interactive parameter forms.

A.2 Workflow-Engine

The workflow-engine is responsible for the execution of a single workflow. It starts and terminates activities and controls the flow of data-objects. If the activity is bound to a tool-execution the tool-server processes this request asynchronously. According to the status of the data-objects the

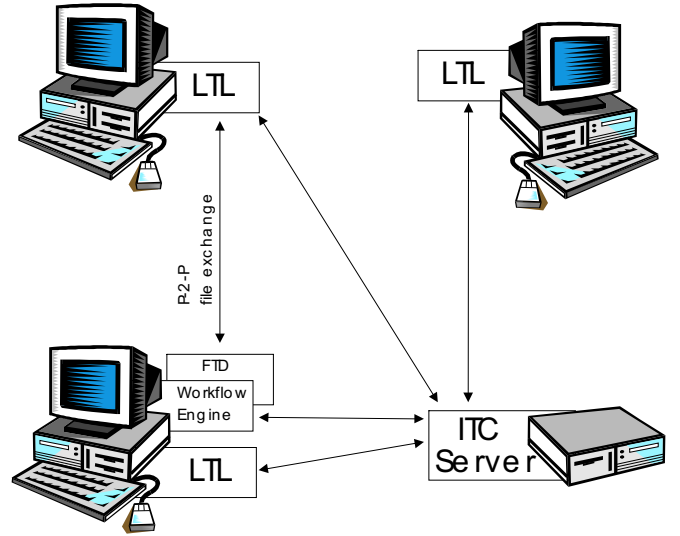


Fig. 3.: LIP virtual machine

execution conditions of activities are computed and displayed. Although the implemented workflow approach tends to hide data dependencies in favour of an action-driven user-interface an integrated data-object browser gives a convenient access to the involved data-objects and the version-manager.

Fig. 4 shows the screen dump of an active engine. This example flow supports the task of performing a simulation with added documentation facilities. The activities display their current state. A blocked state indicates that necessary data for the execution of an activity has not been provided yet or is invalid. Detailed information concerning data object properties are presented in the browser window at the bottom.

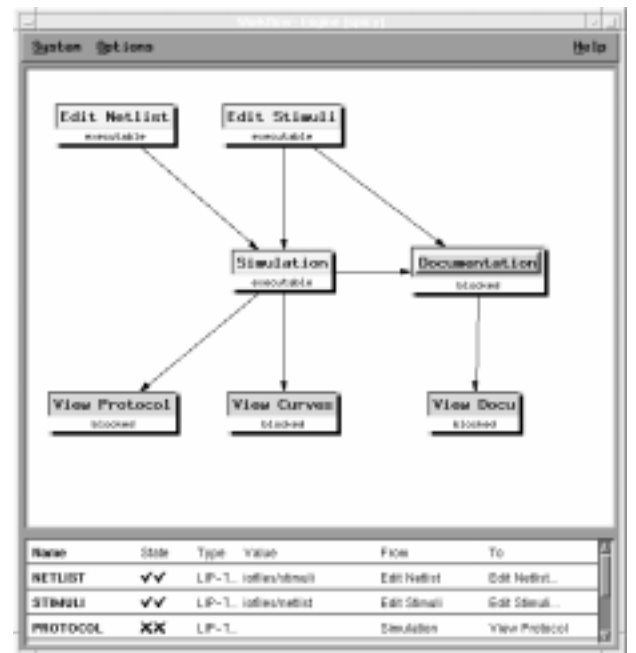


Fig. 4.: Workflow-Engine with example flow

The Documentation activity in the sample flow is a complex activity (which is an important feature of an environment for EMC-adequate system design). With complex activities hierarchical flows can be modeled, for an activity can represent another (sub-)workflow. The start of a complex activity results in starting another workflow-engine for the sub-workflow.

A.3 Workflow-Control-Manager

The feature of structured workflows requires a controlling instance that mediates the data-transfer between flows. This functionality is covered by the Workflow-Control-Manager. In particular it manages the dependencies between dependent flows.

This component gains more importance by establishing a cooperative multi-user environment. In this case data-transfer is not the only issue but the delegation of sub-flows has to be considered additionally. Hence, such concepts as role management, which maintains certain competences in order to organize access to workflows, become relevant in conjunction with a user management functionality. In short the major idea behind delegation is that another user gains responsibility for the execution of a sub-flow or the execution of a successor flow.

A.4 Workflow-Manager

The primary component of a user to create, start or delete new workflows is the Workflow-Manager. In a single-user environment the user selects the appropriate workflow from a repository of workflow-classes and gets a private workflow-instance to work with. The manager displays all created flow-instances of a user. The user can also resume his work on a suspended workflow-instance.

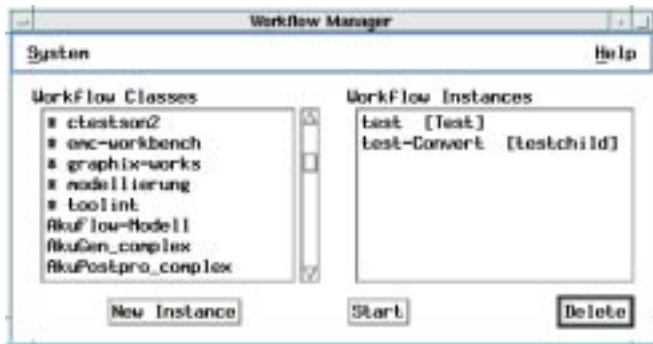


Fig. 5.: Workflow-Manager

Fig. 5 shows the active Workflow-Manager. Public classes are denoted by a leading asterisk in the left subwindow. The right one contains the available workflow instances.

A.5 Workflow-Editor

The Workflow-Editor gives an efficient interface to interactive flow composition and modification. The activities and dataobject of a flow can be defined easily for already integrated tools. With the connection of the input and output ports of the activities the graphical dataflow is entered. With this definition

the Workflow-Editor generates valid workflow descriptions. In addition to the dataflow the visual layout of the workflow can be specified, too. In this view a representation similar to the workflow engine is used.

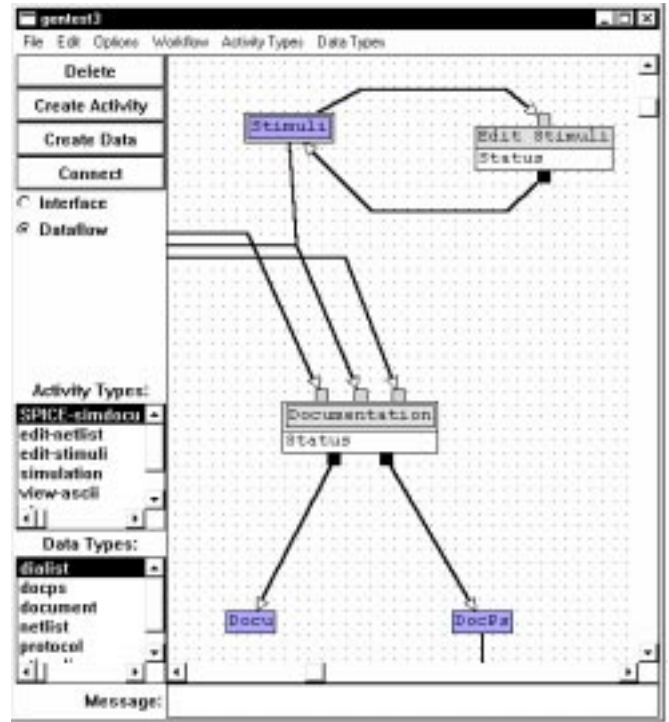


Fig. 6.: Workflow-Editor

B. Scalability

The architecture of the Lean Integration Platform is shown in Fig. 7.

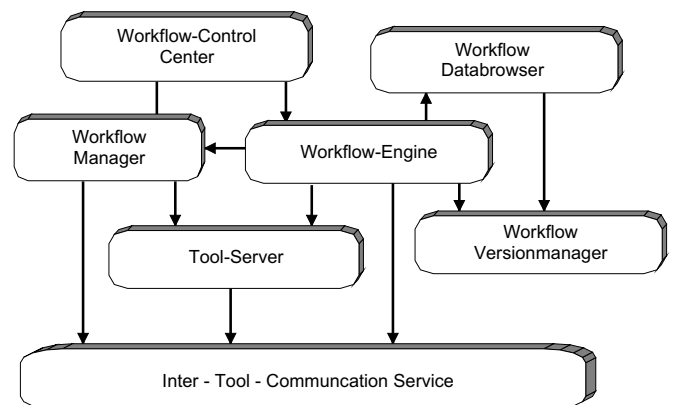


Fig. 7.: Architecture

The individual components provides certain services which are used by other components. All interprocess communication is routed through the ITC communication backbone. So each component can easily be replaced by one or a set of modules that behave identically.

This design allows to tailor the environment to the actual requirements. For instance, if only the tool integration and the execution of workflows is needed, a system stripped down to workflow-engine and tool-server could be appropriate. For instance, if additional modules for intra-workflow version-management and databrowsing are installed this functionality is available in the workflow-engine.

The advantages of this scalability can be pointed out clearly: On the one hand the user only gets the system actually needed. This reduces the complexity of the system. On the other hand the the open architecture of the LIP allows to replace components by more sophisticated ones. Additionally value-adding components such as project-management or a product-data-management can be developed independently or, which may be more practical, existing systems could integrate components of the workflow environment themselves and, for example, start workflows on data-objects directly from a product data management system.

IV. EMC-DESIGN AND ANALYSIS WORKFLOW (SIGNAL INTEGRITY)

The analysis of 'internal' EMC effects like delay, reflection, crosstalk and groundbounce (signal integrity analysis) requires different tools, algorithms and models [8, 9, 10, 11].

To support EMC-adequate designs with the Lean Integration Platform it is necessary to reflect on the design issues mention in section II and derive corresponding flows. As the LIP allows the augmentation of its flow repository it it sensible to deal with some typical EMC-design tasks first and to move on with more complete system design flows later. Because workflows can be reused this means no reduction in the effectiveness of this approach.

Based on the task to handle the signal integrity problems 'reflection' and 'crosstalk' at a prelayout phase a simple flow has been designed.

The workflow for supporting the analysis of single-integrity-problems is depicted in Fig. 8.

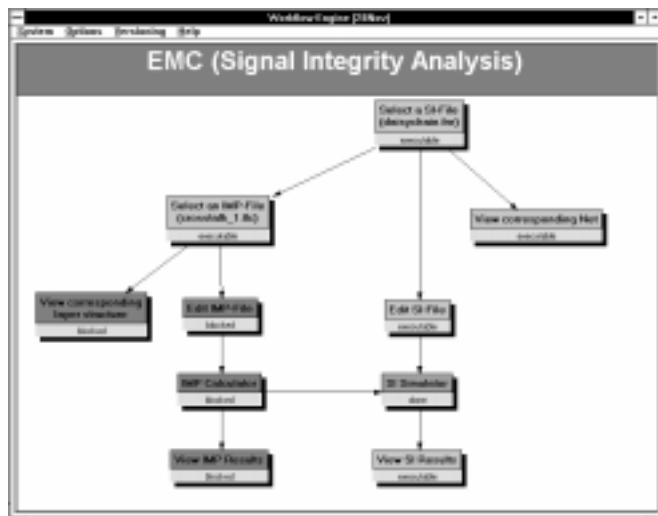


Fig. 8.: Main flow of PCB SI-analysis

This workflow has been divided into two parallel flows. The left one is for the calculation of transmission line parameters on PCB while the flow on the right side shows the main SI-analysis. The workflow is built up to enable a calculation of transmission line parameters in combination with a SI-analysis as well as only a SI-analysis for already determined parameters.

At the beginning of the SI-analysis a subproblem to work on has to be chosen. The selection of the SI-problem closes the following activities as no valid input data exist (daisy chain circuit).

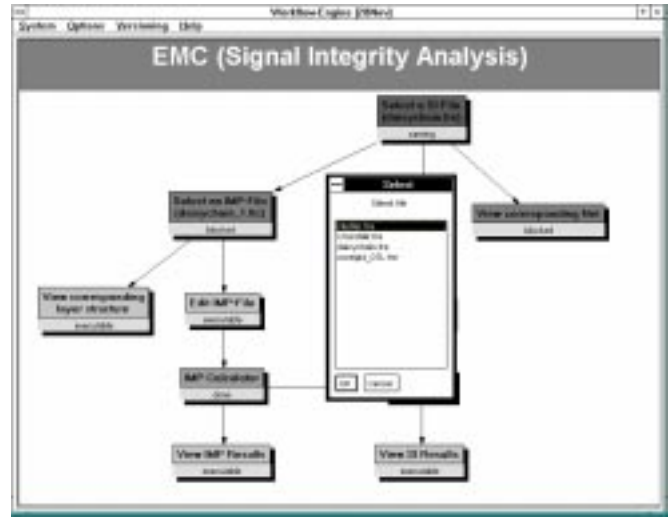


Fig. 9.: Selection of a specific SI-problem

After the selection of a SI-subproblem it is possible to present it, supported by a visual tool, in an abstract way. This enables an easy recognition of the SI-subproblem.

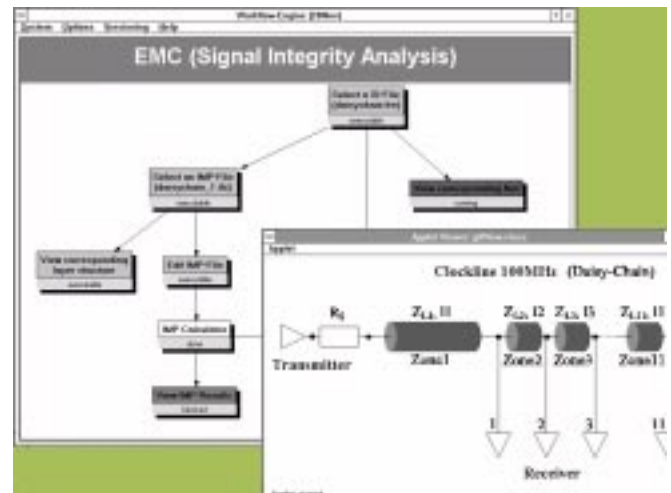


Fig. 10.: Visualization of a SI-subproblem

At the workflow on the left side the layer structure has to be chosen for the determination of the transmission line parameters (Fig. 11).

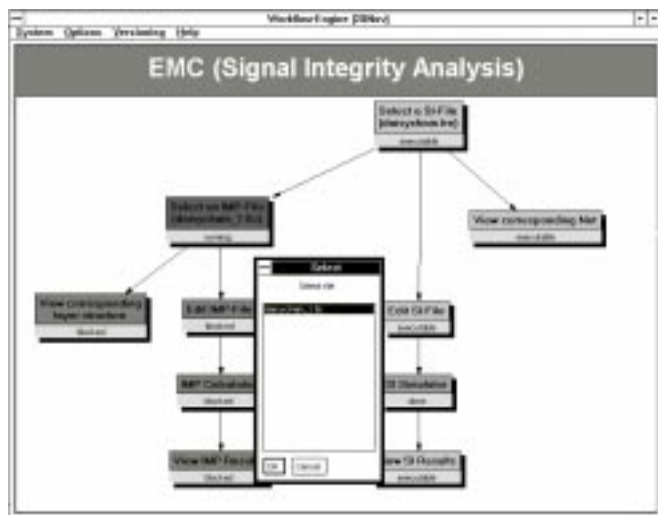


Fig. 11.: Selection of a layer structure

After the selection of the layer structure it is possible, just as on the other side, to be shown one part of the chosen structure (stripline, Fig. 12).

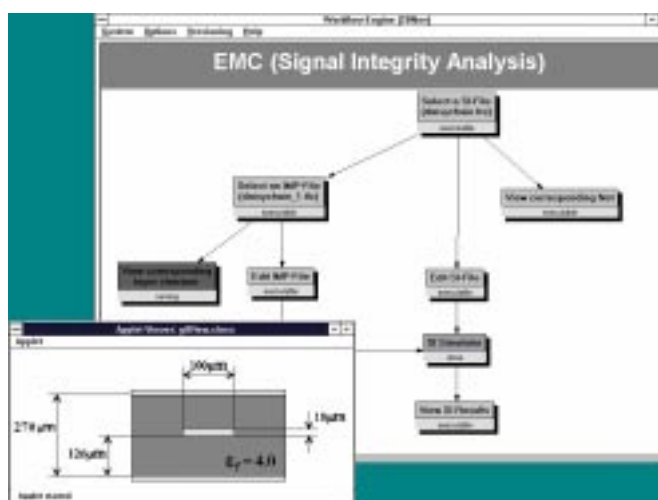


Fig. 12.: Visualization of a part of a PCB layer structure

The chosen layer structure may still be changed while starting an editor and generate new data for transmission line parametrization.

The already edited input file is now used for the calculation of transmission line parameters. The result may also be presented via a visual tool.

Transmission line parameters calculated in the left-side part of the workflow are made available for the SI-simulator automatically to calculate the SI-subproblem. For the simulation an input file is used, too, also changeable by an editor (see Fig. 8).

The results of the SI-analysis can be presented by a visual tool. The PCB circuit designer may draw conclusions from the signal behaviour and then change the layer structure (left-side workflow) or the class of circuit structure (star routing for example; right-side workflow) to reduce or avoid the SI-violations.

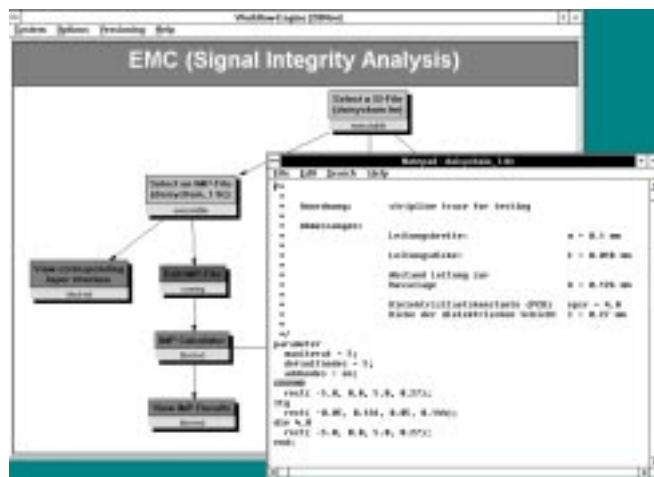


Fig. 13.: Transmission line parametrization

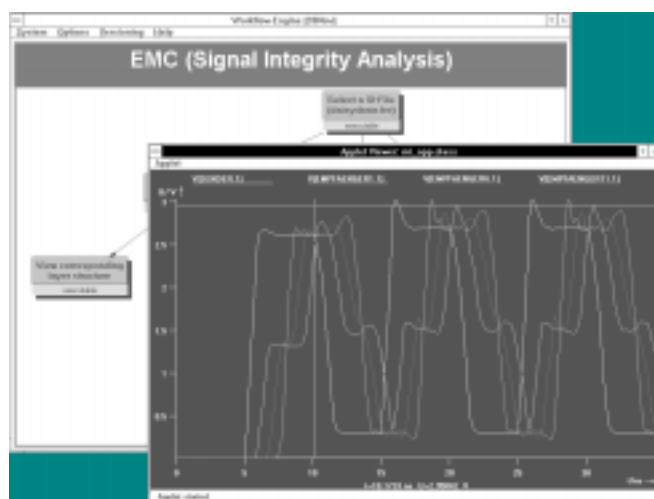


Fig. 14.: Signal behaviour on the transmission lines

V. SUMMARY

Engineering efforts in order to guarantee the EMC of electronic systems have been drastically aggravated due to an ever increasing demand for higher performance. In order to meet economic requirements like 'time to market' and 'cost reduction', new approaches have to be employed. It has been shown that the compound of constraints one is confronted with can only be accounted for satisfactorily by a systematical consideration of EMC objectives at all design stages of a development process.

In order to obtain a general approach in describing the integration of EMC constraints into a domain specific development process a model based on the characteristic design stages has been discussed. This strategy to incorporate EMC constraints into existing development processes opens up the possibility to create user specific design and analysis environments, also including various sets of EMC tools.

Within this paper a signal-integrity-analysis environment with integrated SI-tools has been presented. This environment is based on a workflow oriented integration approach (LIP).

Nevertheless, due to the increasing complexity of leading edge designs of electronic equipments the development of methods and tools which are capable to support EMC adequate design of complete systems will remain of prime importance and a great challenge for industry within the next decade.

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