Power Consumption in CMOS Combinational Logic Blocks at High Frequencies

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Abstract— A new model for estimating dynamic power dissipation in CMOS combinational circuits at differing voltages is presented in this paper. The proposed model deals with power dissipation of circuits at saturation frequencies, where the output voltage does not reach 100% of the supply voltage and the output voltage waveform is almost a triangular waveform. In this paper we show that the dynamic power consumption at *saturation frequencies* is only dependent on the supply voltage, and is independent of load capacitance and switching speed. This model shows that when a circuit is working in the saturation frequency range, as the frequency is increased, the performance/power ratio is increased. However, this increase in performance/power ratio is at the expense of noise margin. The model is theoretically and empirically shown to be correct. This model can be used to design a system where the differing combinational logic blocks are supplied with differing voltages. Such a system would consume lower power than if the system was supplied by a single voltage rail.

I. Introduction

With increasing need for low power systems, reduction of power consumption has become a critical concern in recent years. Several researchers have been working in the area of modelling digital circuits in order to reduce power consumption [1] [2] [3] [4] [5] [6][3] [7] [8][9] [10][11]. The existing methods usually calculate the dynamic power consumed by a CMOS combinational circuit with the formula,

$$P = C_L V_{dd}^2 f, \tag{1}$$

where C_L is the load capacitance of the circuit, V_{dd} is the power supply, and f the switching frequency of the circuit. The above formula assumes that the transistors in the circuit are fully charged or discharged. Figure 1 shows the N-type transistor's output characteristics in a CMOS inverter. The dotted lines shown in Figure 1(a) traces the output voltage of the inverter when the input voltages is varied between 0 and 5 volts. Figure 1(b) shows that when the output capacitor is not fully discharged, and the switching is done sufficiently fast, the transistor remains mostly in saturation . In this case, the circuit can be assumed to be in saturation, and further has constant current when discharging.

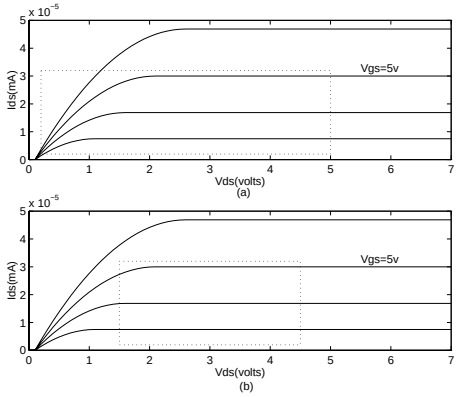

Fig. 1. Output Characteristics of CMOS

In this paper we derive equations for power consumption with low supply voltages and high frequencies in mind. We derive the model for power consumption for circuits where the frequency of switching is so high that the output waveform is triangular rather than square and does not reach 100% of the supply voltage. (Akira in [12], has suggested that the dynamic power could be reduced by applying triangular waveforms).

The rest of the paper is arranged as follows: the equations for power consumption is derived in the next section; the third section shows the experimental results; section four gives simulation results and finally in section five we

ASP-DAC '97
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conclude this paper.

A. Motivation

A large system (such as a microprocessor) is usually made up of smaller components. These components can either be made of combinational logic blocks or synchronous logic blocks. All components of the system are supplied by a single voltage level(usually 5V or 3.3V). In a synchronous system, there is usually only one critical path (with the longest delay) which will govern the speed at which the entire system is to be clocked. In a single supply voltage system the ability to reduce power by reducing voltage and maintaining performance is limited, since the critical path delay is dependent upon the supply voltage. There will be other delay paths in the system which are not critical. The voltages in these paths could be reduced without affecting the overall performance of the system. By carefully designing the system allowing differing voltages for differing paths, the total power consumption can be reduced.

The possibility of the use of several voltages in a system is enhanced by the use of battery powered applications. In battery powered applications, such as laptops, the available voltage is usually given by several cells connected in series. The cells can be tapped individually to get differing voltage levels. These differing voltage levels can supply different sections of a system in order to reduce the total consumed power.

In this paper we have shown the power performance ratio of combinational logic circuits at differing voltages and at differing frequencies. This analysis will be useful in making circuits which will consume lower power with enhanced performance. With the work presented in this paper, it will be possible to design data-paths where the combinational logic blocks will be at differing voltages, which will reduce the total power.

B. Definitions

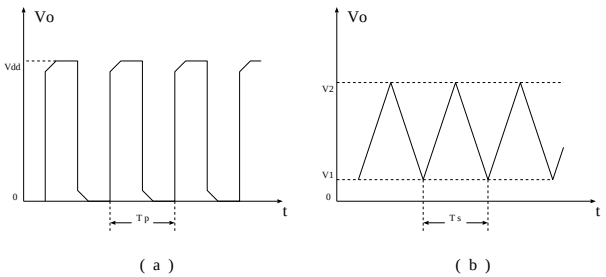

Fig. 2. Output waveform in *normal region* (a) and in *saturation region* (b)

- Propagation Delay, T_d; the time taken for a logic transition to pass from input to output, which is defined as the time difference between input transition (50 percent level) and the 50 percent output level. As the output rise and fall time is dominant, the delay is approximately given by the average of the fall time and rise time of the circuit.
- Normal Region; when a CMOS circuit has the total charging and discharging at the output, the circuit is said in normal region, as shown in Figure 2(a).
- Saturation Region; if a circuit does not charge and discharge completely at the output, this circuit is regarded to be in the saturation region, as shown in Figure 2(b).
- Normal Frequencies; the frequencies at which the circuit works in the normal region.
- Saturation Frequency, f_s; the frequencies at which the circuit works in the saturation region.

II. Mathematical Modelling

The mathematical model used for estimating power fails when using varying voltages at high frequencies. While the model is quite satisfactory for circuits at normal frequencies. In this section the power consumption of combinational circuits with varying voltages at saturation frequencies is analysed .

A. Power at Saturation Frequencies

For a single CMOS inverter, the power dissipation in the normal region is given by,

$$P_{normal} = C_L {V_{dd}}^2 f \tag{2}$$

where C_L is the load capacitance, f is the switching frequency of the circuit, and V_{dd} is the supply voltage.

At higher switching frequencies, the power consumed by the combinational circuits have to be computed differently, since the transistors do not have time to completely charge nor discharge, but are partially charged and discharged. At this time, the circuit could be assumed to be working at saturation frequencies.

The dynamic power of an inverter (Figure 3) at these frequencies can therefore be shown as:

$$\begin{aligned} P_{sat} &= \frac{1}{T_s}\int_0^{T_s/2} i_n(t) v_o dt + \frac{1}{T_s}\int_{T_s/2}^{T_s} i_p(t)(V_{dd} - v_o)\, dt \\ &= \frac{C_L}{T_s}\int_{V_1}^{V_2} v_o dv_o + \frac{C_L}{T_s}\int_{V_2}^{V_1} (V_{dd} - v_o) d(V_{dd} - v_o) \\ &= \frac{C_L}{T_s}(V_2 - V_1) * V_{dd} \end{aligned} \tag{3}$$

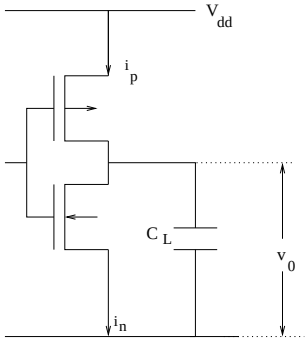

Fig. 3. *CMOS Inverter*

where $T_s = 1/f_s$ is the switching period, V_1, V_2, the lower and high voltages at the output, as shown in Figure 2.

Because the circuit is in the **saturation area**, $V_2 - V_1$ can be approximately assumed to be determined by the saturation current of the circuit, given by $\beta/2(V_{dd} - V_t)^2$, β is the CMOS transistor gain factor.

$$V_2 - V_1 = \frac{1}{C_L}\int_o^{T_s/2} i_c\,dt \tag{4}$$

$$= \frac{1}{C_L}\int_0^{T_s/2} \frac{\beta}{2}(V_{dd} - V_t)^2\,dt \tag{5}$$

$$= \frac{\beta}{2C_L}(V_{dd} - V_t)^2\frac{T_s}{2}. \tag{6}$$

Therefore,

$$P_{sat} = \frac{\beta}{4}(V_{dd} - V_t)^2 * V_{dd}.$$

The formula can also be written as

$$P_{sat} = \frac{\beta}{4} * \frac{V_{dd}}{V_{dd} - V_t}(V_{dd} - V_t)^3 \tag{7}$$

$$= \frac{\beta}{4} * \frac{1}{1 - \frac{V_t}{V_{dd}}}(V_{dd} - V_t)^3 \tag{8}$$

Let $\frac{V_t}{V_{dd}} = k$, obviously $k < 1$. Applying Taylor's series, We can obtain the approximation as

$$P_{sat} = \frac{\beta}{4} \cdot 1.24 \cdot (V_{dd} - V_t)^3 \tag{9}$$

$$= k'(V_{dd} - V_t)^3 \tag{10}$$

where k' is a constant. From Equation 10, it can be seen that the dynamic power consumption is independent of the load capacitance and switching frequency in the saturation region. Note, however, that the noise margin is reduced as the frequency and the capacitance is increased. Despite this reduction in noise margin, that circuits can be operated successfully at saturation frequencies, resulting in superior performance / power ratio.

As has been proven in [14] that when the supply voltage, V_{dd}, is changed, the delay is not simply inversely proportional to V_{dd}, instead

$$T_d \approx \frac{k_{td}C_L}{\beta(V_{dd} - V_t)} \tag{11}$$

i.e., the delay, T_d, is inversely proportional to $(V_{dd} - V_t)$. Then

$$P_{sat} = \frac{k''}{{T_d}^3} \tag{12}$$

From equation 12 it can be seen that for a fixed combinational circuit (with constant capacitance) dynamic power dissipation is approximately equal to the inverse of the propagation delay cubed.

Furthermore, we can derive the formula which relates the delay and *saturation period, T_s*, which is defined as the inverse of saturation frequency, f_s.

When the circuit is in the **saturation area,** the output amplitude $(V_2 - V_1)$ is smaller than V_{dd}. Therefore the amplitude ratio a is given by:

$$a = \frac{V_2 - V_1}{V_{dd}}. \tag{13}$$

substituting equation 6 in the above equation (Equation 13)

$$aV_{dd} = \frac{\beta}{4C_L}(V_{dd} - V_t)^2 T_s \tag{14}$$

Therefore,

$$T_s = \frac{4aC_L V_{dd}}{\beta(V_{dd} - V_t)^2} \tag{15}$$

$$\approx \frac{K_b C_L a}{V_{dd} - V_t} \tag{16}$$

Substituting equation 16 in equation 10,

$$P_{sat} = \frac{K_{ts}{C_L}^3 a^3}{{T_s}^3} \qquad a < 1 \tag{17}$$

where K_{ts} is a constant.

Also note that by substituting equation 11 in equation 16, we get

$$T_s = K_{td}.a.T_d \tag{18}$$

where K_{td} is a constant. The delay of a circuit can be determined by knowing the working frequency and the amplitude ratio.

III. Experimental Results

The experimental procedure was created in order to verify the theoretical equation for P_{sat}. The verification of power being independent of operating frequency at saturation frequencies was also performed. The relationship between T_s and T_d was also confirmed.

The measurements were performed with the aid of a power supply which was used to control the value of V_{dd};

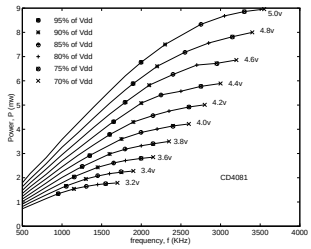

Fig. 4. *Power vs Frequency with different Voltages*

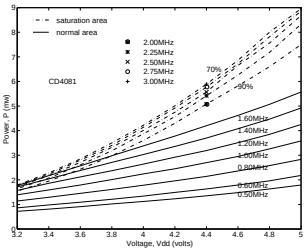

Fig. 5. *Power vs Voltage with different frequencies*

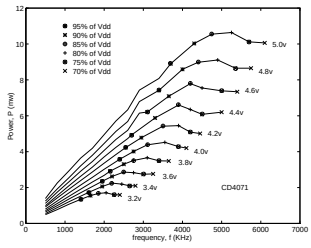

Fig. 6. *Power vs Frequency with different Voltages*

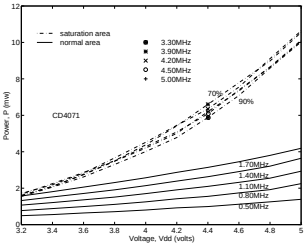

Fig. 7. *Power vs Voltage with different frequencies*

a function generator which was used to provide the input signals; a multi-meter which measured the average current; and a cathode ray oscilloscope which measured T_d and a. The entire system was controlled by the LabVIEW software system [15].

A. Power

Figures 4, 6 and 8 plots graphs with power versus frequency for differing voltages for chips CD4081, CD4071 and CD4023. Figures 5, 7, and 9 plots graphs with power versus voltage, for differing frequencies for chips CD4081, CD4071 and CD4023. Equation 2 shows that dynamic power dissipation is linear in the normal region. Equation 10 shows that the power dissipation is constant in the saturation region for a constant voltage. As can be seen from these plots (Figures 4 to 9), at normal frequencies, the power consumption rises almost linearly with frequencies. At saturation frequencies, the power consumption reaches almost a constant value.

There are minor anomalies in the plots which are not predicted in the theory. These anomalies can be attributed to a combination of factors. The first factor is the short circuit current (which rises with frequency) [2]; the second factor is the fact that the circuit is not completely in the saturation area when the amplitude of the output is close to V_{dd}; and the final factor is that the output is not symmetrical in the saturation area, due to the differing speeds of P-type and N-type MOS transistors.

Finally, several circuits were tested to show the power dissipation model of the circuits in the **saturation region**. The result are presented in Table I, where the first column gives the name of the gate tested, the second gives the regression formula of power versus propagation delay. The last column presents the corresponding data-fitting variance (δ). These results prove that Equation 12 is correct. The constant power in the equation can be attributed to short circuit and leakage currents.

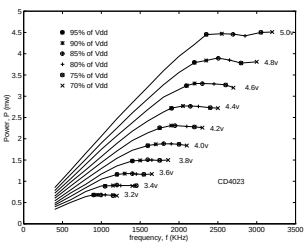

Fig. 8. *Power vs Frequency with different Voltages*

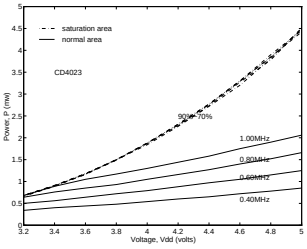

Fig. 9. *Power vs Voltage with different frequencies*

TABLE I
EXPERIMENT RESULTS

gate	$P(mw) \sim T_d(ns)$	δ
CD4011	$P = 0.97 + 494445771T_d^{-3}$	0.35
CD4030	$P = 1.22 + 628951431T_d^{-3}$	0.87
CD4023	$P = 0.72 + 806836671T_d^{-3}$	0.11
CD4081	$P = 0.52 + 472939231T_d^{-3}$	0.98
CD4000	$P = 0.40 + 1471119784T_d^{3}$	0.01
CD4000	$P = 0.48 + 1395191407T_d^{-3}$	0.18
CD4012	$P = 1.79 + 191373499T_d^{-3}$	1.58
CD4071	$P = 1.49 + 227556207T_d^{-3}$	0.48

B. Other Confirmations

In this section we proceed to confirm equation 18. Equation 18 states

$$T_s = K_{td}.a.T_d.$$

Therefore $\frac{T_s}{T_d}$ should be a constant for any voltage. Figures 10 and 11 have plotted $\frac{T_s}{T_d}$ versus voltage for components CD4023 and CD4030. As can be seen from the plots, $\frac{T_s}{T_d}$ is approximately a constant. There is slight increase in $\frac{T_s}{T_d}$ as voltage increases, but this could be due to the approximations in the equations, and measurement errors.

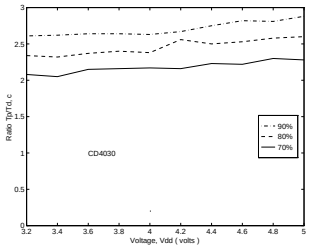

Fig. 10. *Power vs Voltage with different frequencies*

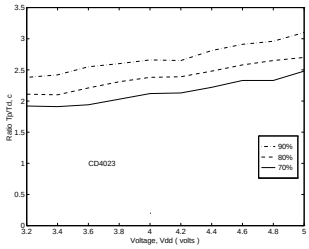

Fig. 11. *Power vs Voltage with different frequencies*

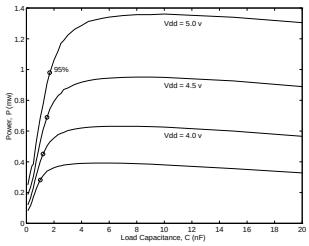

Fig. 12. *Power vs Load Capacitance with different Voltages*

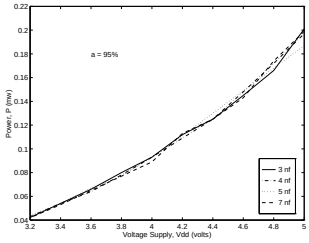

Fig. 13. *Power with different load capacitances in Saturation Region*

IV. Simulation

We used SPICE to simulate CMOS circuits in order to ascertain some of the equations given in Section II of this paper. The simulation was performed on circuits which were assumed to be symmetrical with transistors of width 5 um and length of 20 um. The results of the simulation are given below.

A. Power is Load Capacitor Independent

Figures 12 and 13 show the effect of the load capacitance on the power consumption when the circuit is in the **saturation region** . From figure 12, it can be seen that the power consumption increases as the capacitance increases in the normal area. But when the circuit goes into the **saturation area**, the power consumed is independent of the load capacitance. Figure 13 shows the plot of Power consumption versus V_{dd} at differing capacitances for a circuit just in saturation (output is 95% of V_{dd}).

B. Power is Switching Frequency Independent

In this section we show that the power dissipation is independent of switching frequency at saturation frequencies. The theory for this is derived in Section II.

As can be seen in Figure 14, at saturation frequencies, the power consumed becomes constant. Note however, that at saturation frequencies, the amplitude becomes smaller as the frequency increases.

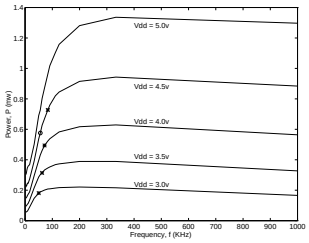

Fig. 14. *Power vs Frequency*

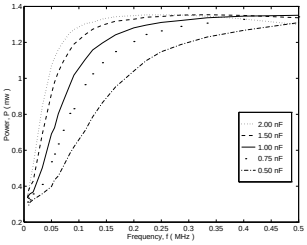

Fig. 15. *Effect of C and f on Power Consumption in the Saturation Region*

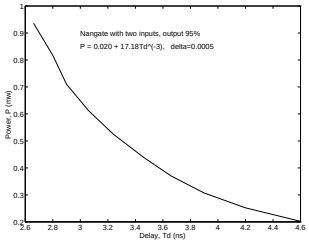

Fig. 16. *Power Consumed by NAND-gate*

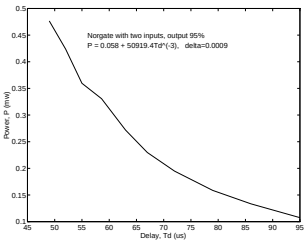

Fig. 17. *Power Consumed by NOR-gate*

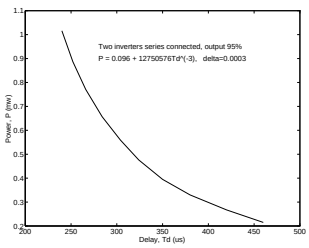

Fig. 18. *Power Consumed by the two-series-connected inverters*

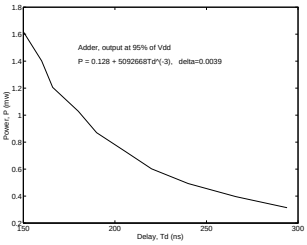

Fig. 19. *Power Consumed by An Adder*

C. Power Formula in Other Circuits

Figures 16, 17, 18 and 19 give plots of power dissipated versus delay (varied by varying the voltage) for four different circuits. Figure 16 shows the plot for a NAND-gate, Figure 17 shows the plot for a NOR-gate, Figure 18 shows the plot for a half-adder circuit and finally Figure 19 shows the plot for a two inverters connected in series. All of the above simulations demonstrate that the power consumed by a combinational logic circuit is proportional to the delay cubed. The power versus delay formula for each plot is given alongside each of the plots.

D. Power, Capacitance and Saturation

As can be seen in Figure 15, when load capacitance increases, the circuit goes into saturation frequencies at lower frequencies. In Equation 16, it can be seen that as

C_L increases, $T_s(1/f_s)$ will also increase. This shows that as load capacitance increases, the frequency needed to go into saturation is reduced.

V. Conclusion

The common problem that designers deal with, is to find an optimum trade-off between power consumption and high performance. The models given in this paper will better facilitate designers in building systems which perform at higher frequencies and with low power.

In this paper we have looked at CMOS combinational circuits running at very high switching frequencies, so that their performance/power ratio is increased. These frequencies are so high that the output is more triangular rather than square. We have derived models for voltage versus propagation delay, and for power at saturation frequencies. At these frequencies the power is shown to be frequency and load capacitance independent, and only dependent on the supply voltage. However it must be noted that, as the load capacitance increases, the frequency at which the circuit goes into saturation will decrease. Further, it must also be noted that as the frequency is increased to higher and higher levels, the amplitude of the output is decreased. All these results can be expected to be useful in reducing power and upgrading performance of CMOS circuits.

VI. Acknowledgement

We are indebted to Dr Y. T. Yeow for several interesting and enlightening discussions. We would also like to thank Mr. Peter Allen for his valuable help during the experiments.

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