CB-Power: A Hierarchical Cell-Based Power Characterization and Estimation Environment for Static CMOS Circuits

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Abstract — In this paper, we present CB-Power, a hierarchical cell-based power characterization and estimation environment for static CMOS circuits. The environment is based on a cell characterization system for timing, power and input capacitance and on a cell-based power estimator. The characterization system can characterize basic, complex and transmission gates. During the characterization, input slew rate, output loading, capacitive feedthrough effect and the logic state dependence of nodes in a cell are all taken into account. The characterization methodology separates the power consumption of a cell into three components, e.g., capacitive feedthrough power, short-circuit power, and dynamic power. With the characterization data, a cell-based power estimator (CBPE) embedded in Verilog-XL is used for estimating the power consumption of a circuit. CB-Power is also a hierarchical power estimator. Macrocells such as flip-flops and adders are partitioned into primitive gates during power estimation. Experimental results on a set of MCNC benchmark circuits show that CB-Power provides within 6% error of SPICE simulation on average while the CPU time consumed is more than two orders of magnitude less.

I. Introduction

In the past, the main objective for circuit designers has been to design fast and compact digital systems. However, recent trends in portable consumer electronics and advances in deep-submicron have resulted in an increasing demand for low power digital systems. Therefore, the challenge for the circuit designers has become to consider joint optimization not only of area and speed but also of power.

Power reduction can be achieved at various abstraction levels ranging from layout and technology to architecture and system. No matter which level it is, a fast and accurate power analysis tool is necessary to quickly obtain the power consumption information in the designs. A direct and simple method of obtaining this information is through a circuit level simulator (e.g., SPICE). Although accurate, SPICE suffers from severe memory and execution time constraints and thus is not suitable for large circuit designs. Recently, a large number of power estimators have been proposed to overcome this problem [1-10]. Among them, several cell-based power estimators [1-5] provide SPICE-like accuracy but with simulation speeds superior to SPICE.

To develop a cell-based power estimator, power characterization is a must step. The difficulty in power characterization is that the power consumption of a cell in a circuit is highly dependent on the transition probabilities of the input signals, the input slew rate, the output loading and the logic state dependence of the nodes in the cell. To estimate the power consumption more accurate, these effects should all be taken into account during characterization. Moreover, due to the advance of technology process, cell library may be upgraded very often. Therefore, building an automatic cell characterization system is important and necessary.

In this paper, we present **CB-Power**, a hierarchical **C**ell-**B**ased **Power** characterization and estimation environment for static CMOS circuits. This power analysis environment is shown in Fig. 1. As shown in Fig. 1, **CB-Power** contains two major parts: power characterization system and power estimation system. In power characterization system, we use a modified state transition graph called STGPE, which was proposed in [1] and [11], to model the power consumption behavior of basic, complex, and transmission gates in the cell library. Then, we use SPICE simulation to characterize the power consumptions associated with each edge in the STGPE. In our methodology, the power consumption of a cell is separated into three components [11] : (1) capacitive feedthrough power, which is measured from the coupling currents of the parasitic capacitances that distribute among the gate, source, drain and bulk terminals, (2) short-circuit power, which is the result of the direct current from supply to ground during the switch of a gate, and (3) dynamic power, which arises when the circuit capacitance of a CMOS circuit is charged or discharged. The purpose of this separation is to provide not only an accurate power estimation of the whole circuit, but also the detail information of individual gate. Those information could be very useful for the power optimizations [12].

In addition to power characterization, we also characterize the rise/fall delay, propagation delay, and input capacitance for each cell in the cell library. After running characterization with different input slew rates and output loadings, we fit the characterization data into some empirical formulas and store them in the database

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for power estimation.

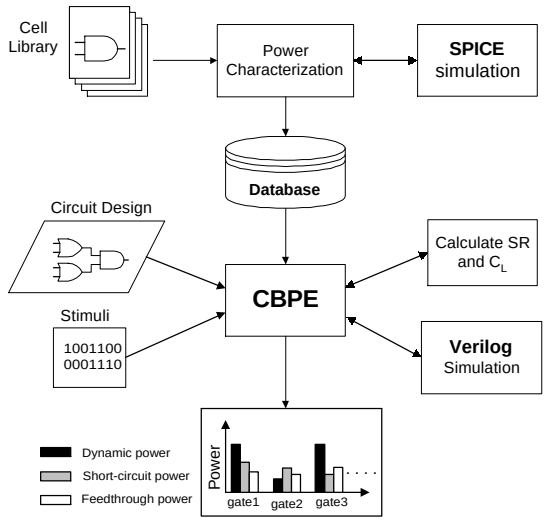


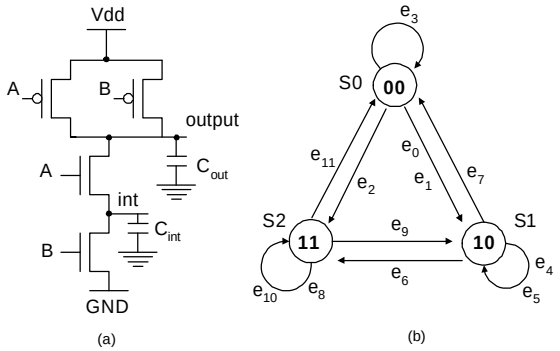
Fig. 1 The CB-Power power characterization and estimation environment.

In power estimation system, we use a Cell-Based Power Estimator (**CBPE**) [1] to estimate the power consumption of a circuit. Given a cell-based circuit design and the stimuli, the CBPE first calculates the input slew rates (SR) and output loadings (C_L) using the database for each gate in the input circuit and then performs Verilog simulation for finding the signal probabilities (the probability of a signal being one) and the transition densities (average number of signal transition per unit time) of each node in the circuit. With those information, CBPE finally calculates the average power consumption of the input circuit over the simulation period and also reports the three power components for each gate in the circuit.

CB-Power estimates the power consumption of a macrocell by using a hierarchical approach. That is, macrocells such as DFF, XOR and adder are partitioned into the primitive gates such as basic, complex and transmission gates. Therefore, power consumption of macrocells can be obtained by summing up the power consumption of the constituting primitive gates. Experimental results on a set of MCNC benchmark circuits show that CB-Power could provide accuracy within 6% error of SPICE results on average.

II. Power Consumption Model in CB-Power

For a CMOS logic gate, the states of the output node and the internal nodes depend both on the input patterns and their previous states. CB-Power uses a modified state transition graph called STGPE to model this sequential behavior. Without loss of generality, we use a 2-input NAND gate and its corresponding STGPE shown in Fig. 2 to demonstrate how the STGPE models the power consumption behavior of a logic gate. In Fig. 2, the state bits from the MSB (most significant bit) to LSB (least significant bit) represent the status of the nodes that are located sequentially along the path from the power supply to the ground end. For example, state 10 represents "output"=1 and "int"=0. It is worthy to know that state 01 does not exist in Fig. 2(b). This is because that the discharging path of the output node passes through the internal node. Therefore, when the output node is discharged, the internal node between output and ground is discharged too. This situation is also valid for NAND gates with more than two inputs. Based on this state encoding, it is impossible to have a state with the less significant bit being one while the more significant bit being zero. Therefore, if a NAND(NOR) gate has *m* inputs, the state number of the corresponding STGPE would be *m+1*. Similarly, the same state encoding strategy can be applied to NOR gates.



$e_k:(i_k,E_k,W_k)$ $\quad i_k:(AB)$

$e_0:(00,E_0,W_0)$ $e_1:(01,E_1,W_1)$ $e_2:(10,E_2,W_2)$ $e_3:(11,E_3,W_3)$
$e_4:(00,E_4,W_4)$ $e_5:(01,E_5,W_5)$ $e_6:(10,E_6,W_6)$ $e_7:(11,E_7,W_7)$
$e_8:(00,E_8,W_8)$ $e_9:(01,E_9,W_9)$ $e_{10}:(10,E_{10},W_{10})$ $e_{11}:(11,E_{11},W_{11})$

Fig. 2 The STGPE of a 2-input NAND gate.

For each edge in STGPE, the label $e_k:(i_k,E_k,W_k)$ is used to model the power consumption of the state transition from one state S_m to another state S_n under the input pattern i_k. E_k is the edge activity number, which denotes the traverse times of edge e_k when a set of sequential patterns are applied, and W_k is the total energy consumption when edge e_k is traversed each time. Therefore, if we know the edge activity number and the energy consumption of each edge in STGPE, the total energy consumption of the logic gate can be obtained by summing up the products of the edge activity number and the energy consumption of each edge. In other words, if a logic gate PG_r has *m* inputs, then its energy consumption can be written as

$$Energy(PG_r) = \sum_{k=1}^{(m+1)\times 2^m} E_k \times W_k. \quad (1)$$

Assume that a circuit *CK1* has *M* logic gates and *N* sequential input patterns are applied into the circuit with clock cycle time *T*. Then, the average power consumption of *CK1* can be calculated as

$$P_{avg}(CK1) = \frac{\sum_{r=1}^{M} Energy(PG_r)}{N \times T} . \quad (2)$$

As mentioned above, it is easy to construct the STGPE of a basic gate. However, for a complex gate, the construction would become more complicated. This is because there possibly have multiple charging or discharging paths for the internal nodes and thus the state encoding strategy of basic gates can not be applied. For example, for an AOI23 example as shown in Fig. 3(a), there are four internal nodes and an output node. The gate initially have 32 states in the corresponding STGPE where we encode the status of the nodes 2, 3, 4, 5, and 6 by the bits from MSB to LSB. After removing some illegal states such as 01000 and 11001, there are still 14 states. Therefore, the final STGPE have 14 states and 448 (14 2^5) edges. Obviously, handing this graph is not a easy task. Therefore, we use a simplified model to model the power consumption of complex gates.

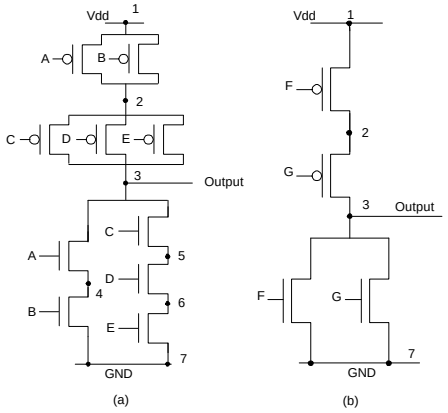


Fig.3 An AOI23 gate and its simplified circuit.

In a complex gate, we classify the nodes into **primary nodes** and **secondary nodes**. Primary nodes are the nodes which must be passed whenever output node is charged or discharged. The other nodes not belonging to the primary nodes are called secondary nodes. In the AOI23 example, the primary nodes include nodes 1, 2, 3 and 7 and the secondary nodes include nodes 4, 5 and 6. In our approach, we estimate the power consumption of a complex gate in two major steps. In the first step, an AOI(OAI) gate is simplified into an equivalent NOR(NAND) gate which retaining the primary nodes only, like the simplified circuit shown in Fig. 3(b). Then, we build the corresponding STGPE for the equivalent NOR(NAND) gate and estimate the power consumption of the primary nodes as the manner of basic gates. In the second step, we can build the STGPE for the secondary nodes and estimate their power consumption. The power consumption of the AOI(OAI) gate can then be obtained by summing up the power consumption of the primary nodes and the secondary nodes. Due to the limitation of space, we do not describe the power model clearly in this paper. Details of the power models of AOI, OAI and transmission gates are shown in [11].

III. Power Characterization System in CB-Power

In this section, we briefly describe the power characterization system in CB-Power. This system characterizes the propagation delay, rising/falling delay, input capacitance and power consumption of each cell in the cell library. The characterization procedure is shown in Fig. 4.

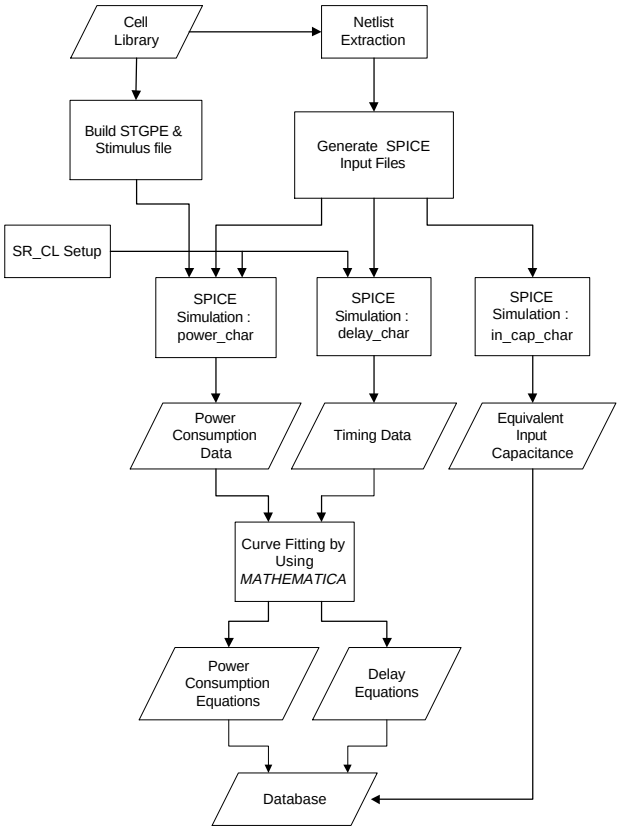


Fig. 4 Cell characterization flow.

For each cell in the library, we build the corresponding STGPE and generate the stimulus file for

characterization. The stimulus file contains input patterns that can traverse each edge in the corresponding STGPE. The SPICE netlist with distinct capacitance for each interconnection layer is extracted from the cell layout by using OPUS layout parasitic extractor. The transistor models used are the level 3 model of 0.8um SPDM CMOS technology provided by CIC (Chip Implementation Center in Taiwan).

In the flow, "SR_CL Setup" is used to set different input slew rates and output loadings for the characterized gate. We run three different SPICE simulations for the characterizations of power, timing, and input capacitances. After running the power characterization, we obtain the power consumption of each edge in the STGPE for different input slew-rates and output loadings. The power consumption data would be divided into three parts: capacitive feedthrough power, short-circuit power and dynamic power. Details of the characterization of the three power components are shown in [11].

In the timing characterization, we can obtain the information of the rising, falling and propagation time of the cell. Without loss of generality, we use the NAND3 gate shown in Fig. 5 to illustrate the method of getting these transient values. In the NAND3 schematic, we choose an input node that is farthest from the output node to be the evaluated input. The other input nodes are connected to Vdd such that the output function can be controlled by the evaluated input node. To examine the effects of the output loading and input slew-rate, we add two adjustable capacitors in both output node and input node. Rising (falling) time is measured from the time of output signal changing from 10% (90%) Vdd to 90% (10%) Vdd. The propagation delay time from high to low (low to high) is measured from the time between the 50% point of input waveform that changes from low to high (high to low) and the 50% point of output waveform that changes from high to low (low to high).

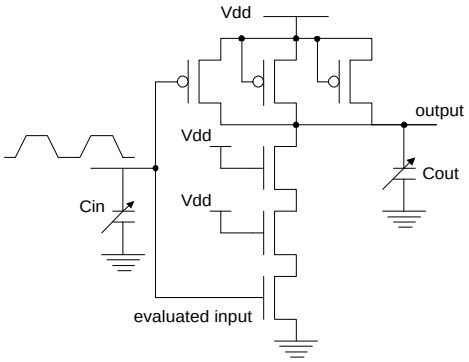


Fig. 5 The method of measuring the transient time of NAND3.

The method of measuring the equivalent input capacitance is shown in Fig. 6. As shown in Fig. 6, we add a current meter, I_m, to the evaluated input, input *A*, of the NAND2 and another current meter, I_n, in the front of the adjustable capacitance, C_{equiv}. The second input, input *B*, is connected to Vdd. We add input patterns to the buffer and adjust the C_{equiv} until the average currents measured from I_m and I_n have the same values or the difference of them is within a user-specified value. Obviously, if we connect input *B* to ground, we will have a different C_{equiv} because the voltage drop between the parasitic capacitances is changed. In our approach, we take the average of the two different C_{equiv} as the equivalent input capacitance of input *A*. Similarly, we can find the input capacitance of the input *B*.

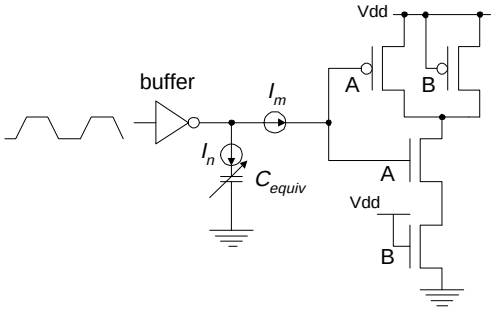


Fig. 6 The method of measuring the equivalent input capacitance.

After running power and timing characterization, we fit the characterization data into some empirical formulas by using a tool *Mathematica*. We fit the timing data into linear equations that are function of output loading. In our experiments, we find that the capacitive feedthrough power is almost independent on the input slew rate and output loading, the dynamic power is dependent on the output loading, and the short-circuit power is mainly dependent on the input slew rate and lightly dependent on the output loading. Thus we fit the power characterization data into the following equations.

$$W_{feedthrough} = \quad _{00}, \tag{3}$$

$$W_{dynamic} = \quad _{00} + \quad _{01} \quad C_L + \quad _{02} \quad C_L^2 + \quad _{03} \quad C_L^3, \tag{4}$$

$$W_{short\text{-}circuit} = \quad _{00} + \quad _{01} \quad C_L + \quad _{10} \quad SR + \quad _{11} \quad SR \quad C_L + \quad _{02} \quad C_L^2 + \quad _{20} \quad SR^2 + \quad _{12} \quad SR \quad C_L^2 + \quad _{21} \quad SR^2 \quad C_L + \quad _{22} \quad SR^2 \quad C_L^2, \tag{5}$$

where C_L is the output loading and SR is the input slew rate and all the coefficients are constant. Finally, these power consumption equations, delay equations and the equivalent input capacitance would be stored in the database, which will be used during power estimation.

IV. Power Estimation System in CB-Power

To design a chip, the circuit designers will run a large number of logic simulations such as VHDL or Verilog simulations to verify the circuit function. In general, the input patterns applied are the possible patterns which may occur in real chip operation. Therefore, we can utilize those simulation data to estimate the power consumption of the chip.

As mentioned before, CB-Power uses CBPE to estimate the power consumption of a circuit. Therefore, we want to link the CBPE with Verilog in our environment. In other words, we hope that the CBPE can estimate the power consumption of a circuit written as a Verilog file.

```
module testmodule;
    reg x1, x2, x3,x4, x5;
        T_nand21_0   g1(x249, x1, x3);
        T_nand21_0   g2(x246, x3, x4);
        T_nand21_0   g3(x253,x246,x2 );
        T_nand21_0   g4(x6, x249, x253);
        T_nand21_0   g5(x251, x246, x5);
        T_nand21_0   g6(x7, x251, x253);
    initial begin
        $P_D_CAL(testmodule,5);
      x1=0;  x2=0;  x3=0;  x4=0;  x5=0;
        #100  x1= 0;     x2= 0;     x3= 0;     x4= 0;     x5= 0;
        #100  x1= 1;     x2= 1;     x3= 1;     x4= 0;     x5= 0;
                                .
                                .
                                .
                                .
        #100  x1= 1;     x2= 1;     x3= 1;     x4= 1;     x5= 1;
        $power_estimation(testmodule);
        #50 $finish;
    end
endmodule
```

evaluated module

input number

Fig. 7 An example of Verilog file with power estimation function.

We have implemented the CBPE in C functions and made the functions as two system tasks, $P_D_CAL() and $power_estimation(), for logic simulation by using the Programming Language Interface (PLI) of Verilog-XL. Fig. 7 shows the Verilog file of benchmark circuit C17 that performs the power estimation function.

In Fig. 7, the system task $P_D_CAL() uses PLI's access routines to get the information of delay and input capacitance from the database and then calculates the output loading and input slew rate of each cell in the circuit. It also calculates the propagation delay of each gate and writes them into the data structure of Verilog for logic simulation. During logic simulation, $P_D_CAL() monitors the signal transitions of each node in the circuit and finally calculates the signal probabilities (P) and transition densities (D) of all nodes in the circuit. Following, Verilog executes the second system task $power_estimation() to estimate the power consumption of each gate individually.

For a logic gate, $power_estimation() first calculates the energies of each edge in the corresponding STGPE by using the power, timing equations in database and the information of output loading and input slew rate obtained by $P_D_CAL(). Then, based on the input signal probabilities and transition densities, $power_estimation() calculates the edge activity number of each edge [1]. Finally, it reports the power consumption of the whole circuit and the three power components of each gate in the circuit.

V. Hierarchical Power Estimation

While the components contained in integrated circuits are growing rapidly, it is very important to consider the regularity, modularity and hierarchy in circuit designs. A circuit designed with modules would be more interested than that composed of primitive gates only, because its functionality is much easier to understand.

Most macrocells such as DFFs, latches, adders and multipliers are composed by basic, complex and transmission gates. Therefore, in our approach, we decompose a macrocell into the primitive gates when the power consumption of the macrocell is estimated. For example, Fig. 8 shows a D-type flip-flop with setB and reset. This D-type flip-flop is composed of 4 inverters, 2 AOI22 gates and 2 AOI12 gates. In CB-Power, each such DFF module in the Verilog description would be transformed into 4 inverters, 2 AOI22 gates and 2 AOI12 gates during power estimation. Using this hierarchical approach, we can estimate the power consumption of a macrocell by summing up the power consumption of the primitive gates which constitute the macrocell.

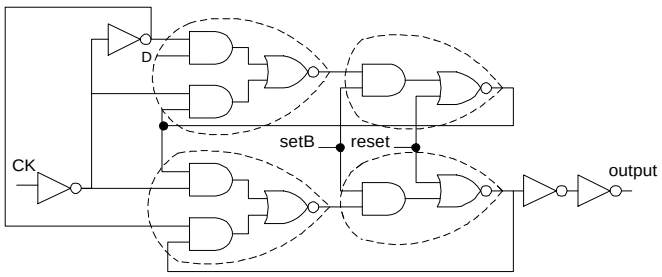


Fig. 8 A D-type flip-flop composed of 4 inverters and 4 AOI gates.

VI. Experimental Results

CB-Power has been implemented in C on a SUN SPARC station 20 with 64 Mbytes of memory. We performed experiments by using the MCNC benchmark

suits. The signal probabilities and transition densities of the primary inputs are assigned to be 0.5 for all circuits. Based on the input characteristics, a random signal generator generates 1000 patterns with 10ns clock cycle time for both SPICE and Verilog simulators. The cell library used involves the 2-to-4 inputs NAND and NOR gates and 5 AOI gates and 5 OAI gates.

Table 1 reports the exact SPICE simulation results and CB-Power simulation results of some sequential circuits. The D flip-flops used in these sequential circuits are shown in Fig. 8. In the experiments, the power consumption due to hazards should be discounted. This is because the transitions due to hazard are regarded as a complete charging or discharging in our system. However, from the exact SPICE simulation results, we observe that the output waveform due to hazard does not make a full execution. Therefore, the power consumption contributed by hazards should be discounted in CB-Power. For simplicity, we assume that the power is discounted by 50%. Experimental results show that the power estimation based on CB-Power provides 5.15% error of SPICE estimation on average while the CPU time spent is more than two orders of magnitude less. In fact, the Verilog simulation consumes over 95% of CPU time in CB-Power.

VII. Conclusion and Future Works

In this paper, we present CB-Power, a hierarchical cell-based power characterization and estimation environment for static CMOS circuits. CB-Power can deal with the circuits composed of basic gate, complex gate, transmission gate, and macrocell. During power estimation, CB-Power decompose the macrocells into some primitive gates and then estimates the power consumption of the primitive gates directly. Therefore, CB-power is a hierarchical power estimator. In CB-Power, the power consumption of a cell is divided into three power components: capacitive feedthrough power, short-circuit power and dynamic power. CB-Power reports not only the average power of a circuit but also the three power components for each gate. These information would be very useful for a short-circuit power driven or dynamic power driven power optimization.

The accuracy of cell-based power analysis depends not only on the accuracy of power modeling and characterization but also the accuracy of the switching activity estimation. In simulation based approach, the accuracy of switching activity estimation is strongly dependent on what input patterns and how many patterns are applied. In the future, this problem needs considerable research efforts.

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Table 1. Estimation results for a subset of MCNC sequential benchmark circuits.

Circuits	Ins.	Outs.	Trs.	Gates	DFFs	Power (uw)		CPU time(sec.)		Error
						SPICE	CB-Power	SPICE	CB-Power	
opus	5	6	396	63	4	6547	6688	15224	34.9	2.15%
train4	2	1	118	15	2	1937	1890	3550	13.8	2.43%
train11	2	1	292	37	4	4113	4039	9488	25.1	1.8%
mc	3	5	168	27	2	2604	2683	5764	16.6	3.03%
ex3	2	2	368	56	4	7991	7897	16600	34.6	1.18%
ex5	2	2	290	44	3	4527	4436	9567	24.5	2.01%
ex6	5	8	410	71	3	6794	7032	16847	35.1	3.5%
bbtas	2	2	206	23	3	2984	3406	6774	18.7	14.14%
dk512	1	3	334	44	4	6362	7416	12323	31.6	16.57%
Average Error										5.15%