A Rapid Prototyping Method for Top-down Design of System-on-Chip Devices Using LPGAs

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Abstract

This paper proposes two methods for a rapid prototyping of top-down System-on-Chip(SOC) design using laser programmable gate arrays (LPGAs).

The first one is a design flow of SOC consisting of four steps: concept-making, virtual-world prototyping, synthesis, and real-world prototyping. The steps can be undertaken individually or in tandem and provisional product models are transformed from upper stream (concept-making) to lower stream (synthesis) either automatically or semi-automatically. This method differs from ordinary rapid prototyping methods in that design evaluation is shifted more upper stream. The SOC device is manufactured early; The steps follow concept-making, virtual-world prototyping, synthesis and real-world prototyping(In the ordinary case, from real-world prototyping to synthesis) . This method allows the device to be evaluated in the actual operating environment.

The second method we propose is based on LPGAs and use of a real-time production fabrication system (RPFS). With these design methods and environment, we can get a shortest time to market which offers exciting audio and video capabilities while giving designers the flexibility they need to rapidly produce innovative and creative products. This paper describes on the application of these methods to develop video signal processors for LCD projectors, demonstrating their efficiency for design tuning and performance optimization.

I. INTRODUCTION

In recent advances of electronic equipment, particularly multimedia technology, the development of SOC[1] technologies have led to integration of video, audio, information processing and communication functions, with advances in Application Specific Integrated Circuits(ASICs) and microprocessors, and with the effect of intensifying competition in an already competitive market[2]. The move to SOC involves design of entire systems in which some or all of the major functions are, as fast as possible, embodied in a single silicon chip using large-scale integration(LSI). The market is demanding (1) methods to shorten SOC development time from the current four to eight weeks to two weeks or less, and (2) a development environment that gives

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designers full control of the design process with the flexibility they need to develop high value-added SOCs. For the first demanding , Field Programmable Gate Arrays(FPGAs)[3] have met need for rapid development, allowing devices to be manufactured in a matter of days, but for mass production, a separate process is required. And for the second demanding, advances in EDA(Electronic Design Automation) tools and simulation technology[4, 5, 6, 7] have gradually pushed system design evaluation from production towards upper stream, but further advances are awaiting development of new design processes.

The demand is for an approach that integrates both creative and production prototyping, and in which rapid creative prototyping leads naturally and easily into production prototyping.

This paper proposes a rapid prototyping method for top down design of system-on-chip devices that addresses these issues by use of an integrated production process that reduces the lead time from prototype production to trial or mass production, and use of LPGA-based device technology that makes engineering prototypes comparable to final production devices available in 1 to 5 days.

Specifically:

(1) The SOC top-down design can be divided into two stages, the upper stream portion from the concept to the virtual-world environment, and the real-world environment. These are further subdivided into concept making and virtual-world prototyping, and synthesis and real-world prototyping, respectively. Conventional methods have used FPGAs to perform real-world evaluation of proposed devices, then followed the synthesis needed to unify the logic in order to produce an SOC device. This method is the exact opposite: the design evaluation phase is shifted even further upper stream. The SOC device (LPGA) is fabricated rapidly and the product evaluated in the real-world prototyping environment, creating a sequence of design steps that flows from virtual-world prototyping to synthesis, then to real-world prototyping with the role of each step clarified. We propose a top down SOC design method that offers continuous updating for each stage. The real-world environment is one that corresponds closely with the actual environment, with the actual inputs applied to a chip of the final product, with power consumption and operating voltage close to actual values and at the intended operating frequency. This means providing an environment that enables, as fast as possible, those subjective judgments of personal preferences inherent in the development of multimedia equipment, and thus facilitating their effective development and reducing the development time.

(2) We propose use of LPGAs for SOC prototyping, which we can select the development process from trial production to mass production, and use of RPFS. LPGAs offers advantages of rapid design using the same methods used for FPGAs, low costs, and being easily transferred to prototype and mass production. The RPFS provides real-time design data transfer between the designer and LPGA manufacturer that minimizes time requirements associated with design data transfer.

Like conventional CMOS(Complementary Metal-Oxide-Silicon) gate arrays, LPGAs[8] consist of two levels of metalization. All possible connections are made for both the first and second layers. Unnecessary connections are laser cut by a laser cutting machine, with the remaining connections forming the circuit. A 40,000 gate scale LPGA can be cut in a single day, giving these devices the name "one day gate arrays." Because the same CMOS process is used for the prototype and the production device.

Because simulation, the actual environment and the semiconductor (SOC) production are unified, rapid prototyping is smoothly followed by to small-scale, medium-scale and large-scale production.

The authors have employed this method in three design applications, and demonstrated that it results in shorter development cycles with enhanced product quality. The second chapter of this paper describes on the system development background and analyzes development issues. The third chapter describes top down design and LPGA development methods. The fourth chapter introduces applications used to test the method. The fifth chapter offers discussion on the proposed method.

II. BACKGROUNDS OF THE PROPOSAL AND TECHNOLOGY ISSUES

A. Backgrounds of The Proposal

A.1. Improvements in Time to Prototype Production

Device developers in the competitive multimedia market are under intense market pressure to provide early samples of new products. Conventional gate array devices, which are available on relatively short lead times, take 30 to 52 days on average between net list submission and device delivery. FPGA require 7 to 14 days before production can begin. If a device is evaluated in FPGA and mass produced in CMOS, process differences require an additional simulation step. FPGAs operate three to four times slower than CMOS gate arrays, requiring a final real-world evaluation process when the first CMOS gate array samples are produced. Further, four to ten FPGA devices are required for a system, making it impossible to fabricate an equipment prototype to the planned dimensions of the final product. Demand is therefore strong for a rapid prototyping technology that links simulation to small-scale production, medium-scale production and large-scale production. LPGAs support these capabilities: they are relatively inexpensive, samples can be produced as soon as the design is complete, and nearly final devices are available for evaluation.

A.2. Upper Stream and Lower Stream of Design

The complexity of semiconductor design facilities, the specialization of technology expertise, and the high cost of device development have led to development of rapid prototyping methods whose steps consist of correct device specifications, device testing in simulation, real-world prototyping for functional qualification, and finally logic synthesis. Availability of LPGAs that can be manufactured within a day at low cost gives LPGA-based devices an outstanding time-to-market value. As a result, other device-development technologies are being reviewed from the

standpoint of accommodation to change. FPGA qualification processes are gradually being supplanted by processes using improved EDA tools [11]and high-performance simulations to qualify devices in a virtual-world environment. Human visual and auditory characteristics and be modeled, and product characteristics can be evaluated in advance for their appeal or otherwise to human users, enabling basic circuitry to evaluated in a virtual-world. When it is necessary to develop a series of similar devices, LPGAs make it possible to vary specific parameters and produce each device for testing in real-world equipment. In this way, there is demand for product design environments that support broad, progressive design concepts and give designers a wide latitude to exercise their creativity through a number of LPGA design iterations. The functions that can, and cannot, be evaluated in virtual-world and real-world environments are shown in Table I.

TABLE I
Functions Checked in Virtual- and Real-World Environments

Step	Virtual-World	Real-World
A	*Time independent functions *Some of the functions inferred from humann characteristics *Critical path *Number of gates *Max./min./typ. operating speeds *Location of logic errors	*Human sensibilities Display: presence Spartiality: naturealness, three-dimensionality Time: disconfort,fatigue Space-time: impact *Performance:throughput *Features: regular processing system positioning *Measurement:heat dissipation power consumption corresponding to that of actual device *Observation of I/O waveform
B	*Human sensibilities *Measurement,heat dissipation and power consumption	*Location of logic errors with LPGA devices is either impossible or time consuming

A:Functions that can be checked
B:Functions that cannot be checked

A.3. Operating Frequency

Much recent multimedia equipment employs embedded display systems. Ordinary equipment had only to manage video or converted RGB signals, for which operating frequencies of 4.2 to 16.8MHz were adequate. Higher quality signal standards such as VGA and XGA require device operating frequencies of 20 to 50MHz, or even above 80MHz . The FPGAs have been widely used for rapid prototyping of display processors, offering maximum advantage on scales of 10 to 20 kilogates with operating frequencies of 5 to 15MHz. And many design iterations are needed to perform logic mapping to accommodate a toggle frequency ceiling[9] and FPGAs are subject to ground bounce when operating in the 30MHz region that can delay testing of prototype devices[10]. Therefore, devices and methods suitable for rapid prototyping of 20 to 50MHz devices are needed and expected.

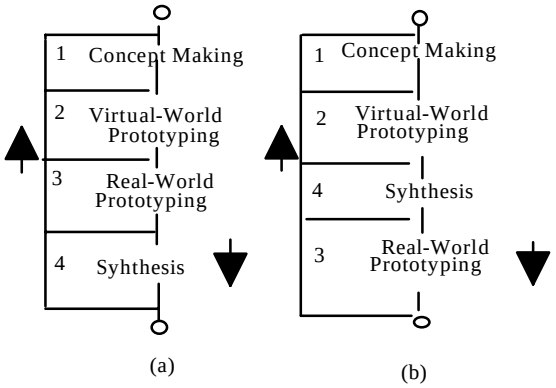

Fig.1 The Process of A Rapidprototyping Method of Topdown Design
(a) The ordinary process
(b) The proposed process

B. TechnologyIssues

The following technology issues must be addressed before we can overcome the limitations of current technology detailed above:

1. Rapid prototyping methods that generate device constructions (design)
2. LPGA design for 20 to 50MHz operating frequencies (design, production)
3. Selection of LPGA methods to suit production scale and information transfer between design and production systems that supports short turnaround times (design-to-production)
4. Making continuity and congruity between virtual and real-world environments (design-to-production)
5. Shortened simulation and emulation times (design, production)

Regarding point (1), a primary consideration in the design of the rapid prototyping method is that backtracking to an earlier step in the design process should be possible at any point. In a conventional and ordinary design process such as FPGA shown in Fig. 1(a), the process proceeds from steps 1 to 4, whereas when LPGA is used (Fig. 1(b)) system qualification follows LPGA prototype production so that steps proceed in the order 1-2-4 or 2-4. As a result, the virtual-world environment used in LPGA development must be capable of accurately verifying system functionality and performance.

Regarding point (2), the LPGA is laid out like the grid-pattern of the metal pattern. The array structure groups together larger units and is well suited to the design of synchronized circuits. It is therefore important to choose a design method and tools able to take advantage of this. Since the sample LPGA is fabricated early for system qualification, the device operating characteristics must be determined in advance during the product design stage. It is desirable to perform simulation and qualification to ensure that the device logic meets maximum and minimum values, and that typical operating speeds and delay times are suitable over 20 to

50MHz operating frequencies, and it is essential to provide the vendor with a test vector to accompany the net list. It is therefore preferable that LPGA vendor and client register a library of LPGA device characteristics in the design tool prior to specific device design.

Regarding point (3), LPGAs are configured so that devices and systems are suited to small, medium and large-scale production, allowing scale to be selected to suit the product concept. Although the LPGA device itself can be fabricated in just one day, the advantages of LPGA technology are not fully available using the same task distribution and data management flow used for conventional gate arrays. It is desirable to avoid duplication of effort by the LPGA designer and manufacturer, and accuracy should not be sacrificed. Design data transfer should be automated as fast as possible. For example, a smooth simulation is required for system qualification and device changing when transitioning from small to large-scale production. Preparing a test vector consisting of a set of I/O points and I/O test data is also important.

Regarding point (4), the model and data created within the virtual-world environment are often expressed in a diversity of formats, procedures and languages, so many issues revolve around communicating this information to the real-world environment accurately, automatically, and in a timely manner.

Regarding point (5), various languages are used for functional verification in the virtual-world environment. Without improvements in simulation methods, the simulation can take an inordinate amount of time. Further, when the simulation is carried out on the emulation side, a great deal of time and trouble is required to handle
equipment startup and loading.

III. A Rapid Prototyping Method for Top-Down Design of System-on-Chip Devices Using LPGAs

A. The Top-Down Design Method for SOC Devices

A.1. Concept-Making

(1) Functions

The intended target is chosen, ideas are created to solve the associated problems, and the best support tools for the particular application field are used to model the idea for qualification, evaluation and testing in order to select several promising solutions out of many possibilities.

(2) Tools and Languages

Solution support tools include a generation purpose numerical processing tool and specialized communication tools. There are also display tools that convert numerical results into charts and graphs to provide visual support for evaluation and decision making processes. C, C++, and special-purpose tool languages are used.

(3) Output

Qualification objects are created for multiple solutions used in subsequent steps as shown in Fig.2.

A.2. Virtual-World Prototyping

The activities in this step are in Fig.3.

(1) Functions

In this step, multiple algorithms representing part or the whole of the system conceived in the previous step are embedded in a model that is simulated at high speed on a workstation or personal computer. Virtual development environment, such as virtual-measuring instruments and virtual-display support give a direct view of the results in the virtual-space as processed signal waveforms, video images, and character strings that can be used for

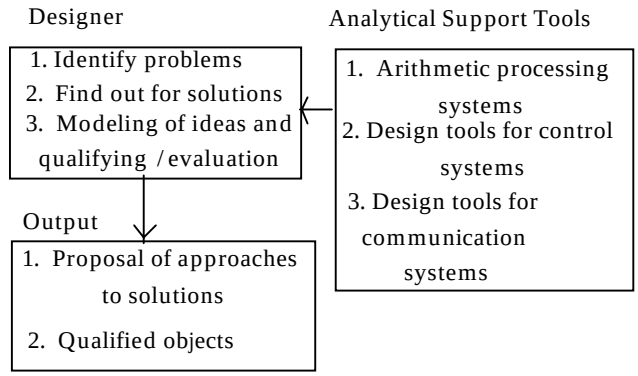

Fig.2 The Concept-Making Step

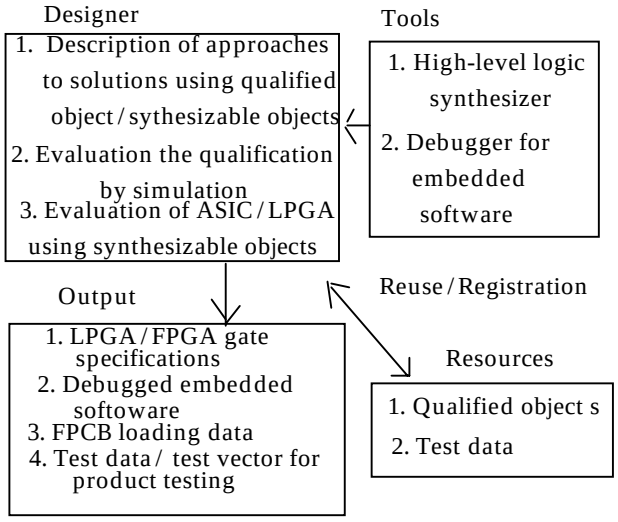

Fig.3 TheVirtual-World Prototyping Step

qualification and evaluation. Once the optimum model is selected, the hardware and software elements representing the system implementation are distributed in the optimum manner. ASIC step count and gate count are projected at this stage based on objects that synthesize the required functions, performance and price.

(2) Tools and Languages

A high speed simulator language executing on a workstation is used to implement multiple algorithms. High-level software description languages are used in the early steps. Later, after a physical model has been selected, a CO-design high-level logic simulator and logic synthesis tool, that combine hardware and software functional description capabilities is used. Another tool is used to output the logic network for LPGA production. An embedded software debugger is used for software debugging.

For abstract descriptions, C and C++ are used, with redefined graphic descriptions hardware/software block diagrams, using automatics or semi-automatic logic conversion into hardware description languages (primarily VHDL(Very high-speed integrated circuit Hardware Description Language)), specification description languages and vendor-specific description languages to perform logic simulation and logic synthesis. In netlist and test-vector generation, EDIF (Electronic Design Interchange Format) using C or vendor-specific format transformations are used . The laser cutting list and one mask checking list output uses a vendor-specific description language.

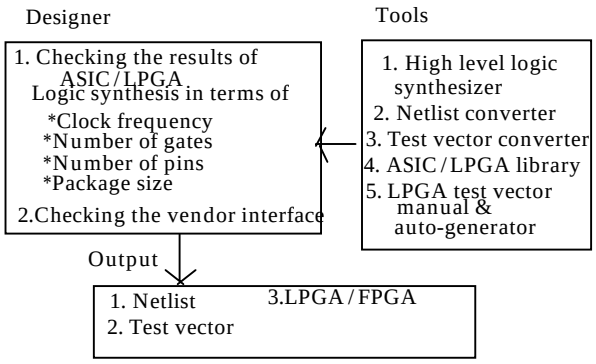

Fig.4 The Synthesis Step

(3) Output

Outputs include SOG (sea of gates), FPGA and LPGA gate specifications, debugged embedded software, test data for product inspection, and PCB(Printed Circuit Board) data. The designer returns to the previous step if satisfactory results are not obtained. To support transitioning to SOC chip production processes, we use automatic or semiautomatic support for conversion from software description languages to VHDL, or other hardware description languages or specification languages.

A.3. Synthesis

The activities in this step are shown in Fig.4.

(1) Functions

In this step, a net list is created for converting the logic circuits qualified in the previous step to an actual device. The netlist may also contain actual device gate numbers, price and other data estimated in the virtual-world prototyping step. Based on the net list data, tradeoffs are made among gate count, pin count, package dimensions and operating frequencies, and the functions and performance of the resulting SOC device are evaluated. The designer returns to previous steps if the results are unsatisfactory and conducts additional evaluation iterations.

(2) Tools and Languages

Tools include a high level logic synthesis tool (synthesizer) that performs logic synthesis and logic simulation and outputs net lists and test data; a net list(netlister) and test data converter for converting between industry standard and ASIC vendor data formats or EDIF(Electronic Design Interchange Format); and vendor-specific CAE tools that output a laser cutting list or laser one-mask etch list. C and C++ and predefined graphic description languages for hardware and software block diagrams are used for abstract descriptions. For functional descriptions, VHDL, and graphic description language for basic hardware and software components are used. And for netlist-converters and test data-converters, c and c++ are used.

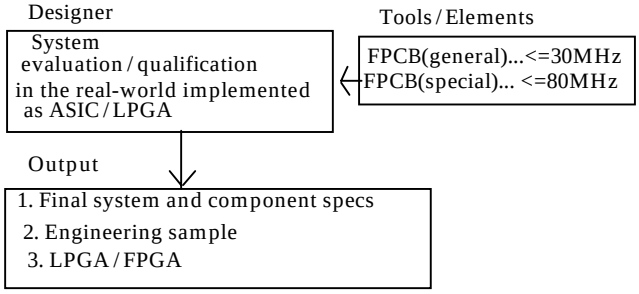

Fig.5 The Real-World Prototyping Step

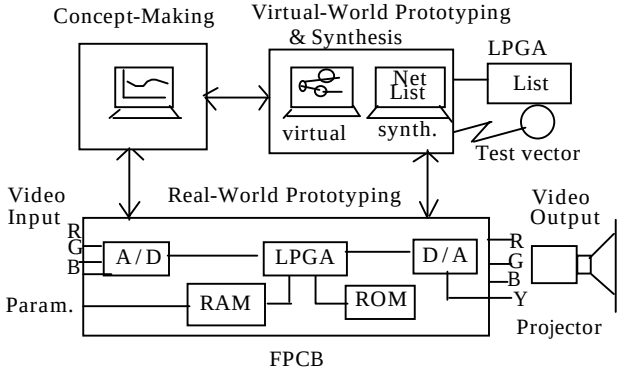

Fig.6 The Application Specific FPCB

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(3) Output

Tool data display outputs include gate count, connection count, critical and logical virtual- interconnection design data, delay timing qualification data, and maximum operating frequency timing qualification data. The final net-list/test-vector output is used in LPGA production. Again,

for mass production, the output of netlists and test vectors enables the selection of other processes.

A.4. Real-World Prototyping

The activities in this step are shown in Fig. 5.

(1) Functions

In this step, the LPGA produced by Synthesis step used to replace the logical circuits developed using simulations in virtual-world prototyping with the software added, and downloaded automatically or semi-automatically to a field programmable circuit board FPCB for a real-world prototyping as shown in Fig.6 and qualification and evaluation are performed in an environment that closely approximates actual operating conditions. This step comprises not only the qualification and evaluation of basic system functions but also provides for those reflecting the personal tastes, preferences and value of systems that are so characteristics of users of multimedia equipment.

(2) Tools and Languages

Tools include a loader that loads logic data to the FPCB, a tool that manages logic distribution and partitioning, and a tool that sets up system wiring for the FPCB. This is not usually necessary for an LPGA, which is a single high-density logic device. A waveform measurement oscilloscope may be used to check EMI, timing and other device characteristics. The loader for the dedicated FPCB is described in C.

(3) Output

After checking and reflecting the personal tastes, preferences, and value of systems ,this step determines final specifications for systems ,components and engineering samples.

B. The LPGA : Real -Time Production Fabrication System

B.1. Special Device Characteristics

Like conventional CMOS gate arrays, LPGAs employ double layer of metalization. All possible connections are made for both the first and second layers. Unnecessary connections are later cut by a laser cutting machine, with the remaining connections forming the circuit. A 40,000 gate scale LPGA can be cut in a single day, giving these devices the name "one day gate arrays." A mass production process that is similar with the LPGA process is used for mass production. The special characteristics of LPGAs include:

- Device process :0.6 to 0.8 micrometer dual-metal single-polysilicon channel-type CMOS
- Capacity :Many capacities from 2 to 250K gates
- Gate utilization efficiency :About 80-90%
- Maximum toggle frequency :About 460-800MHz Max.FF
- Typ. delay time :300ps

The structure and the concept of Laser Cutting of metal lines of LPGAs are shown in Fig.7.

B.2. Scaling LPGA Production

Since LPGAs are fabricated individually by a laser cutting process, small lots are available in a very short time. However a different production process is needed for medium to large production scales involving quantities in the tens to hundreds of thousands. Three production methods are available as shown in Fig.8.

(1) Small-scale production by laser cutting
(2) Medium-scale production by one-mask etching type
(3) Large-scale production by an ASIC process or by using similar process with LPGAs

The laser cutting method processes a die-size array at a rate of about 16,000-20,000 cuts per second, and is suitable for production quantities of 1 to 20 devices. The turnaround time in the United States is about one day. One mask etching produces devices in wafer multiples, with typical production quantities of 1 to 20 wafers. The turnaround time in the United States is seven days. Production is preceded by laser cutting when large production scales are involved.

B.3. Configuration of The Real-Time Production Fabrication System

Although the LPGA device itself can be fabricated in just

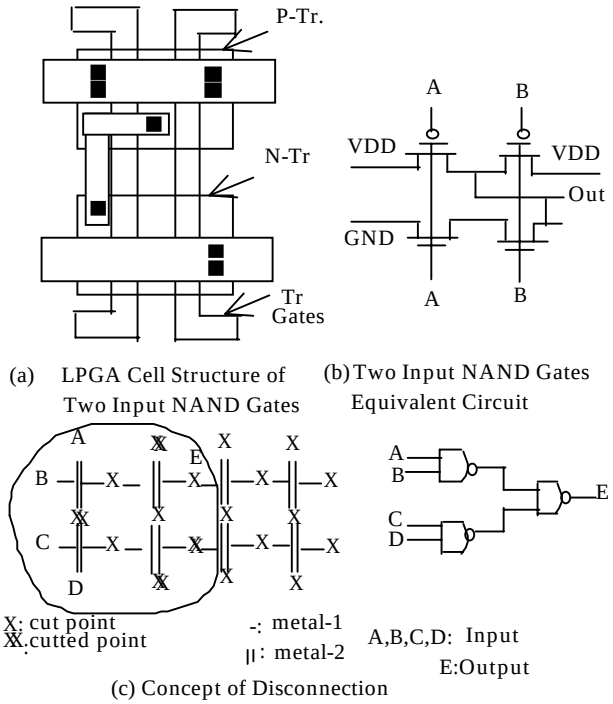

Fig.7 The Concept of Laser Cutting of Metal Lines of LPGAs

one to two days, the advantages of LPGA technology are not fully available using the same task distribution and data management flow used for conventional gate arrays. The basic concepts of the RPFS are: avoiding duplicate efforts by product designers and LPGA manufacturers; rapid and accurate data exchange; data exchange over networks wherever possible.

(1) System Flow (design-production-qualification)

On completion, the upper stream design stages comprising virtual-world prototyping yield net list, test vector, and pin assignment information that is passed to the synthesis step for conversion to LPGA manufacturing data. The LPGA device family, and package type are selected, and small, medium or

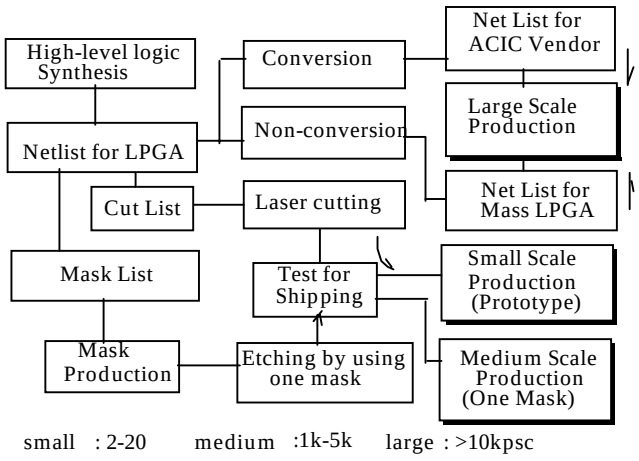

Fig.8 The LPGA Production Process System

large production scales are chosen. Based on this information, LPGA production begins.

The LPGA system consists of: a standard CAE tool used to conduct initial checks of design rule, timing and other characteristics of the received production data; automatic placement and routing tools, and a tool for generating the cutting list or etching mask list for one-mask. The laser cutting process is used for small-lot production (prototype products) and laser one-mask etching(one-mask products) for medium-scale production. For large-scale production the net list for cutting is processed by a standard CAE tool to generate a vendor net list for gate array or cell-based array production or high area reduction die array production witch is similar with LPGAs. After cutting and functional testing are finished, the LPGA production process is complete. The LPGA is then mounted on a dedicated FPCB for evaluation by real-world prototyping.

(2) Logic Simulation and Logic Synthesis

Once the desired LPGA device family is selected, device library and cells are registered, and logic qualification and net list generation are conducted in accordance with the design rule. Cell registration requires cooperation from and a contract with the LPGA vendor. Gate count, connection count, critical and logical virtual-interconnection design data, delay timing qualification data, and maximum operating frequency timing qualification data are verified prior to this step. The output of this step is the exchange data detailed above.

(3) Automatic Test Vector Generation

Since multimedia equipment inherently processes large amounts of video and audio data, a large amount of test data is also required. The test vector is automatically generated during logic simulation and logic synthesis. Data generated by data logging during the simulation is filled out with pin data and control constants, the simulation is repeated and output is captured. The input and output data is labeled, edited and converted automatically to the vendor's format as the test vector.

(4) Net List Converter and Test Vector Converter

Tools are created for data exchange between designer and manufacturer in industry standard formats such as EDIF and vendor data formats. These tools are necessary to support the high volume of data exchange associated with negotiations regarding price, chip size, quotations on incorporating additional features, etc.

(5) Establishing a Design Data Exchange Network

A network is used to exchange the LPGA production data.

IV. Applications to Actual Systems Used to Test the Proposed Method

A. *Small-Scale Production of Signal Processor System (A)*

(1) Purpose

Several algorithms may be used to convert any VGA standard RGB video signals from a personal computer into separate [NTSC] luminance and chroma signals.

TABLE II

SOC Top-Down Design Methods / Adopted LPGA Systems

	Adopted Systems	Design Time unit: day a	b	c	d	sum	Number of gates K	LPGA pieces	frequency MHz	note
1	Image Pro-cessing A	25	10	7	3	45	40	4x1	30	1 st LPGA
		25	10	14	10	59		4x1		FPGA
		2	1	7	1	11		4x2		2nd LPGA
2	B	20	15	7	15	57	30	4x1	30	1st LPGA
		4	4	21	10	39		1x1		2nd LPGA
3	C	20	15	10	10	55	20	1x1	50	1st LPGA
		10	20	30	15	75	90	1xm		2nd Cell

a: Concept-Making b: Virtual-World Prototyping
c: Synthesis d: Real-World Prototyping
m: mass number

The purpose of this project was to implement a number of signal processing algorithms as LPGA devices and provide them to experts for evaluation. VGA signals require a minimum device operating frequency of 31.5MHz. Each processing algorithm was to be implemented as a single LPGA, and the total production volume was several devices.

(2) Design Environment and Process

Fig.6 shows the dedicated FPCB we used for this system. The development environment is organized to allow rapid improvements in the flow from idea to logic and algorithms, actual circuit, and trial. The FPCB consists of analogue to digital converter units(ADC), control I/O units, an LPGA and digital to analogue converter units(DAC). During the concept making phase, the relationship between the RGB and luminance signals is elucidated using a numerical processing

tool, and during the virtual-world prototyping phase, C language is used to implement these findings as algorithms and video images were simulated. A workstation is used to perform ideal virtual-color reproduction free from the losses associated with physical optics. The workstation screen images are evaluated by engineers in the project, and the algorithm is improved. The C algorithm is converted to a basic component of a high-level logic description tool and to a block diagram objects to support co-design processes. Recompiling the code makes it possible to naturally transition from software description language to hardware description language.

The hardware description language is then used to simulate the screen, and if the screen is identical, the software-to-hardware conversion is judged successful. Next, at the synthesis stage, a net list is generated and supplied to the vendor company, which uses laser cutting to produce an LPGA within a week. Finally, in real-world prototyping, the LPGA is mounted in the FPCB and tested. If the image quality is identical to the original screen simulation, the implementation is judged successful. Several LPGAs are fabricated in this way, each implementing different algorithms.

(3) Results

Approximately two weeks were required at concept making phase to create the basic logic to support the initial idea. Following this, one month and three development iterations were required to develop improved liquid crystal projector equipment using these devices. Three types of projectors were developed in a month. All three devices demonstrated no errors in logic or manufacturing, and all the prototypes passed one week of accelerated aging at 50C. Details are listed in Table II.

B. Medium-Scale Production of Video Signal Processor System (B)

(1) Purpose

The rapid prototyping method was applied to developing picture quality controls for each monitor in a multiscreen display system. The operating frequency requirement was identical to that of the example in section 4.1. A one-mask etching process was used to test produce 20 chipsets of four devices, each consisting of some 30K gates

(2) Design Environment and Process

We used the same environment as described in section 4.1. Since we had many interfaces to external control, in the final stage FPCB was mounted on the system board. The development process was generally as described in section 4.1, but since the quantity involved makes failure of the project prohibitively expensive, the algorithm developed in the previous project was reused as far as possible, and a single set of four devices was fabricated by one-mask etching and tested prior to medium-scale production of 20 chipsets by the same process.

(3) Results

Both the first run of one chipset and the second run of 20 chipsets passed testing. In total, 84 devices were fabricated without a single failure. Table 2 lists details.

C. Large-Scale Production of Video Signal Processor System (C)

(1) Purpose

This project evaluates the picture quality benefits if the pixel count of current liquid-crystal projectors is doubled, and evaluates the additional cost of the internal memory and random logic under mass production. The device operating frequency is 50MHz, and standard cells were used for mass production.

(2) Design Environment and Process

This system requires the LPGA development environment and a conventional standard-cell mass-production environment. In the LPGA environment, an FPCB is used for trials during LPGA prototyping as described in section 4.1, and after the LPGA is approved, the design process transitions to the standard-cell environment. A production PCB is used for testing in the mass production phase. A high level synthesis tools are used to manage algorithm and functional changes, and logic compression.

Qualifying the picture quality control circuits was a primary consideration in the LPGA development environment, so substantial time was invested in verifying picture quality using the high level synthesis tool on a workstation. After the LPGA was qualified, it was mounted on the FPCB for projection testing, and nearly all system functions were tested and verified. The first steps of mass production were cost optimization decisions related to cell series selection, package selection, internal memory capacity, and absorption of specification changes. This required use of the high level synthesis tools and optimization tools from each vendor for purposes such as design checking and logic compression, and a net list format conversion utility (Netlister, which we developed for the application.) At the end of the process the net list format was converted and supplied to the cell vendor. The LSI was then manufactured, mounted and tested.

(3) Results

As Table 2 shows, the first LPGA process was conducted on a 20K gate scale, but the memory capacity of the cell-based devices was boosted by 90K gate. The LPGA development process was nearly identical to that described in section 4.2. The cell-based development process required about two months. The Netlister utility provided reversible conversion between net list formats that supported the final cost performance tradeoff decisions made in consultation with the various vendors involved. Performance and cost goals were ultimately satisfied.

V. DISCUSSIONS

A. Regarding Top-Down Design of SOC Devices

(1) Design Flow: Synthesis to Real-World Prototyping

Virtual-world prototyping was shown to provide adequate functional qualification, while real-world prototyping makes it possible to address user interaction and preference of human issues in a real-world environment early in the development cycle. Since real world prototyping is prohibitively costly and time-consuming under previous LSI technologies, the design flow continues from virtual --> real --> LSI synthesis in the

final step. But with LPGA technology making LSIs available early in the design cycle, a flow of virtual --> synthesis --> LSI prototype --> real becomes possible, and Table 2 shows the advantages of this organization. In example A, these steps took ten, three and seven days, (20 days in total) out of 45 days required for the entire process through the first iteration, then one, one and seven days out of total of 11 days required for the second iteration, a 50% reduction. When the final seven-day step abroad is replaced by two days inside Japan, only four days--one fifth of the time--is required. This shows that the new process is highly advantageous for LPGA production.

(2) Reduction of Design Time and Quality

As table 2 shows, concept-making required an average of 20 days, and the time requirements tended to diminish as the design process flowed lower stream. Ten to 20 days were required for evaluation in the virtual- world environment. Undertaken in Japan, the time requirements would shorten to three to 13 days. An average of ten days was required to generate the net list, fabricate the LPGA and conduct an evaluation using the FPCB. The fact that LPGA and CMOS devices share the same manufacturing process and development environment has a huge impact on development time. We used the simultaneous circuit design tools for the examples presented in this study, which allowed rapid simulation and yielded error-free LPGA designs, and not a single damaged device in a major contribution to design quality. The division of the design flow into four clearly delineated steps with free transitioning backward and forward provides tremendous advantages in a rapid prototyping approach to top-down SOC design.

(3) Intercompatibility and Congruency

As described in section 2.2, compatibility between interconnected objects makes design data transfer between them automatic or semiautomatic, which serves to accelerate the design and test iterations by which engineers optimize the specifications, look, feel and function of new designs. The compatibility of interconnected models and tools often turns out to support the integration of new procedures and formats as they are developed. We had to develop format conversions for the examples presented here, particularly for the mass production example, and the lack of this intercompatibility caused a time loss of about a week.

B. LPGA Application Systems

(1) Scale and Development Time

The system was applied to development of small, medium and large production scales, and the following characteristics were observed. In the first iteration of developing an idea, 1.5 to 2 months were required regardless of the final production scale with concept making accounting for about 20 days of this time. In the second and subsequent iterations, the iteration time dropped to one half or even one third of the previous iteration time. The development period increases by a factor of about 1.4 times when moving from LPGA to a cell-based process. We believe that further savings of the time taken by system evaluation using real time control in the real-world prettying and a continuous CMOS process using LPGAs would also be possible , although we did not collect data to support this hypothesis. Table 2 suggests that we could expect a 10 to 20 day maximum savings in the first real- world environment time.

(2) Comparison with FPGA

We can describe on a comparison between LPGA and FPGA development for a small system such as shown in Fig.9. The FPGA equipment took 24 days to develop(real+synthesis process), compared to ten days for identical equipment developed in LPGA. The chief reason for the difference is the time associated with logic division and wiring requirement tradeoffs that are required when FPGA is used for high-speed logic.

(3) Comparison with Conventional Gate Array

The data for the development projects presented here shows the number of days required for each step of the project from concept-making to completion. The contrasts between LPGA and conventional gate-array based development are especially apparent from the synthesis phase lower stream. The conventional gate array based development process requires 52 days to complete: seven days for simulation, seven days for layout, 14 days for layout simulation, three days for mask production, 14 days for the two-layer wafer process, seven days for packaging and shipping. If synthesis and processing for LPGAs require seven to ten days, the savings is a factor of 8 to 10.

VI. CONCLUSION

The authors have proposed a rapid prototyping method for top-down design of SOC devices using LPGAs, and employed this method in three design applications, and demonstrated. The result shows that it is in shorter development cycles with enhanced product quality, particularly for devices scaled at 4 to 200k gates and operating 20 to 50MHz, giving development times of one to two weeks, and with an efficient migration path to semiconductor production processes from small to large scale. Three- to ten-day savings in gate-array development times, with development times as short as one day by LPGAs, are especially significant.

In addition, this single technology supports much of current multimedia equipment development, meeting performance and accelerated development needs while satisfying requirements for painstaking review of physical design and user interaction through hardware prototyping support. But many advanced methods of design implementations using rapidprototyping devices have been developed, it must be taken special care of the strategy of selecting devices to make maximal profit.

This paper has presented a method of dividing top down SOC design into four steps covering idea development to production, with seamless integration of design iterations through enhanced connectivity and compatibility among the tools that constitute the development environment. Some problems, however remain to be solved.

(1) Automated transition from abstract representation to concrete representation
(2) Cooperative design with embedded software
(3) Optimized boundaries between hardware and

software

(4) Optimized tradeoffs between chip cost and production process

(5) Establishing infrastructure for even faster SOC development

The authors plan to continue research on solviing these issues and realizing further performance improvements and development time reductions.

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REFERENCES

[1] Latest ASIC Design Technology '94 "System-On- Silicon Implements Equipment for the Multimedia Age", Nikkei BP -sha, 1993, pp.26~30.(in Japanese)

[2] Kikuchi Minoru, " Information Media White Paper 1994 ",Kabushiki Kaisha Dentsu Soken, pp.3~10.(in Japanese)

[3] MP-3 / MP-4 Reference Manual. APTIX, 1996

[4] Hisao Koizumi, Katsuhiko Seo, Fumio Suzuki, Yoshisuke Ohtsuru, Hiroto Yasuura "A Proposal for a Co-Design Method in Control Systems Using Combination of Models", IEICE Transactions on Information and Systems, E78-D (1995), 3, pp.237~247.

[5] W.Bruce Culbertson, T.Osame, Y.Ohtsuru, J.Barry Shackleford and M.Tanaka "The HP Tsutsuji Logic Synthesis System", HP Journal, 44 (1994), 4, pp.38~51.

[6] Express V-HDL Reference Manual, i-Logix, 1995

[7] James H. Aylor, Barry W. Johnson "ADEPT WORKSHIP (Day 1 (July 12)) Overview", University of Virginia, 1993, pp.1~60.

[8] Technical Report, Reprinted from the March 1993 edition of SOLID STATE TECHNOLOGY, copyright 1993 by PennWell Publishing Company, Chip Express, 1994

[9] Seuyoshi Toshinori, Ouchi Masahide and Tanaka Ko-ichiro "A practical multi-FPGA Support Environment for Rapid System Prototyping", Third FPGA / PLD Design Conference & Exhibit CMP Japan, 1995, pp.383~392.(in Japanese)

[10] Mikami Kenji, "High-Speed Stable Dynamic Circuits(1) Design Methods" Third FPGA / PLD Design Conference & Exhibit, CMP Japan, 1995, pp.135-181.(in Japanese)

[11] Vps Reference Manual, Zuken Corporation, 1996.(in Japanese)