Static power driven voltage scaling and delay driven buffer sizing in Mixed Swing QuadRail for sub-1V I/O swings

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Abstract

This paper describes and explores the design space of a four power-supply rail methodology (called Mixed Swing QuadRail) for performing low voltage logic in a high threshold voltage CMOS fabrication process. Power and delay trade-offs are studied to suggest approaches for efficient selection of voltage levels and buffer transistor sizes. Posynomial models for QuadRail power and delay are derived to show that at reduced I/O swings (sub-1V), both under- and over-sizing of transistors can lead to steeply increased delays. Transistor sizing techniques are proposed for optimizing delay and energy per logic operation as a function of load capacitance and voltage levels. Experimental results from detailed HSPICE simulations and an And-Or-Invert (AOI222) QuadRail test chip fabricated in the Hewlett-Packard 0.5µm process are presented to support the models and demonstrate significant power reduction compared to static CMOS.

1 Introduction

The fast-growing portable communications industry, driven by the need for performing high throughput DSP and multimedia tasks at low power, has spawned great interest in innovative low power circuit design techniques [1]. Most of these techniques have focused on using standard CMOS logic circuits and lowering the power supply voltage (voltage scaling) [2], because of its quadratic influence on dynamic power consumption. For instance, a recently published low power microprocessor [3] and DSP embedded processor [4] targeted at portable applications operate at power supply voltages significantly below the process-permitted maximum voltages. However, when power supply voltages are scaled below the sum of the threshold voltages of a NMOS and PMOS device ($V_{tn} + |V_{tp}|$), gate delays increase steeply making them a substantial critical path delay contributor. Furthermore, variations in device threshold voltages due to inevitable variations in the IC fabrication process have limited the lowest possible operating voltage to slightly above the larger of V_{tn} or V_{tp} [5]. In a CMOS process with nominal V_t's of 0.75V, this lower bound is about 1V. Random variations in transistor V_t are inversely proportional to $\sqrt{L \cdot W}$, and the constant of proportionality can be as high as 30mV-µm [6]. With rapidly reducing feature sizes, it is obvious these variations are becoming even higher. Reducing nominal V_t's and electronically controlling their variations [7], [2] are possible solutions, but they are both difficult and expensive.

In this paper, we describe the Mixed Swing QuadRail methodology, which addresses maximum possible voltage scaling with little or no reduction in operating speed, in a high threshold voltage CMOS fabrication process. The described architecture requires four power supply rails to be distributed to all circuits sharing this signalling methodology [8], and logic is performed by intermixing high and low swinging voltage signals. The design space of Mixed Swing QuadRail is explored to study the power and delay trade-offs. A static power driven voltage scaling approach is described for selection of high and low swing voltage levels, by evaluating the ratio of off- to on-drive currents for a worst-case on-drive scenario. Posynomial power and delay models for QuadRail are derived to study device sizing tradeoffs and techniques are proposed for efficient transistor sizing to optimize delay and energy per logic operation. Comparisons of our power and delay models to HSPICE simulations using Level 13 BSIM1 models in the Hewlett-Packard CMOS14TB 0.5µm process are performed. Experimental results from detailed HSPICE simulations and an And-Or-Invert (AOI222) QuadRail test chip fabricated in the same process are presented to demonstrate significant power reduction compared to static CMOS.

2 Mixed Swing QuadRail gate architecture

The essence of the Mixed Swing QuadRail methodology, is that it allows the designer to exploit the best aspects of both voltage scaling, and full-swing CMOS. As the name suggests, this requires an additional pair of power supply rails and special low swing drivers. Unlike other low swing transceiver techniques, we propose efficient off-chip low voltage supplies. Dynamic power reduction is obtained by driving loads at reduced voltage swings while performing logic at high swings. For typical digital ICs, the power used to drive interconnect loads can be 50-80% of total power. As feature sizes shrink, this percentage will grow because interconnect capacitance (due to fringing) falls more slowly than gate capacitance (due to active area). Thus the technique will be even more applicable at reduced feature sizes.

Fig. 1 shows a two stage Mixed Swing QuadRail gate, consisting of a logic stage and driver/buffer stage. The buffer stage is a CMOS inverter, with high swinging inputs (Vdd1-Vss1 = V_l) and low swinging outputs (Vdd2-Vss2 = V_b), both centered to maximize noise margins. No DC path exists between the supplies. PMOS devices in both stages are 2.5X wider than the NMOS to equalize rise/fall times. The buffer transistors are ra-

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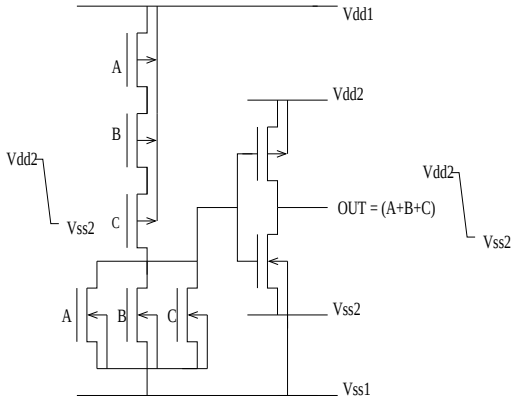


Figure 1: Mixed Swing (two-stage) QuadRail 3-input OR gate.

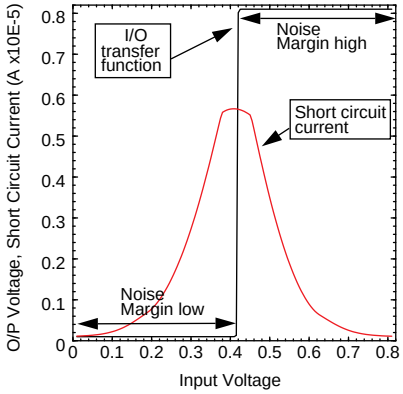


Figure 2: Mixed Swing QuadRail DC transfer chanracteristics.

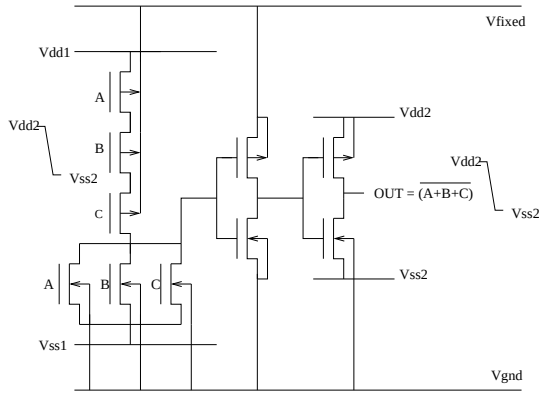


Figure 3: Mixed Swing (three-stage) QuadRail 3-input NOR gate.

tioed by a factor *k* (>=1) relative to logic stage transistors to improve current drive. Each stage has its own N-well in order to minimize body effect. Since the devices are driven by $(V_l + V_b)/2$, switching performance remains good. The ratio of load to driver input capacitance (which in typical ICs is large), sets an upper bound on power savings compared to static CMOS.

The logic stage is identical to a CMOS inverting gate topology, except its inputs have reduced swings. This is tolerable because the transition region in a CMOS gate is smaller than the input range. Noise margins are smaller in absolute terms, but still large compared to some logic families, e.g., ECL. However, care must be taken to control both power supply noise and crosstalk, especially from high swing lines to low swing lines. Both these problems are best addressed by developing CAD tools that can assess these problems and can design to meet noise margin specifications. Noise margins are set by maximum allowable totempole currents in the logic stage, and are approximately $V_b/2$ as shown in Fig 2. The multi-stage gate has high gain, fully restored outputs, and essentially Class B power/switching characteristics.

This technique can be extended to three (or more) stages as shown in Fig. 3 to allow larger voltage differences between the highest and lowest swing stages by using intermediate stages. These are also CMOS inverters (or gates), and can perform logic (not shown here). Because the buffer's input swing is increased, the gate's output drive is greater for a given buffer size. Although the extra stage adds delay, the increase in drive can result in a 4X reduction in the driver's size and input load. Alternately, the steeper slope at the output can cause lower short circuit power in the fanout gates, and lower delay even with the added stage. Any number of high or reduced voltage logic stages can be cascaded to form more complex functions, and followed by a buffer to deliver the output to the next gate. This is desirable because grouping of several clustered gates into a single more complex gate reduces delay, power and area. These added intermediate gates consume negligible static power, because of their full swing inputs. The avoided buffer stages would have added input load (driven full swing) like the extra intermediate gate itself, as well as parasitic output load.

The analysis presented in the ensuing sections is for the two stage architecture in Fig 1, but can be extended to more number of stages.

3 Mixed Swing QuadRail power and delay models

The dynamic power dissipated by a QuadRail gate driving a load capacitance C_{load} can be expressed as the sum of the energies drawn by each stage from their respective supply rails over one clock cycle [2], i.e.,

$$P_{dyn} = \alpha \cdot k \cdot C_{in} \cdot \left(V_l\right)^2 \cdot f_{clk} + \alpha \cdot C_{load} \cdot \left(V_b\right)^2 \cdot f_{clk} \quad (1)$$

where, C_{in} is the gate capacitance per input, α is the switching activity, f_{clk} is the input signal frequency, and k is as defined in section 2. Parasitic source/drain capacitances for each stage are accounted for in C_{load} and kC_{in}. The static and short circuit power components in the logic stage are as given in [9], and are negligible for the buffer stage. As the buffer transistor size increases, logic stage loading increases, increasing the dynamic power. This decreases the buffer's switching time, reducing short circuit power in all receivers (this reduction is more significant for large fanouts). Thus *QuadRail circuit power dissipation is a posynomial [10] function of buffer transistor size.*

The quadratic relationship between dynamic power and V_b suggests that smaller V_b is desirable for minimal power. This is limited by the smallest I/O swings possible under noise margin constraints [11]. The maximum separation between logic and buffer swings is limited by totempole off-currents in the logic stage. Thus, selection of high and low voltage levels involves careful consideration of the off-drive currents. Section 4 explains our static power driven approach for optimal volt-

age level selection.

Transistor level optimization problems have typically adopted RC-tree delay models [9], which deviate from SPICE simulations by 10-20%, yielding suboptimal solutions [12]. This is primarily due to not considering input waveform slope and short channel effects, both of which become significant at submicron feature sizes. Further, at reduced power supply voltages, transistors are predominantly operating in the saturation region, and a resistance approximation of a transistor during switching is inadequate. We have derived an analytical gate delay model for QuadRail gates taking into consideration both input waveform slope (approximated as a ramp signal [13]) and channel length modulation, a dominant short channel effect [9]. The expression for the 50% rising/falling delay of each stage is as follows (mathematical derivations are omitted due to space constraints):

$$Delay_{logic} = \frac{2 \cdot k \cdot C_{in}}{\beta_1 \cdot \lambda} \cdot \frac{1}{\left(\Delta + V_b - V_{t1}\right)^2} \cdot \ln\left(\frac{V_l + \frac{1}{\lambda}}{\frac{V_l}{2} + \frac{1}{\lambda}}\right) + t_T - \frac{t_T}{3 \cdot V_b} \cdot \frac{1}{\left(\Delta + V_b - V_{t1}\right)^2} \cdot \left(\left(\Delta + V_b - V_{t1}\right)^3 - \left(\Delta - V_{t1}\right)^3\right) \quad (2)$$

$$Delay_{buffer} = \frac{C_{load}}{k \cdot \beta \cdot \left(\Delta + V_b - V_{t2}\right)} \cdot \ln\left(\frac{4 \cdot \left(\Delta + V_b - V_{t2}\right) - V_b}{2 \cdot \left(\Delta + V_b - V_{t2}\right) - V_b}\right) + m \cdot t_{1(r/f)} \quad (3)$$

where, $t_{1(r/f)}$ is the first stage output's rise/fall time, given by:

$$t_{1(r/f)} = \frac{2 \cdot k \cdot C_{in}}{\beta_1 \cdot \lambda} \cdot \frac{1}{\left(\Delta + V_b - V_{t1}\right)^2} \cdot \ln\left(\frac{0.9V_l + \frac{1}{\lambda}}{\Delta + V_b - V_{t1} + \frac{1}{\lambda}}\right) + t_T - \frac{t_T}{3 \cdot V_b} \cdot \frac{1}{\left(\Delta + V_b - V_{t1}\right)^2} \cdot \left(\left(\Delta + V_b - V_{t1}\right)^3 - \left(\Delta - V_{t1}\right)^3\right) + \frac{k \cdot C_{in}}{\beta_1 \cdot \left(\Delta + V_b - V_{t2}\right)} \cdot \ln\left(\frac{2 \cdot \left(\Delta + V_b - V_{t2}\right) - 0.1V_l}{0.1V_l}\right) \quad (4)$$

Δ is the seperation between rails, i.e., Vdd1-Vdd2 = Vss2-Vss1, t_T is the input rise/fall time, λ is the channel length modulation factor [9], $\beta_1$and β are the transconductance gain factors of the logic stage and a unit-sized (1X NMOS, 2.5X PMOS) transistor respectively, V_{t1} and V_{t2} are the logic and buffer stage threshold voltages[1], and m is an empirically fitted constant for a given set of voltage levels[2].

Increasing the buffer transistor size (*k*) leads to increased load on the logic stage while improving the buffer current drive, i.e., *QuadRail delay is also a posynomial function of buffer transistor size*. This suggests that there exists an optimal buffer transistor size for a gate (for minimal delay) as a function of voltage levels and load capacitance. Section 5 explores the selection of buffer transistor size for delay and energy per logic operation optimization.

1.logic and buffer stage threshold voltages are different because opposite type devices are in conduction for any input combination that causes a transition at the output.

2.since only a portion of the logic stage output's slope affects the buffer stage delay, the input waveform slope's contribution is empirically fitted through HSPICE Level13 BSIM1 models in our analysis.

4 Static power driven voltage level selection

As mentioned in section 3, selection of high and low voltage levels in QuadRail is critical for minimizing static power as well as noise margin degradation. In order to ensure strongly turned-off devices in the logic stage, we must restrict the off-currents (static power) to an extremely small fraction of the average on-drive currents (dynamic power). Fig. 4 shows the ratio of logic stage totempole off-current to the worst-case on-drive current vs. high voltage swing for buffer swings of 0.4-1.0V for the 3-input OR gate (Fig. 1). It is observed that all graphs have two distinct regions - a steeply falling region, where I_{off} (I_{on}) falls quadratically (linearly) with V_{logic}, and a flat region where I_{off} falls exponentially with V_{logic}, due to sub-threshold conduction. Selecting a I_{off}/I_{on} ratio defines unique logic voltage swings at these buffer voltage swings; the smaller this ratio, the tighter the turn-off. As an example, selecting the "knee" of these graphs as operating points, the static currents are less than 2.5% of the on-drive currents. Fig. 5 shows these "knee" points on a buffer swing vs logic swing plot. It is observed that the graph is approximately linear and corresponds to roughly $V_{logic} = V_{buffer} + 2V_t$. Any operating point above this line implies a larger static dissipation (I_{off} > 2.5% of I_{on}) and any operating point below this line implies even tighter turn-off at the cost of increased logic and buffer stage delays. Thus, scaling down operating buffer and logic voltage levels along this line offers an efficient technique for simultaneous reduction of static and dynamic power dissipation, without degrading the switching characteristics and noise margins. As an example, at V_{logic} = 2.0V and V_{buffer} = 0.6V, a dynamic power reduction of 10X compared to static CMOS operating at 2.0V is obtained for the same load capacitance, buffer size, and clock frequency, while ensuring sufficient turn-off characteristics.

5 Delay driven buffer size selection

While optimal logic and buffer swings are set by static power driven techniques, selection of buffer transistor sizes is determined by delay constraints. From (3) it is seen that for large loads, unit-sized buffers have inadequate current drives and high delays. Since QuadRail delay is posynomial, there exists an optimal buffer transistor size (guaranteed to be a global minima [10]), for which delay is minimized. This *delay optima* is determined by differentiating (2)+(3) with respect to *k*. The optimal buffer transistor size depends on $\sqrt{C_{load}}$, $\sqrt{\beta_1}$, and approximately on the square root of the ratio of V_{buffer} to V_{logic}. Since QuadRail power is also a posynomial function of buffer size, there exists a value of *k*, for which power is also minimized. This *power optima* can be determined if the fanout and interconnect loading on a gate, and the buffer transistor sizes of those fanout gates are known. In general, larger the fanout, larger the power reduction obtained due to sizing the driving buffers at this *power optima.* Thus, increasing the buffer transistor size towards the *delay optima* simultaneously of-

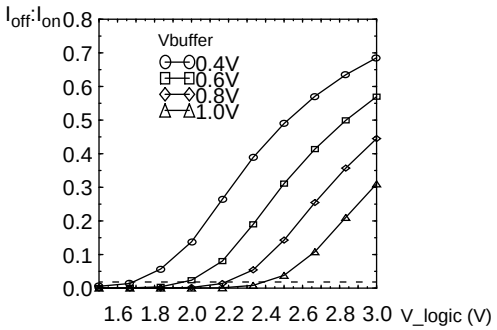


Figure 4: Off- to on-drive current ratios vs. logic stage voltage.

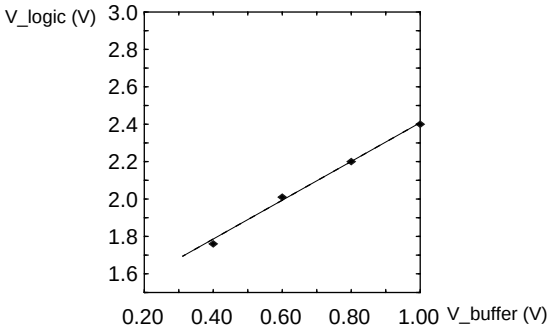


Figure 5: Logic vs. buffer stage voltage swing with $I_{off}/I_{on} < 0.025$.

fers a power reduction, until power starts to increase beyond the *power optima*.

6 Analysis of QuadRail power and delay models

To analyze the QuadRail power and delay models, we have considered a 6-input And-Or (AO222) gate cascade circuit. Fig. 6 and 7 show the gate and experimental circuit setup. The driving gate drives all the fanout gates' inputs in addition to a capacitive load of 300fF (corresponding to approximately 3000µm of metal interconnect in the HP 0.5um process). The fanout gates have unit sized buffer transistors. Fig. 8 shows the power and delay for this setup obtained from our model with V_{buffer} = 0.8V, *k* varying from 1-10 and V_{logic} varying from 1.5-3.0V. Some important conclusions can be drawn from these graphs:

- As V_{logic} is scaled towards $V_{buffer} + 2V_t$, i.e., more tighter logic stage turn-off, non-optimal sizing can cause steep delay penalties, both for over- and under-sized buffers. As V_{logic} -> 3.0V, buffer overdrive increases and optimal sizing does not significantly impact delay. We conclude that optimal buffer transistor sizing is critical at reduced power supply voltage swings.
- As V_{logic} -> 3.0V, non-optimal sizing of buffer transistors incurs a power penalty because of the high short circuit power component with minimum sized buffers. This penalty depends on the driving gate's fanout and interconnect loading. As V_{logic} is scaled, the short circuit power diminishes cubically, and power penalty due to minimum sized buffer transistors also diminishes. We conclude that minimum sized buffer transistors are best for optimal power at reduced power supply voltage swings, although there still exists a *power optima* very close to unit size.

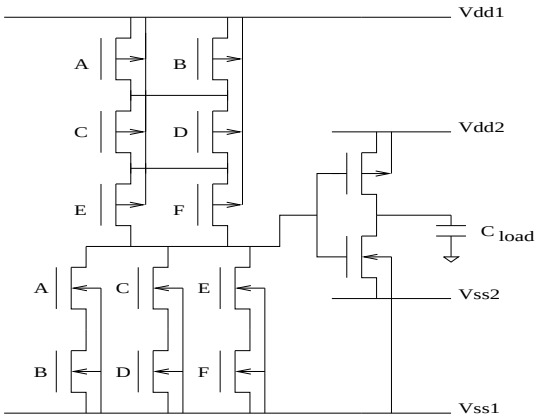


Figure 6: QuadRail 6-input AND-OR (AO222) gate.

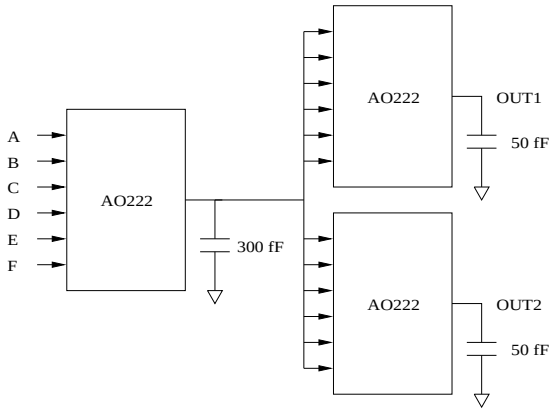
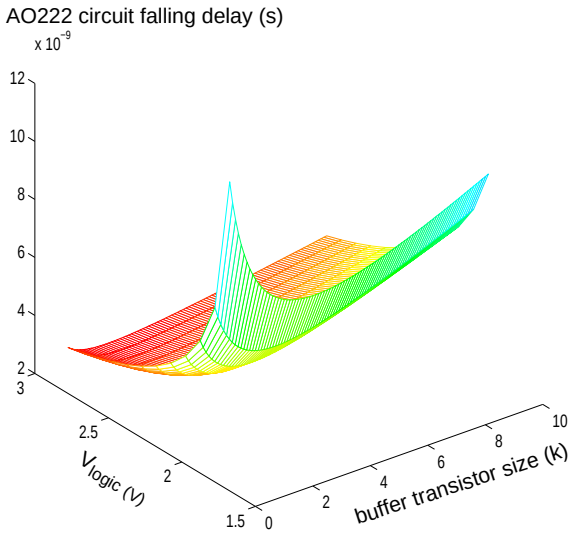


Figure 7: AO222 experimental circuit setup.

Fig. 9 shows the power and delay for the same circuit setup obtained at one operating point: V_{logic} = 2.2V and V_{buffer} = 0.8V (i.e., a snapshot of Fig. 8 with V_{logic} = 2.2V). Our models show good agreement to HSPICE simulation results; the optimal buffer transistor size predicted by our models is within 2% of HSPICE results over many operating voltage levels and capacitive loads. Notice that both Fig. 8 (our models) and Fig. 9 (HSPICE simulation) correctly show a less steeper delay penalty for over-sizing than under-sizing as expected. This is due to the relative dominance of the logic and buffer stage delays in the total delay (eqn. (2) and (3) respectively).

7 CMOS vs. QuadRail comparison results

In this section we present power and delay comparisons between QuadRail and static CMOS for the AO222 gate. QuadRail operates at the same operating point as in section 6 (V_{logic} = 2.2V and V_{buffer} = 0.8V) and CMOS operates at V_{dd} = 3.0V and at a V_{dd} for which QuadRail and CMOS delays are approximately equalized, i.e., difference in delays is less than 1.5ns (V_{dd} = 1.6V). The comparison results are obtained through HSPICE simulations in the 0.5µm process. Load capacitances in the range 0-1pF and buffer sizes of 1X, 2X, and 4X are considered for both cases. Fig. 10 shows the worst-case delay of the CMOS and QuadRail AO222. Fig. 11 shows the power



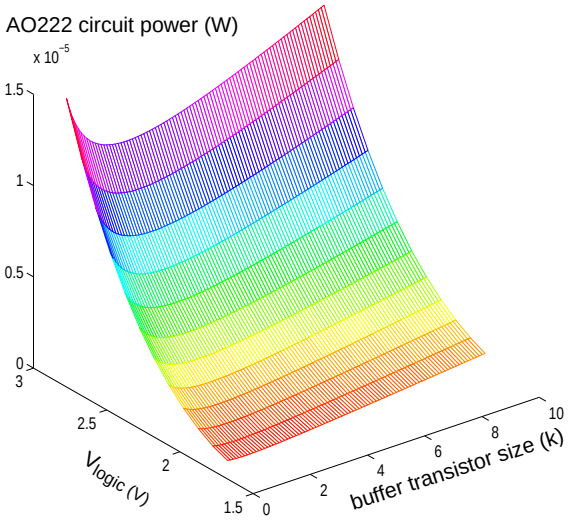


Figure 8: AO222 circuit falling delay and power vs. V_{logic} and buffer transistor size (k) [f_{clk} = 50 MHz; α = 1].

consumption of both CMOS and QuadRail gates at 50MHz and α = 1. With increasing loads, both QuadRail and CMOS delays increase with the same steepness, but QuadRail's power increases less steeply than CMOS due to reduced load voltage swing. Thus, at a load capacitance of 1pF, with equal delays a 3X power reduction is obtained compared to CMOS, and a 10X power reduction is obtained compared to CMOS at V_{dd} = 3.0V (corresponding delay penalty = 3X), when both are sized optimally for that load. The power savings is even higher as load capacitance increases beyond our range of analysis. At small loads (< 150fF), CMOS power dissipation is better compared to QuadRail when their delays are equal: this is due to QuadRail's *not-fully-turned-off-logic-stage* subthreshold power dissipation. Since static CMOS inputs swing rail to rail, the only off currents (and hence static power) is due to leakage currents of parasitic p-n junctions formed by the transistor diffusion regions and well/substrate. Fig. 10 re-emphasizes the importance of selecting the optimal size for buffer transistors in QuadRail - a 2.2X delay penalty if the buffers are 1X for

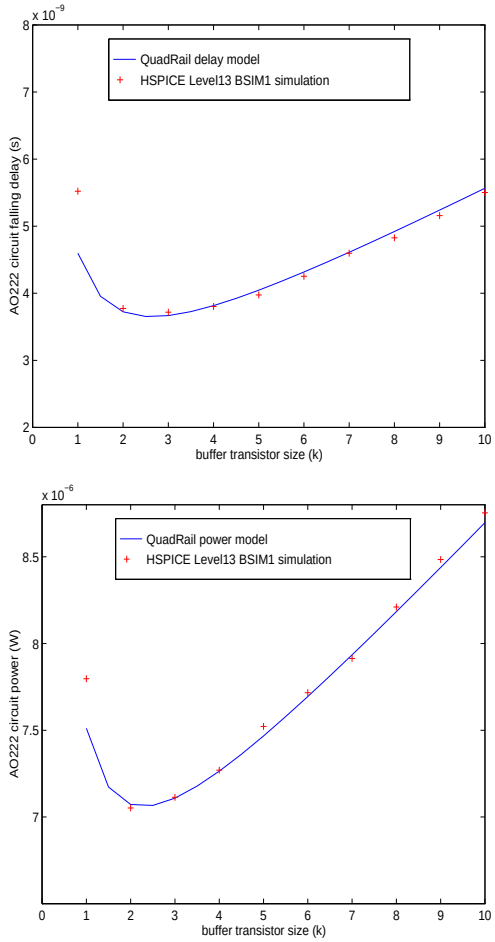


Figure 9: QuadRail delay and power models compared to HSPICE results [V_{logic} = 2.2V, V_{buffer} = 0.8V, f_{clk} = 50 MHz, α = 1]..

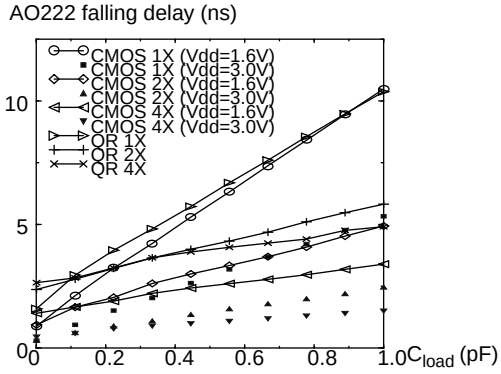


Figure 10: CMOS vs. QuadRail comparison: AO222 falling delay vs. C_{load} for 1X, 2X, and 4X buffers.

C_{load} = 1pF as opposed to their optimal size of 4X.

8 AOI222 Test-chip measurement results

A 6-input And-Or-Invert (AOI222) QuadRail test chip was fabricated in the HP 0.5µm process, to compare power and delay of QuadRail vs. static CMOS. 17 AOI222 gates were cascaded together with each AOI222 driving the next AOI222's 6 inputs and an additional load of 0.25mm, 0.50mm, 1.0mm, and 2.0mm of metal interconnect capacitance. The buffer

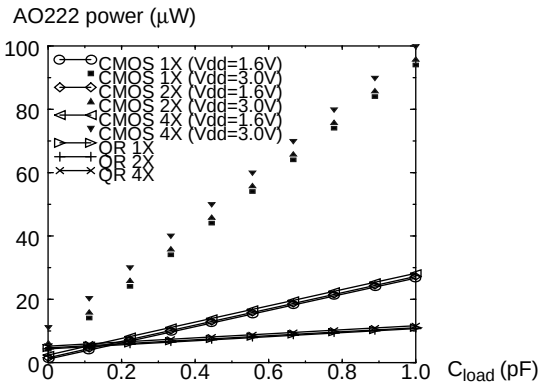


Figure 11: CMOS vs. QuadRail comparison: AO222 power vs. C_{load} for 1X, 2X, and 4X buffers.

stage:logic stage transistor size ratio is 2.5X. The AOI222 gate is constructed in a NAND-NAND-INVERT configuration as in Fig. 3. For the QuadRail AOI222s, the first (preamplifier) stage 2-input NAND gates and second (logic) stage 3-input NAND gate operate at supply voltage swings of 2.0V and 3.0V respectively. The buffer stage supply voltage and I/O swings are 1.0V. For the CMOS AOI222 all three stages operate at V_{dd} = 3.0V. Table 1 summarizes the measured power (with α = 1) and input-pin to output-pin delay for the QuadRail and CMOS AOI222 blocks. The input signal frequency is 10MHz. A 3.1X power savings is achieved compared to CMOS for a 2mm interconnect loading. At this load, QuadRail AOI222 delay is 1.06X higher than CMOS, offering an overall power-delay product reduction of 2.92X, at the same operating frequency. HSPICE full-chip simulation results show good agreement (within 10%) to these experimental measurements. The AOI222 test chip microphotograph is shown in Fig. 12.

Table 1. QuadRail AOI222 test chip measurement results.

interconnect length (mm)	QuadRail power (μW)	CMOS power (μW)	QuadRail delay (ns)	CMOS delay (ns)
0.25	206	383	32.82	18.24
0.50	214	418	33.80	19.24
1.00	275	450	34.99	20.81
2.00	289	896	39.81	37.62

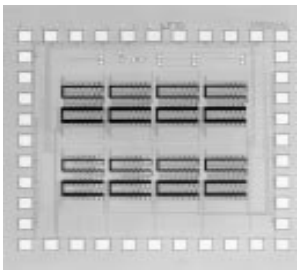


Figure 12: Microphotograph of the QuadRail AOI222 test chip.

9 Conclusion

Mixed Swing QuadRail approach presents an effective methodology for low voltage (sub-1V) logic in a high threshold voltage CMOS fabrication process, while maintaining high performance. Static power driven selection of the high and low swing voltage levels in QuadRail offers simultaneous reduction of static and dynamic power without degradation of switching characteristics and noise margins. QuadRail delay and power models reveal the importance of optimal selection of buffer transistor sizes at sub-1V I/O swings: both under- and over-sized buffer transistors can lead to steeply increased delay penalties. Comparison results between static CMOS and QuadRail show that significant power savings can be achieved through optimal selection of voltage levels and buffer sizes. Detailed HSPICE simulations using Level 13 BSIM1 models and test results from a 6-input AOI222 chip fabricated in the HP 0.5μm process substantiate our models and demonstrate significant power reduction compared to static CMOS.

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