LTCC Spiral Inductor Modeling, Synthesis, and Optimization

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In RF/microwave circuit design, inductor design is one of the most difficult and time-consuming tasks due to the tedious trial-and-error optimization process to achieve the target specifications.

This paper brings forward a fast and accurate spiral inductor synthesis method, which automatically generates physical layout of inductors according to electrical specifications. This method is based on the fusion of substrate-aware PEEC model with optimal nonlinear optimization engine. Calculated inductance and Q values show good agreement with industrial field solver and measurement results.

I. Introduction

In the realm of analogue circuits, CMOS technology is one of the most popular processes. However, the lossy nature of silicon limits the implementation of high quality inductors in CMOS technology. An alternative approach could be integrating CMOS circuits with passive elements implemented on LTCC (low temperature co-fired ceramic) technology which has better dielectric properties. Although the LTCC process can deliver higher quality inductors, the design process is time consuming due to the lack of fast and accurate model to estimate inductors' electrical characteristics. In this paper, we propose accurate partial elements equivalent circuit (PEEC) modeling, synthesis, and optimization algorithms in LTCC process. The important details in LTCC spiral inductor modeling are described and the measurement results demonstrate the accuracy and quality of our algorithms.

The straightforward inductor optimization approaches are enumeration and binary search based upon exhaustive field solver [1] or simplified circuit model [2]. Other proposed optimization methods include geometry programming (GP) [3], SQP [4], mesh adaptive direct search (MADS) [5], and implicit space mapping (ISM) [6]. These methods are either based on CMOS inductor model [4-5] or posynomials (sum of monomial) formulas derived from a large CMOS inductor family [3], [6]. Since the conductor size and spacing on a typical LTCC process are much larger than those in CMOS process, the circuit models or formulas proposed in these literatures are no longer valid. In [7], an approach of optimizing LTCC inductors using neuron network is proposed. Instead of using circuit models or extracted posynomials functions, this method trains the neuron network from measured inductor data which is far too expensive and time-consuming.

The rest of this paper is organized as follows: in section II, we present the background knowledge of inductor synthesis and our enhancements to the traditional PEEC inductor model. The optimization method is presented in section III. The verification on calculated inductance and Q value by proposed method against EM field solver and measurement is given at section IV. The optimized results of a 2.5 turn inductor are also included. Finally, we conclude this paper in section V.

II. Preliminaries

A. *Basic inductor modeling*

Fig. 1 shows the layout of a 1.5 turn spiral inductor with its tuning variables of outer dimension (*W,H*), width (*w*) and spacing (*s*). In this paper, an extra variable *d* is introduced to realize inductor with non-uniform width. The actual width for each segment, w_i is given as follows:

$$w_i = w_{i-1} - (total\ segments - i)\, d\,, \qquad (1)$$

where *i* is an incremental number assigned to each segment starting from the outer ring to inner ones. By narrowing the line width of inner turns, the total magnetic induced currents can be reduced, which results in a higher quality factor. The distributed lumped model for spiral inductors is shown in Fig 2.

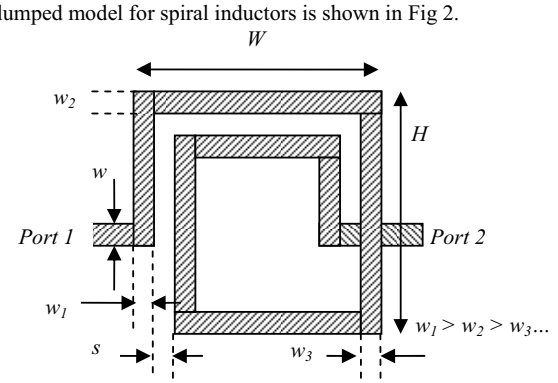

Fig. 1 Inductor layout (top view) and related parameters.

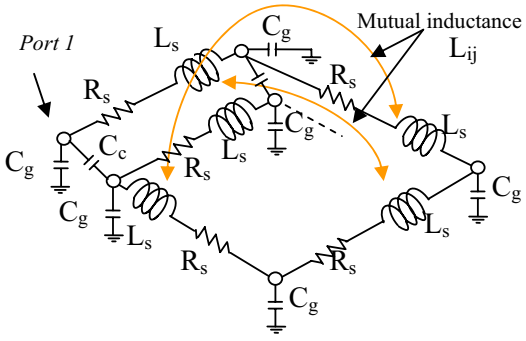

Fig. 2 Equivalent lumped circuits for inductor.

B. *Skin and proximity effects modeling by adaptive meshes*

It is well known that at microwave frequencies, the metal loss is dominated by skin and proximity effects instead of DC resistance. In [8], Pettenpaul propose a fitted close form formula to estimate the skin effect. However, the proposed

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formula is limited to conductors with $w/t < 12$. On the other hand, [2] propose that skin effect can be estimated by dividing the conductor into 6 segments horizontally with an approximate resistance formula to account for lateral current distribution. However, this method is found accurate only when the conductor size is small. In [2], the proximity effect is estimated by an effective width concept with the assumption of $w>>s$. This assumption is mostly valid in CMOS process but not applicable in LTCC technology. There is another close form formula proposed in [9] to predict the effective resistance due to proximity effect. This approximate formula is accurate up to a cutoff frequency which is often found to be lower than operating frequencies.

In order to capture both skin and proximity effect, we introduce a PEEC simulation technique with 2 dimensions meshing strategy. In [10], the author shows that both skin and proximity effects can be captured by a conductor divided into 20 x 20 filaments using PEEC simulation technique. In this paper, we show that similar result can be obtained by a non-uniform meshing strategy where the conductors are divided into 6 segments in horizontal and vertical directions. This would result in a total of 36 filaments per conductor rather than 400. Therefore, the simulation time is greatly reduced. Instead of a fixed [w/20, w/20, 2w/5, 2w/5, w/20, w/20] ratio as proposed in [2], we divide conductors into
[δ, δ, (w-δ)/2, (w-δ)/2, δ, δ] along horizontal axis and
[δ, δ, (t-δ)/2, (t-δ)/2, δ, δ] on vertical axis. Since the skin depth is frequency dependent, the size of filaments close to conductor surface will decrease according to the simulation frequency and therefore ensures the filaments are small enough to capture the non-uniform current distributions at high frequencies. Fig. 3 illustrates a conductor's cross section with our meshing strategy.

After performing the meshing, the DC resistance for each filament is calculated and filled into the system matrix (3). Besides, the self and mutual inductance of filaments are calculated using the well known Greenhouse formulas [11] to form the complete impedance matrix, Z.

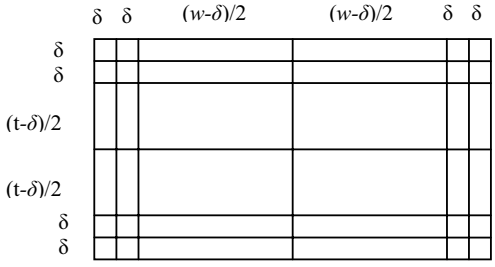

Fig. 3 A conductor with non-uniform meshing.

In this paper, the proposed 2 dimensions meshing strategy is verified using an industrial field solver [12]. In order to show the skin effect in different technology, two typical CMOS conductors and a typical LTCC conductor are simulated. These simulations are carried out on a 500um long rectangular copper conductor in free space with a ground plane. The conductors' dimension and extracted resistance are shown in Fig. 5.

In Fig. 5, it is observed that the single dimension meshing method proposed in [2] is only accurate for small size conductors (line *a* and *b*) while the 2 dimensions meshing strategy applied in this paper is capable of capturing skin effect for all cases up to 10 GHz. Based on the extracted surface current data, we found that the vertical current distribution for thick conductor is not symmetrical as compared to the thinner one. Therefore, the approximation formula used in [2] which assumed symmetrical vertical current profile is not applicable for LTCC technology where thick conductors are used.

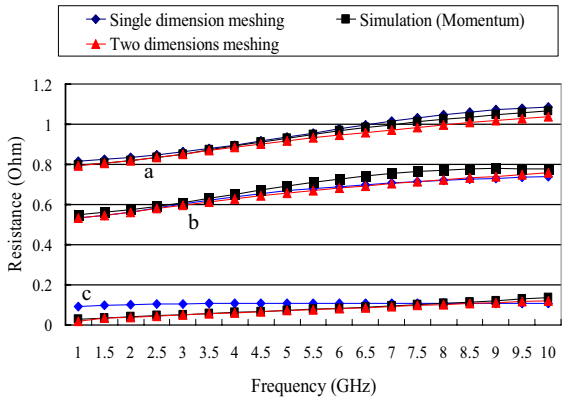

Fig. 5 Resistance of a single conductor with different width and thickness, (a) w=10,t=1, (b) w=15,t=1, (c) w=100, t=13. (unit:um)

C. Substrate effect

In this paper we model the eddy current effect by placing an image inductor opposite to the physical one carrying the same current magnitude but in opposite direction and the effective inductance is given by,

$$L_{eff} = L_{freespace} - L_{image} \tag{2}$$

D. Parasitic capacitances

In LTCC process, the inductor metal tracks are wider and covering larger area compared to typical CMOS process. Thus, the capacitance effect should in no way be neglected or approximated by simple DC formula.

In this approach, the parasitic capacitance is estimated by capacitance formulas derived from microstrip lines model. The wavelength of RF operating frequencies is much larger than typical inductors implement on LTCC. Therefore, we assume that the voltage phase difference between the adjacent metal tracks is very small and that the complex capacitance coupling effects are dominated by even mode components. The formulas for the distributed capacitance model are given in [13-14].

E. Inductance and quality factor extraction

The distributed RLC network is written in a system matrix format as follows:

$$\begin{bmatrix} Z & A^T & 0 & 0 \\ A & S & Y_g^* & Y_C^* \\ 0 & Y_g & I & 0 \\ 0 & Y_c & 0 & I \end{bmatrix} \begin{bmatrix} I_s \\ V_n \\ I_g \\ I_c \end{bmatrix} = \begin{bmatrix} 0 \\ V \\ 0 \\ 0 \end{bmatrix}, \tag{3}$$

where Z is the impedance matrix of the branches, Y_g is the admittance matrix for the capacitance of parallel branches, Y_c is the

admittance matrix models the coupling between metals, and *I* is an identity matrix, respectively. *A* is the incidence matrix for series inductors while Y_g* and Y_c* are incidence matrix from capacitances. S is a unique matrix with zero entries except for the top left and bottom right corner entries assigned to 1. On the right hand side, V is a matrix represents the unity input voltage. I_s are the solved currents for each filaments, V*n* are the nodal voltages, I_g are the currents flow through capacitors connected to ground and I*c* are the currents flow in coupling capacitors, respectively.

After solving the matrix, the Y parameters can be extracted from the input and output current with proper excitation voltage, where

$$Y_{11} = \frac{total\ input\ current}{Excitation\ Voltage}, \quad \text{and} \tag{4}$$

$$Y_{12} = \frac{-total\ output\ current}{Excitation\ Voltage}. \tag{5}$$

The inductance *L*, quality factor *Q* and series resistance *R* can be extracted by,

$$L = im(-1/Y_{12})/2\pi f, \tag{6}$$

$$Q = im(-1/Y_{12})/re(-1/Y_{12}), \text{ and} \tag{7}$$

$$R = re(-1/Y_{12}). \tag{8}$$

III. Inductor Optimization.

Let *W, H, n, w, s* be the outer width, outer length, number of turns, conductor width and spacing, respectively. We have inductance

$$L(W,H,n,w,s) \quad \text{and} \tag{9}$$

$$Q(W,H,n,w,s) = \frac{2\pi f \times L(W,H,n,w,s)}{R(W,H,n,w,s)}. \tag{10}$$

In [4], Yong Zhan has shown that this problem can be fit into a SQP routine. In this work, we integrated our simulation engine with the Matlab SQP tool box for optimization purpose. With the presented accurate model, a high quality inductor can be found without going through exhaustive field solver as proposed in ISM [6].

IV. Experimental and Simulation Results

A. Inductance and Q calculation

Several inductors were fabricated on LTCC process with the geometry parameters given in table I. The process used a low loss substrate with loss tangent = 0.0033 and a dielectric constant, ε_r = 7.5. Metal tracks are made of silver with a thickness of 13 um.

The fabricated inductors were measured using Agilent E8361A network analyzer and the measured S-parameters were calibrated. The *L* and *Q* are extracted using equation (6) and (7) and the results are shown in Fig. 6-7.

Table I. Fabricated Inductors Geometries

Inductor	Substrate thickness	Outer dimension	Turns	Metal width/spacing
S-800	520	800um	1.5	100um
S-1200	205	1200um	1.5	100um

The measurement results in Fig. 6-7 show that our simulation results and solutions from Agilent ADS Momentum have similar profile and are quite accurate as compare to the measurement results.

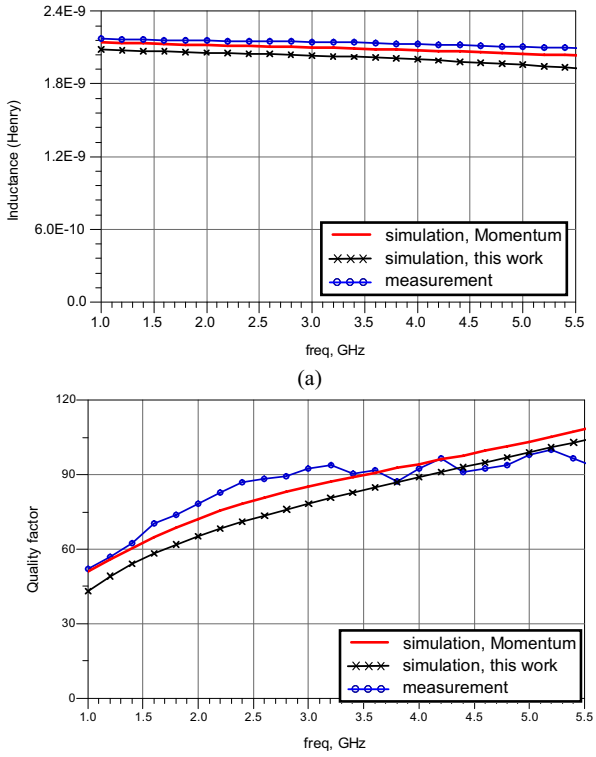

Fig. 6 Measurement and simulation results of (a) inductance and (b) quality factor for S-800.

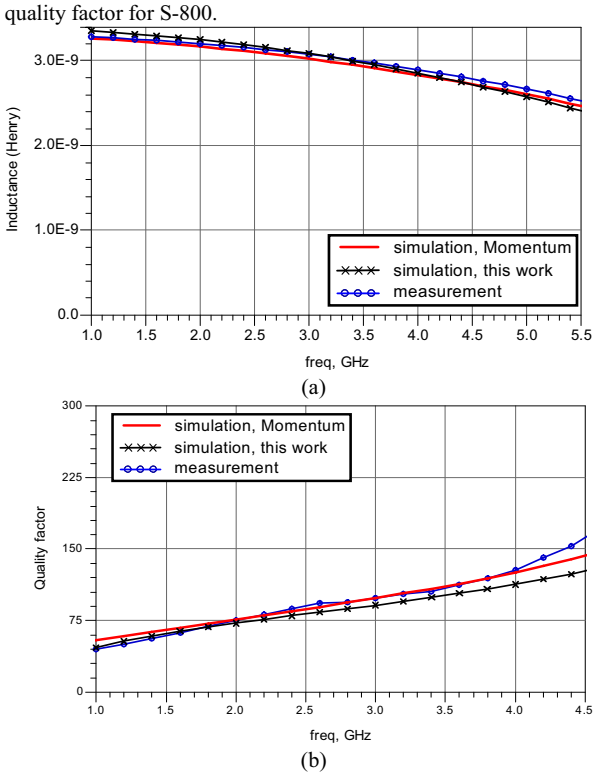

Fig. 7 Measurement and simulation results of (a) inductance and (b) quality factor for S-1200.

B.Optimization results

Our optimization method is compared to the enumeration method. The enumeration method is set to scan through the constrained region with 10 sample steps for each variable. Meanwhile, the optimization goal is to maximize the quality factor with a desired inductance value at a given frequency. The constraints of design parameters and targeted inductance values are listed in Table II. The optimized inductor parameters are verified by field solver [12] and the results are given in Table III.

Table II. Design parameters constraints.

Parameter	Constraints
Outer width, *W*	1000~1500um
Outer Length, *H*	1000~1500um
Width, *w*	100~200um
Spacing, *s*	100~200um
Parameter for inductor with decreasing width, *d*	0.1~2um
Frequency	3 GHz
Inductance (*case B*)	4nH

The results in Table III show that our method is able to find the desired inductance within 6% error and it is much faster compare to the enumeration method. The quality factors obtained by our method are also better or at least equal to the enumeration method ones. Moreover, it is observed that the inductors with non-uniform width (larger conductor width at outer ring and smaller width in inner ring) have better quality factor with a little more time cost. The result in agrees with the observation in [15], where the best Q is found for inductor with decreasing width from outer ring to the inner rings.

Table III. Optimization Results

Parameters	Enumeration	This work (constant width)	This work (non-uniform)
W (um)	1250	1183	1275
H (um)	1150	1127	1253
w (um)	110	105	126
s (um)	110	100	100
d (um)	-	-	0.5
L (nH)	3.8	3.7	3.8
Error	5%	6%	5%
Freq. (GHz)	3	3	3
Q	83	92	100
Time (s)	10002	114	207
Turns	2.5	2.5	2.5

V. Conclusion

This work has shown that with a proper model and meshing strategy, the PEEC method can estimate various electrical characteristics for inductors fabricated in LTCC process. With this method, an inductor synthesizer and optimization tool is developed without going through the curve fitting of a large inductor family. In addition, by allowing each conductor segment as dependent variable, the quality factor can be improved compared to inductors with constant width.

Acknowledgment

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