Technology Modeling and Characterization Beyond the 45nm Node

Sani R. Nassif
IBM Research - Austin
11501 Burnet Road, MS 904-6G021, Austin, TX 78758, USA
nassif@us.ibm.com

ABSTRACT

The semiconductor industry is unique in that it produces products with little or no prototyping! While a car company will build (and crash) many prototypes before converging on a final design, integrated circuits are built almost entirely on a basis of computer predictions. These predictions are based on models of performance based on simulation performed at multiple hierarchical levels, but always rooted in the end in classical circuit simulation using tools like the venerable Spice [1]. But as we continue to scale technology further, we observe a diminishing rate of performance return which is in turn causing a spiral of increasing manufacturing process complexity in an attempt to maintain performance per historical trends. This increase in technology complexity is introducing a number of *systematic* (i.e. design dependent) sources of design variability which demand modeling and characterization resources.

At the same time, we are entering a regime where the averaging effect of the law of large numbers is becoming weaker, resulting in an increase in influence of fundamental atomistic variations. Phenomena like channel dopant fluctuations [2] and line-edge roughness [3] are creating a random variability *noise floor* which is difficult to get around without significant process impact. The result of the increase in these, and other sources of variability is a corresponding increase in important circuit phenomena like SRAM stability and leakage power variations.

The net result is a gradual breakdown of the traditional ”device model + design rule” contact between design and manufacturing, and a corresponding lack of predictability in fabrication outcome that is endangering the profitability of Silicon semiconductor manufacturing as we enter what may be the last handful of generations of CMOS. This lack of predictability is happening because of two important factors.

- The overall CMOS technology slowdown has led to rapidly increasing complexity in the process and in its interaction with design. This has in turn caused an increase in the number and magnitude of systematic sources of mismatch between simulation models (both at the circuit simulation and timing levels) and hardware measurements.
- Manufacturing variability, both systematic and random, -long a source of concern only for analog design- is becoming important for digital designs as well and thus its prediction is now a first order priority. However, it is competing for the attention of researchers and CAD developers with a host of other so-called nm effects, thus slowing down the delivery of needed solutions.

The result is (a) our ability to arbitrarily compose a design out of disparate components is compromised because of a high degree of interaction between these components , and (b) our ability to predict the nominal performance of a design as well as its tolerances and sensitivities is in danger.

In this talk, we will review these issues and show how they are all related to the core issue of model to hardware matching. We will also show examples of potential solutions to this problem some of which are currently being developed in IBM, and some which are longer term and would benefit greatly from the attention of the academic community.

REFERENCES

[1] L.W. Nagel, *SPICE2: A Computer Program to Simulate Semiconductor Circuits*. PhD thesis, University of California, Berkeley, 1975.

[2] P. A. Stolk, et. al. *Modeling Statistical Dopant Fluctuations in MOS Transistors*. IEEE Trans. Electron Devices, Sep. 1998.

[3] P. Oldiges, et. al. *Modeling line edge roughness effects in sub 100 nanometer gatelength devices*. Proceedings of SISPAD, 2000.

978-1-4244-1922-7/08/$25.00 ©2008 IEEE