Modeling the Overshooting Effect for CMOS Inverter in Nanometer Technologies

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Abstract— **With the scaling of CMOS technology, the overshooting time due to the input-to-output coupling capacitance has much more significant effect on inverter delay. Moreover, the overshooting time is also an important parameter in the short circuit power estimation. Therefore, in this paper an effective analytical model is proposed to estimate the overshooting time for the CMOS inverter in nanometer technologies. Furthermore, the influence of process variation on the overshooting time is illustrated based on the proposed model. And the accuracy of the proposed model is proved to greatly agree with SPICE simulation results.**

I. Introduction

In high speed digital circuit designs, the switching speed of cells is one of the most important performance parameters to be considered. Much effort has been devoted to the extraction of accurate and efficient analytical timing models for CMOS gate cells [1]-[12]. The traditional gate delay model associates a constant delay to an output-load related characteristic of its size and input signal transition time, without taking into account the influence of the input-to-output coupling capacitance [1]-[5]. Due to the nonlinearity for propagation delay induced by the input-to-output coupling capacitance, the gate delay models in these papers[6]-[12] were proposed as the effect of input-to-output coupling capacitance was considered. However, the authors did not give detailed analysis about the overshooting time for CMOS inverters.

With semiconductor feature sizes shrink into the nanometer scale regime, the effect of the input-to-output coupling capacitance becomes much more significant to the gate delay. Therefore, it is required to present a comprehensive model of the overshooting effect for the gate timing analysis. In addition to gate delay, the overshooting time also plays an important role in the power consumption estimation because it is usually used to calculate the short circuit power consumption. Unfortunately, the overshooting time is so complicated that it has to be assumed to be as an arbitrary value in previous research, which results in inaccurate estimation for power consumption. Therefore it is also necessary to develop an accurate model of overshooting time for inverter power consumption estimation.

In this paper an efficient analytical model is proposed to estimate the overshooting time due to input-to-output coupling capacitance of CMOS inverters, which is proved to be in good agreement with the SPICE simulation results. In recent technologies, the variability of circuit delay due to process variations has become a significant focus [14]-[19]. As an important part of inverter delay, the overshooting time is also influenced by the process variation, especially in nanometer technologies. Therefore, in this paper we also evaluate the influence of the process variability on the overshooting time. And based on the evaluation, we derive that the threshold voltage contributes the largest part to the variation of overshooting time, and in contrast the variation of gate size has almost no effect on the overshooting time.

This paper is organized as follows: the problem formation is described in Section II. The proposed analytical model of overshooting time is given in Section III, while the influence of process variation on the overshooting time is derived in Section IV. Some experimental results are shown in Section V and the work is concluded in Section VI.

II. Problem Formulation

A. Inverter Model

Figure 1 shows the dynamic behavior of CMOS inverter, where the input-to-output coupling capacitance is considered. The differential equation for the CMOS inverter of Fig. 1 loaded by a coupling capacitance C_M can be described as:

$$C_L \frac{dV_{out}}{dt} = I_p - I_n + C_M \frac{d(V_{in} - V_{out})}{dt}, \quad (1)$$

where C_L is the output load including the inverter diffusion capacitance, the interconnect wire capacitance and the load gate input capacitance. Also, V_{out} and V_{in} are the gate output and input voltages respectively. I_p and I_n are the PMOS and NMOS transistor currents, respectively. Here, the differential equation is solved only for the falling input ramp since the similar expressions can be derived for the rising input ramp. The input voltage for the falling input ramp is expressed as

$$V_{in} = \begin{cases} V_{DD} & : \quad t \le 0 \\ (1 - \frac{t}{t_{in}})V_{DD} & : \quad 0 \le t \le t_{in} \\ 0 & : \quad t > t_{in} \end{cases}, \quad (2)$$

where t_{in} is the input falling time. The value of C_M in input high state consists of the side-wall capacitance of both transistors drain and the gate to drain overlap capacitance of NMOS transistor in the linear region [13].

$$C_M = C_{ox}\left(\frac{W_{neff}L_{neff}}{2} + X_{Dp}W_{peff} + X_{Dn}W_{neff}\right), \quad (3)$$

where W_{peff} and W_{neff} are the PMOS and NMOS effective channel widths respectively and L_{neff} is the NMOS effective

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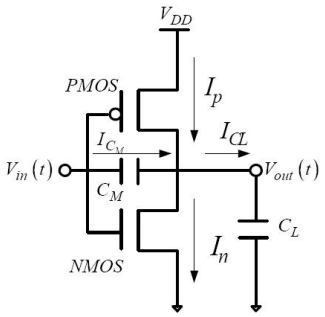

Fig. 1. CMOS inverter model.

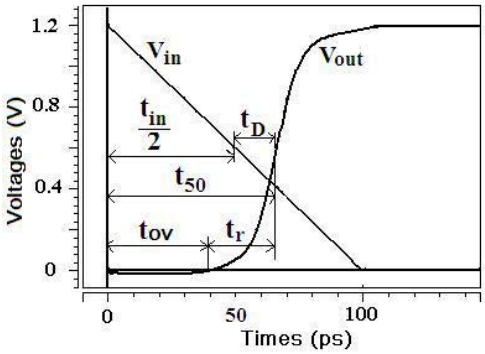

Fig. 2. The output voltage of CMOS inverter for a falling input.

channel length. Also, X_{Dp} and X_{Dn} are the gate-drain under-diffusion for PMOS and NMOS transistors, respectively. And C_{ox} is the gate-oxide capacitance per unit area.

B. Overshooting Time in Inverter Timing Analysis

Figure 2 shows the output voltage V_{out} of CMOS inverter for a falling input V_{in} using CMOS 90nm process BPTM [20]. In this paper, the overshooting/undershooting of the beginning waveform change is defined as "overshooting" and the overshooting time t_{ov} is defined as the time interval where the output voltage is beyond the power supply range as shown in Fig. 2. The gate propagation delay t_D is defined as the time interval from $V_{in} = V_{DD}/2$ to $V_{out} = V_{DD}/2$. From Fig. 2, we can obtain the gate delay

$$t_D = t_{50} - \frac{t_{in}}{2}, \tag{4}$$

where t_{50} is the time for the gate output voltage from the initial point to 50% V_{DD} point and t_{50} consists of two parts:

1) Overshooting time t_{ov}, which is resulted from the input-to-output coupling capacitance as shown in Fig. 2.
2) Gate output waveform rise time t_r from $t = t_{ov}$ to 50% V_{DD} point.

Therefore, we have

$$t_D = t_{ov} + t_r - \frac{t_{in}}{2}. \tag{5}$$

For traditional long channel transistors, the time t_{ov} is generally ignored because the coupling capacitance is small and the overshooting effect can usually be neglected [21]. Therefore, the inverter delay can be directly obtained by using the simple model of t_r. That makes researchers place the major emphasis on the rise time t_r of the gate output waveform and there is little focus on the overshooting time t_{ov}. With the scaling of gate feature sizes and the coming of the nanometer age, this value of t_{ov} becomes equal to or larger than gate delay.

Figure 3 shows the CMOS gate delay t_D and the overshooting time t_{ov} for various technology processes from 180nm to 65nm with the typical supply voltage [22]. The transistor lengths L are the minimum feature size. And the PMOS widths W_p are ten times of L while W_p is two times of W_n. The load capacitance is $C_L = 0.01pF$. The input signal transition

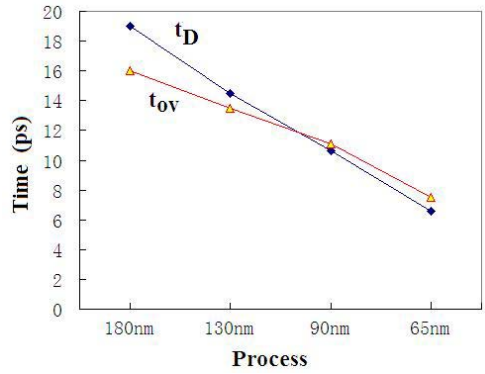

Fig. 3. Gate delay t_D and overshooting time t_{ov} with various process.

time t_{in} is 50ps. From Fig. 3, it is clearly shown that the value of t_{ov} becomes equal to or larger than gate delay in nanometer technologies, which leads to the accuracy of gate delay is determined greatly by t_{ov}.

Moreover, from Eq. (5) it can be inferred that the gate delay estimation in nanometer technologies consists of two main parts. One is t_r that can be obtained by using the traditional model. Another is t_{ov} which is generally ignored in traditional research. Therefore, it is necessary to develop an accurate model of t_{ov} for the inverter timing analysis.

C. Overshooting Time in Inverter Power Analysis

The power dissipation of CMOS gates consists of two main components. One is the dynamic dissipation, which is due to the charge/discharge of gate output loads. Another is the short circuit power, which is due to the direct supply-ground conducting path created during the transition. Several works have reported the model of the power consumption in [13][23][24], where the overshooting time is one of important parameter in the short power estimation as shown in Fig. 4. The short-circuit energy dissipation per transition is commonly written as

$$P = V_{DD} \int_{t_{ov}}^{t_{off}} I_n dt, \tag{6}$$

where t_{off} is the time when NMOS transistor is off and equals the time spent by the input slope to reach the supply-

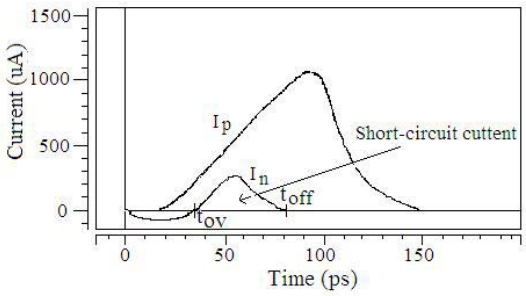

Fig. 4. Output current evolution in NMOS and PMOS transistors for a falling input voltage.

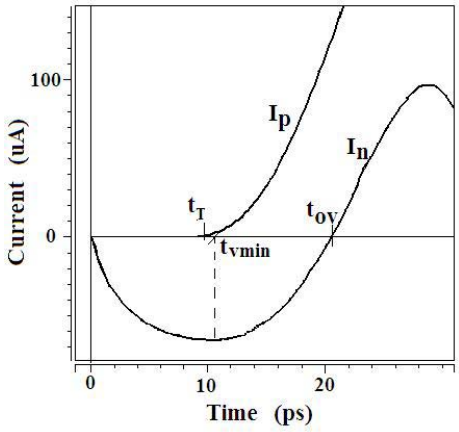

Fig. 5. The PMOS and NMOS transistor drain currents I_p and I_n during t_{ov}.

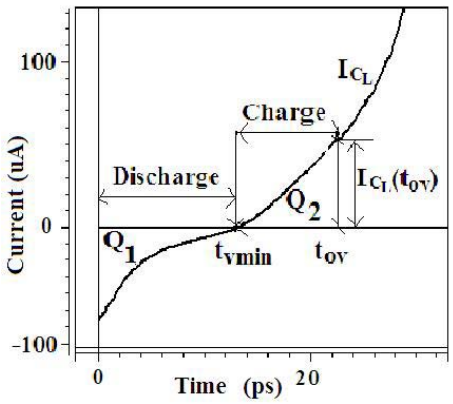

Fig. 6. The approximation of the current C_L during t_{ov}.

voltage value reduced the NMOS threshold voltage value. However, t_{ov} is so complicated that it is often assumed to be an arbitrary value, which results in inaccurate estimation for power consumption. Therefore it is also necessary to develop an accurate model of t_{ov} for power consumption calculation. In the following section, we will propose an efficient analytical model for the overshooting time including the overshooting voltage and the overshooting current.

III. Modeling the Overshooting Effect

We firstly define two time points. As shown in Fig. 5, t_T is the time when the PMOS transistor is on and $t_T = \frac{|V_{THP}|}{V_{DD}} t_{in}$. And, t_{vmin} is the time when the output voltage is at its minimum. Then the overshooting period can be divided into two parts

1) $t < t_T$: PMOS transistor is off. The voltage of the capacitance C_L begins to decrease from zero due to a partial discharge through coupling capacitance.
2) $t > t_T$: PMOS transistor begins to conduct and the PMOS current charges the load capacitance C_L. Then the voltage of load capacitance increases. Once the output voltage goes up to zero, the NMOS current becomes positive.

At the time $t = t_{ov}$, the charge of C_L is zero and the gate output waveform rises from zero. Therefore, we have

$$Q_L = Q_2 - Q_1 = 0, \tag{7}$$

where Q_1 is the charge flowing out of C_L, and Q_2 is the charge flowing into C_L during the overshooting time.

We rearrange Eq. (1) as

$$I_{C_L} = I_p - I_n + I_{CM}, \tag{8}$$

where I_{C_L} is the load current and I_{CM} is the current flowing through the coupling capacitance C_M. When $t < t_T$, $I_{C_L} = I_{CM} - I_n$. When $t = t_T$, the PMOS transistor turns on. Then $I_{C_L} = I_p - I_n + I_{CM}$. Figure 6 shows the load current I_{C_L} during t_{ov}. The sizes of inverter transistors are $W_p/L_p = 2um/0.1um$ and $W_p/L_p = 4um/0.1um$ with $90nm$ process technology [22]. The input transition time is $t_{in} = 50ps$ and the load capacitance is $C_L = 0.01pF$. As shown in Fig. 6, the load current I_{C_L} can be assumed as linear during the charge time $t > t_{vmin}$. Therefore, we can get a simple expression for Q_2 as

$$Q_2 = \int_{t_{vmin}}^{t_{ov}} I_{C_L}(t)dt \approx \frac{I_{C_L}(t_{ov})(t_{ov} - t_{vmin})}{2}. \tag{9}$$

Then, we have the expression

$$t_{ov} = \frac{2Q_1}{I_{C_L}(t_{ov})} + t_{vmin}, \tag{10}$$

where the second term t_{vmin} corresponds to the discharge time and the first term $\frac{2Q_1}{I_{C_L}(t_{ov})}$ corresponds to the charge time.

When $t = t_{ov}$, the PMOS transistor is on. Since the drain-source voltage V_{DS} of NMOS transistor is zero, the drain current I_n should be zero. Also, due to $\frac{dV_{in}}{dt} \gg \frac{dV_{out}}{dt}$ during overshooting period, the current $I_L(t_{ov})$ can be expressed as

$$I_{C_L}(t_{ov}) = C_M \frac{dV_{in}}{dt} + I_p(t_{ov}). \tag{11}$$

Before proposing the analytical model, the transistor model in nanometer technology is firstly described. As shown in Fig. 7, the transistor model can be assumed as linear model based on α-power MOSFET model [3] because $|V_{DS}|$ of PMOS transistor is much more larger than $|V_{GS} - V_{TH}|$ in the

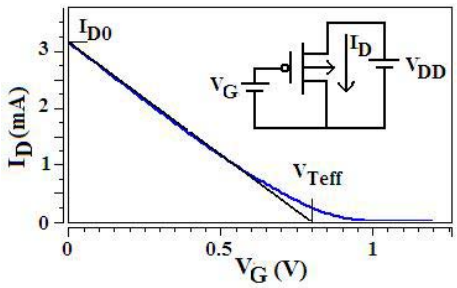

Fig. 7. The approximation of PMOS transistor drain current.

overshooting period. Therefore, this linear model is given as

$$I_p(t_{ov}) = I_{D0}\left(\frac{|V_{GS}| - |V_{Teff}|}{V_{DD} - |V_{Teff}|}\right), \tag{12}$$

where I_{D0} is the drain current in saturation at $V_{GS} = V_{DS} = V_{DD}$ and V_{Teff} is the effective threshold voltage in the linear approximation as shown in Fig. 7. Also,

$$|V_{GS}| = \frac{t_{ov}}{t_{in}} V_{DD}. \tag{13}$$

Due to Eqs. (10), (11) and (12), we can obtain that

$$t_{ov} = \frac{2Q_1}{\frac{t_{ov}-t_{Teff}}{t_{in}-t_{Teff}} I_{D0} + C_M \frac{dV_{in}}{dt}} + t_{vmin}, \tag{14}$$

where $t_{Teff} = \frac{V_{Teff}}{V_{DD}} t_{in}$.

A. Analytical Expression for Q_1

When $t < t_T$, the PMOS is cut off. Since $V_{DS} \ll V_{GS}$, the NMOS drain current can be simply expressed as

$$I_n \approx K' \frac{W}{2L}(V_{GS} - V_{THN})V_{DS}, \tag{15}$$

where K' is the transconductance parameter and V_{THN} is the NMOS threshold voltage. Therefore, we have the expression

$$(C_L + C_M)\frac{dV_{out}}{dt} + \beta_n(V_{GS} - V_{THN})V_{out} = C_M \frac{dV_{in}}{dt}, \tag{16}$$

where $\beta_n = \frac{K'W}{2L}$. Since V_{GS} is also a function of time, the equation can not be easily solved analytically. For this reason, V_{GS} is replaced by its average value $\hat{V}_{GS} = (2V_{DD} - |V_{THP}|)/2$, where V_{THP} is the PMOS transistor threshold voltage. This is a valid approximation since for most of the practical cases V_{GS} values are very close to the average values. Then the solution of the differential equation is that:

$$V_{out}(t) = \frac{C_M \frac{dV_{in}}{dt}}{\beta_n(\hat{V}_{GS} - V_{THN})}\left[1 - e^{-\frac{\beta_n(\hat{V}_{GS}-V_{THN})}{C_L+C_M}t}\right]. \tag{17}$$

When $t_T < t < t_{vmin}$, the PMOS transistor is on and the expression for the output voltage is more complicated. Commonly, the output voltage at t_T is close to the one at t_{vmin} for the fast input signal. For the slow input signal, $V_{out}(t_T) = V_{out}(t_{vmin})$. Then the charge Q_1 is obtained from the output voltage and expressed as

$$Q_1 = C_L V_{out}(t_{vmin}). \tag{18}$$

B. Analytical Expression for t_{vmin}

When $t = t_{vmin}$, since $\frac{dV_{out}}{dt} = 0$, the current flowing into capacitance loads is zero. Therefore, from Eq. (1) we have

$$I_p(t_{vmin}) = I_n(t_{vmin}) - C_M \frac{dV_{in}}{dt}. \tag{19}$$

Commonly, the value of $V_{out}(t_{vmin})$ is close to $V_{out}(t_T)$. And we can also assume that $I_n(t_{vmin})$ is equal to $I_n(t_T)$. Then we obtain

$$I_n(t_{vmin}) = C_M \frac{dV_{in}}{dt}\left[1 - e^{-\frac{\beta_n(V_{DD}-V_{THN})}{C_L+C_M}t_T}\right]. \tag{20}$$

Using the PMOS transistor drain current expression at the time $t = t_{vmin}$, we obtain the expression of t_{vmin}

$$t_{vmin} = t_T + \kappa(t_{in} - t_T), \tag{21}$$

where

$$\kappa = \frac{C_M V_{DD} e^{-\frac{\beta(V_{DD}-V_T)}{CL+C_M}t_T}}{t_{in} I_{D0}}.$$

As for the fast input, when the PMOS transistor is on, the NMOS transistor drain current is less than the current flowing through the coupling capacitance. Therefore, $t_{vmin} > t_T$. However, as for the slow input, the NMOS transistor drain current is equal to the current flowing through the coupling capacitance, $t_{vmin} = t_T$. Then t_{vmin} should be larger than or equal to the time when the PMOS transistor is turned on.

C. Analytical Expression for t_{ov}

Depending on the above analysis, we then can get the final expression for t_{ov} as

$$t_{ov} = t_{vmin} - \frac{1}{2}\left[t_{vmin} - t_{Teff} - C_M \frac{V_{DD}}{t_{in}} \frac{t_{in} - t_{Teff}}{I_{D0}}\right] + \sqrt{\frac{2Q_1}{I_{D0}}(t_{in} - t_{Teff}) + \frac{1}{4}\left[t_{vmin} - t_{Teff} - C_M \frac{V_{DD}}{t_{in}} \frac{t_{in} - t_{Teff}}{I_{D0}}\right]^2}, \tag{22}$$

where Q_1 and t_{vmin} are obtained using Eqs. (18) and (21). As t_{in} decreases to zero, the overshooting time can be written as

$$\lim_{t_{in}\to 0} t_{ov} = t_{ov}^{min} = \frac{C_M}{I_{D0}}(V_{DD} - V_{Teff}), \tag{23}$$

where $I_{D0} \propto C_M$. From Eq. (23), it can be inferred that the value of t_{ov}^{min} is almost constant for a certain technology and the power supply voltage since it is determined only by I_{D0} and C_M. Moreover the overshooting time rises when the input signal transition time increases as discussed. Thus, this value is regarded as the minimum value of the overshooting time. From Eq. (5), it can be seen that the gate delay t_D is the sum of t_{ov} and t_r when $t_{in} = 0$. For a given process and the power supply voltage the gate delay cannot be smaller than t_{ov}^{min}. Therefore, the existing of the minimum overshooting time is one of the main reasons that the gate delay can not be reduced further when it decreases to a certain value.

IV. Considering Process Variation

In recent technologies, the variability of circuit delay due to the process variation has become a significant concern. As process geometries continue to shrink, the evaluation for critical device parameters is becoming more and more difficult due to the significant variations such as device lengths, doping concentrations, oxide thicknesses and so on. As one of the main parts in gate delay, the overshooting time is also influenced greatly by these process variations. Therefore, it is necessary to give the analysis of the influence resulted from the oxide thickness T_{ox}, the transistor threshold voltage V_T and the gate length L.

In order to assess the impact of the variability on the overshooting, it is better to compute the sensitivities of the overshooting time with respect to the variation sources. Similarly as the path-based statistical timing analysis approach introduced in [14] and [15], we also get the first order model for the overshooting time as a function of the variation sources:

$$t_{ov} = t_{ov}^0 + \frac{\partial t_{ov}}{\partial V_T}\triangle V_T + \frac{\partial t_{ov}}{\partial T_{ox}}\triangle T_{ox} + \frac{\partial t_{ov}}{\partial L}\triangle L, \qquad (24)$$

where t_{ov}^0 is the nominal overshooting time and $\triangle V_T$, $\triangle T_{ox}$ and $\triangle L$ are the process parameter deviations from nominal. In Eq. (12), V_{Teff} can be assumed to have almost the same variation as the V_T is directly because it is directly related to V_T. By using Eq. (22), we can get the first model of the variations

$$\frac{\partial t_{ov}}{\partial L} = \lambda_L \simeq 0, \qquad (25)$$

$$\frac{\partial t_{ov}}{\partial V_T} = \lambda_{V_T} \approx \frac{t_{in}}{V_{DD}}\left[1 - \kappa - \xi(1 - C_M\frac{V_{DD}}{t_{in}I_{D0}})\right], \qquad (26)$$

where ξ is obtained from Eq. (22) and can be approximately assumed to be a constant. From Eqs. (25) and (26), it is obvious that the gate length variation has almost no effect on overshooting time and that λ_{V_T} is in direct proportion to the input time t_{in}. Thus, reducing input transition time can decrease the influence of process variations greatly. As for $\partial t_{ov}/\partial T_{ox}$, it is not easily to obtain a simple expression directly from Eq. (22). But we can observe its values from amounts of Monte Carlo simulation results. Commonly, these values are much smaller than $\partial V_T/\partial V_T$.

The above analysis can be proved by the Monte Carlo simulation results using the 90nm technology process [22] as shown in Table 1, where each variation source in Table 1 is characterized by Gauss distribution $N(\mu, \sigma^2)$ (μ and σ are the mean value and the standard deviation respectively) and each source maintains a 10% variation from run to run for a 3σ distribution. From Table 1, it is shown the effect of V_T variation is the largest in the three parameters and the variation of L has almost no effect on the overshooting time. Moreover, the percent of σ/μ for V_T is approximately constant and the percent for T_{ox} decreases greatly when t_{in} is changed from $100ps$ to $20ps$. Thus, V_T has much more significant effect on the variability of t_{ov} than T_{ox} because t_{in} also decreases with the device scaling. Furthermore, it can be seen from Eq. (24) that the variation of the overshooting time is determined by the process parameter deviations from nominal. As shown in Fig. 8, the variability of threshold voltage V_T becomes larger and larger ,and even reaches above 80% in sub-28nm process with the gate feature size scaling. Therefore, V_T will contribute the main part to the variation of overshooting time with continuing device scaling.

TABLE I

T_{ov} distribution for different parameter variation.

tin (ps)	mean (ps)	σ for V_T (ps)	σ for L (ps)	σ for Tox (ps)
20	14.65	0.24	0	0.04
40	21.18	0.41	0	0.12
60	27.06	0.57	0	0.21
80	32.62	0.73	0	0.305
100	37.95	0.9	0	0.402

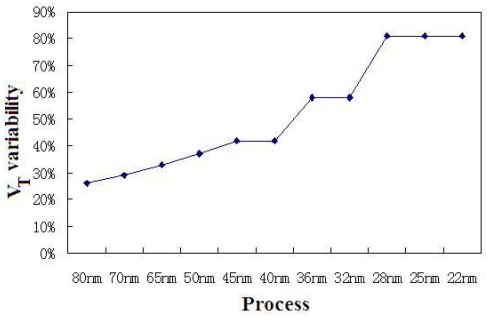

Fig. 8. Threshold voltage variability with feature size scaling [20].

V. Experimental Results

We have applied the proposed method to the CMOS inverters to further verify its correctness with the 90nm technology process [22]. In [1] and [6], the authors assumed the output waveform rise/fall at the time $t = t_T$ or $t = t_n$, which is defined as the simple model in this paper. Furthermore, an empirical expression of t_{ov} was derived to calculate the power consumption of CMOS buffer in [13] and this empirical value was also used to estimate the inverters delay in [12]. In the followings the overshooting time of the proposed method is compared with the ones of SPICE, reference [13] and the simple model for various input signals, various driving transistors.

Figure 9 plots the comparison of the overshooting time t_{ov} with respect to the various input signal t_{in}. The sizes of inverter transistors are $W_p/L_p = 2um/0.1um$ and $W_n/L_n = 1um/0.1um$. The input signal transition time ranges from $10ps$ to $100ps$ covering both fast and slow input transition time. The capacitance load is $C_L = 0.01pF$. From Fig. 9, it can be inferred that the overshooting time t_{ov} increases with the input signal transition time t_{in}. Simulation results show that the proposed method is close to the SPICE results within 4.6%. By contrast, the method in [13] cannot capture the overshooting time with the increasing input signal transition time. The simple method also results in a large error about 75.0%.

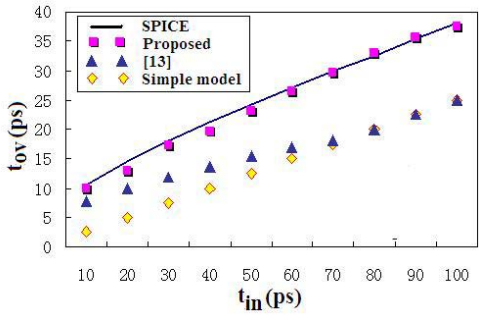

Fig. 9. The overshooting time t_{ov} comparison of proposed method with SPICE, [13] and the simple model for various input signal transition time t_{in}.

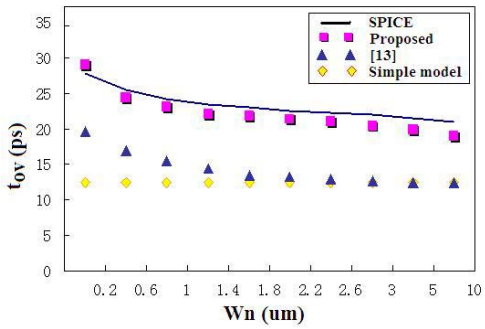

Fig. 10. The overshooting time t_{ov} comparison of proposed method with SPICE, [13] and simple model for various gate drive ability.

Figure 10 plots the comparison of the overshooting time t_{ov} with respect to the various gate driving abilities. The PMOS width varies from $0.2um$ to $10um$, where the ratio of PMOS widths to NMOS width is $W_p/W_n = 2/1$. The PMOS and NMOS transistor lengths are $L_n = L_p = 0.1um$. The input transition time t_{in} is $50ps$. The capacitance load is $C_L = 0.01pF$. From Fig. 10, it can be seen that the overshooting time decreases a little as the device widths increase. The simulation results show that the proposed model can be an effective method to estimate the overshooting time within 6.1% error. When the methods of [13] and the simple method were used, the errors can reach about 40%.

In [13], the authors proposed an empirical expression for overshooting time. However, from the simulation results it is seen that such an empirical expression cannot ensure the accuracy. Furthermore, the simple model also results a large error for estimating the overshooting time. Compared with the above methods, the approach proposed in this paper can get a much more accurate results.

VI. Conclusions

In this paper, we have presented an analytical model to estimate the input-to-output coupling capacitance effect on CMOS inverter in nanometer process. This paper clearly shows that the overshooting time due to the coupling capacitance becomes the main part in inverter output waveform. Using the proposed model, we can obtain accurate analysis for the inverter timing and power consumption. Furthermore, we derive that the threshold voltage contributes the largest part to the variability of overshooting time while the variation of the gate sizes has almost no effect on the overshooting time.

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