A New Methodology for Interconnect Parasitics Extraction Considering Photo-Lithography Effects .

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***Abstract*— Even with the wide adaptation of resolution enhancement techniques in sub-wavelength lithography, the geometry of the fabricated interconnect is still quite different from the drawn one. Existing Layout Parasitic Extraction (LPE) tools assume perfect geometry, thus introducing significant error in the extracted parasitic models, which in turn cases significant error in timing verification and signal integrity analysis. Our simulation shows that the RC parasitics extracted from perfect GDS-II geometry can be as much as 20% different from those extracted from the post litho/etching simulation geometry.**

This paper presents a new LPE methodology and related fast algorithms for interconnect parasitic extraction under photo-lithographic effects. Our methodology is compatible with the existing design flow. Experimental results show that the proposed methods are accurate and efficient.

I. Introduction

Layout Parasitic Extraction (LPE) is a critical step in the design and verification of integrated circuits. A LPE tool reads the layout geometry, computes the parasitic resistance, capacitance and inductance among the conductors, and outputs a SPICE/DSPF/SDF file. Due to runtime and historical reasons, the geometry of the conductors are assumed to be exactly the same as that in the layout.

As the optical wavelength being held at $193nm$, it is getting more and more challenging to sustain smaller and smaller critical dimensions (CD) in today's CMOS integrated circuit products. Nowadays, Resolution Enhancement Techniques (RET) are widely used to expand the capability of the exposure tools so that smaller CDs can be achieved. For example, one typical RET, the Optical Proximity Correction (OPC), involves the modification of the polygon shapes in the layout, so that the distortions introduced by the sub-wavelength lithographic processes can be compensated. However, even with these elaborate enhancement processes, it is still quite possible that significant differences exist between the ideal polygon shapes and the manufactured shapes. In Fig. 1, top views of the litho/etched metal shape profile, simulated with litho simulator PROLITH [1] is overlaid with the original layout shapes. Accurate calculation shows that the difference of RC parasitics is 20% between the *assumed* ideal polygon shapes and *realistic* shapes after litho/etching process. Such lithography effect has recently been studied by industry and academia, such as timing analysis[1], mask cost reduction[2] and litho-friendly design[3].

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Z. Li is now with IBM Austin Research Lab.
[1]PROLITH is a trademark of KLA-Tencor Corporation.

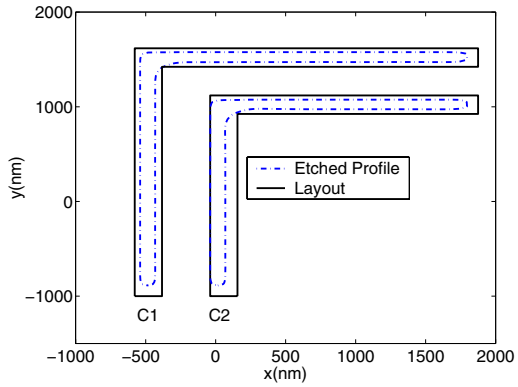

Fig. 1. The litho/etched profile vs. layout (top view)

One purpose of deploying RET and LPE tools is to ensure accurate translation of designers' intent from design to manufactured products. The LPE tools are used to compensate the non-ideal timing/noise characteristics of signal transmission paths, while the RETs are used to compensate the distortions in non-ideal litho/etching processes. With the unavoidable distortions become more and more expensive to correct, one approach is to compensate them in the LPE tools, so that their impact on the timing/noise performance of the design can be accounted for. In this paper, we present a new LPE methodology with consideration of photo-lithographic effect. Our methodology provides a way to analyze the lithography effect on the parasitics, which is key for further accurate timing and noise verification. Moreover, the methodology also provides designers capability to analyze the lithography effects under all process conditions, which can provide them a way to study the variations of these conditions and their behaviors.

The rest of paper is organized as follows. Section II introduces the lithography simulation flow used in our method. Section III provides overview of the existing and the new LPE methodologies. Section IV discusses the details how we perform side wall layer selection,shape correction, resistance and inductance parasitic extraction. Section V concludes the paper.

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II. Lithography Simulation

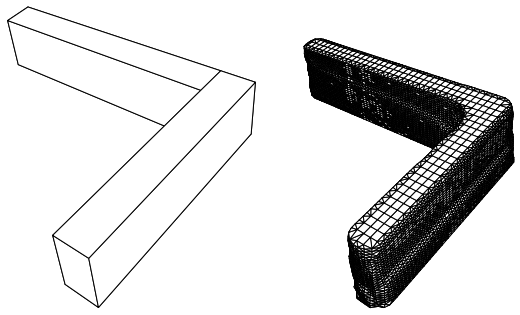
Photo-lithography modeling and simulation have been used in the industry for about 30 years. Due to its speed and cost-effectiveness, lithography simulation is widely used to study the process development, determination of sensitivity to manufacture variables, mask design verification and yield analysis. Modern lithography simulation engine can provide accurate process models for the current lithography sequence. In this paper, we use 3D lithography simulator PROLITH[4] provided by KLA-Tencor, to study the lithography effect on interconnect. In our experiments, $90nm$ technology is used and $193nm$ UV light is assumed as the lithographic light source.

The lithography simulation of our new LPE methodology includes four steps. First, the typical 3D structures are selected from the interconnect library. Second, the proper masks with OPC are derived, and the process window selection and optimization of the manufacture parameters are followed. Third, the lithography simulation is carried out to produce the 3D geometry of the interconnect structures. Finally, the lithography images are post-processed to a GDS-II format.

The outputs from lithography simulators PROLITH after processed are contours at different elevation. In other words, the output are points in the X-Y plane, organized for different Z, which we call layers. Note that such layer definition is different from metal layer in the traditional way. For each metal layer, there are often several elevations. The output for the profile in Fig. 1 is as follows:

x	y	z	layer
480.5	-1394.151	0	0
531.5	-1398.848	0	0
⋮	⋮	⋮	⋮
480.5	-1394.4	-3	1
531.5	-1399.1	-3	1
⋮	⋮	⋮	⋮

Fig. 2(a) and Fig. 2(b) show the original layout profile and the corresponding litho/etched profile, respectively. The litho/etched profile is no longer in rectangular shape and hence the current commercial 3D field solver can not handle it.



(a) Layout (b) Litho/Etched

Fig. 2. 3D profile for an elbow conductor

The difference of the extracted RC value between the original layout and the corresponding litho/etched profile can reach 20%. For example, the layout is shown in Fig. 1. Table I and II show that the parasitic capacitances and resistances considering lithographic effect are very different from those of the original layout. Note that such difference will become more severe for $65nm$ and $45nm$ technology.

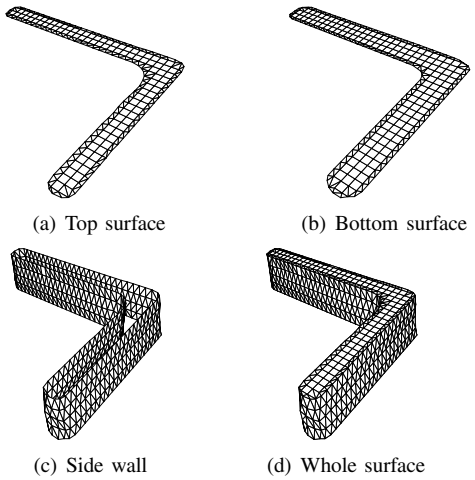
TABLE I
CAPACITANCE COMPARISON BETWEEN LITHO/ETCHED PROFILE AND LAYOUT FOR TWO ELBOW CONDUCTORS

Capacitance (aF)	Litho/ Etched	Layout	Error (%)
C_{11}	110.8	123.9	11.02
C_{22}	93.9	105.9	11.91
C_{12}, C_{21}	57.9	67.7	15.52

TABLE II
RESISTANCE COMPARISON BETWEEN LITHO/ETCHED PROFILE AND LAYOUT FOR TWO ELBOW CONDUCTORS.

Resistance (Ω)	Litho/ Etched	Layout	Error (%)
R_1	0.29	0.23	20.69
R_2	0.23	0.18	21.74

For the litho/etched interconnects extraction, Boundary Element Method such as FastCap [5] [6] is used to compute the accurate capacitance in this paper. Boundary Element Method generally only accepts triangular and quadrilateral shapes as input. Standard triangulation algorithms such as 3D Delaunay triangulation [7] [8] can be used to discretize the entire surface panels (top, bottom and side walls) with triangles. In this paper, we implemented a simple linear discretization algorithm to discretize the whole surface. The algorithm selectively connects neighboring layers for side walls to create quadrilaterals or triangles, and creates as many as rectangles on the top and bottom surfaces. From extensive experiment, we found that our special treatment gives the good balance between the number of panels and capacitance accuracy. One example of discretized panels with our algorithm is shown in Fig. 3.



(a) Top surface (b) Bottom surface

(c) Side wall (d) Whole surface

Fig. 3. One discretization example for an elbow-shape conductor

III. New LPE Methodology

The traditional LPE flow is illustrated in Fig. 4. First, the common interconnect structures and the technology files are

input to a 3D field solver. The field solver generates a pattern library to be used for LPE tools. LPE tools then read the circuit layout and the pattern library to compute the parasitics of the entire circuit. No lithography effects are considered in the traditional flow.

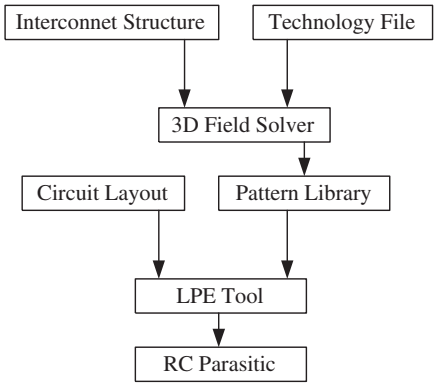


Fig. 4. Traditional LPE methodology

Here, we proposed a new flow to account for the litho/etched effects shown in Fig. 5. Two new procedures are embedded into the new flow: lithography simulation and shape correction. The shape correction algorithm is used to simplify the complicated geometry from lithography simulation, so that current 3D field solver can handle the litho/etched profile, such as shown in Fig. 1. Meanwhile, the new LPE methodology has minor change the traditional one. It is clear that the new LPE methodology improves the accuracy of parasitic extraction, and fits well into the existing design flow.

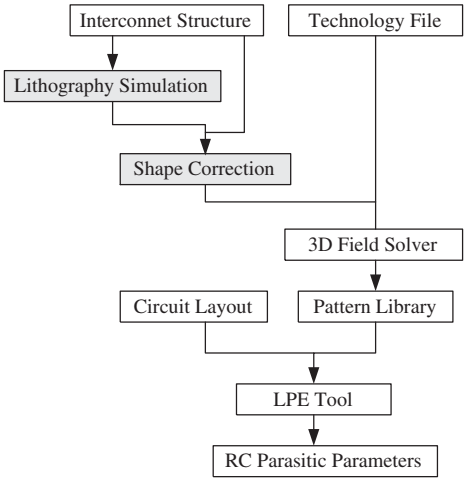


Fig. 5. New LPE methodology

IV. Shape Correction Methodology

In this section, a dynamic programming based algorithm for selecting side wall layers, and a shape correction algorithm are introduced for the irregular shape interconnect capacitance extraction. An algorithm for resistance computation of irregular shapes is also proposed.

A. Side Wall Layer Selection

From extensive simulation, we found that selecting few middle layers (top and bottom layers must exist) from the original lithography simulation output is accurate enough while significantly speeding up the 3D capacitance solver running time. Comparing Fig. 2(b) with Fig. 3(d), where the latter one is generated by taking few middle layers from an original profile with 37 layers and performing our surface discretization algorithm, it takes significantly longer time and bigger memory for 3D BEM based solver to do extraction for the former case than the latter one, while the capacitances of these two cases are almost same. Therefore, it is acceptable to use fewer middle layers and fewer sampling points to approximate the original interconnects.

How to choose the number and the locations of middle layers from the original etching files with acceptable accuracy is a hard problem. It is not affordable to simulate all combinations due to a lots of sampling points and layers. What's more, simply choosing layers with fixed interval (i.e. choose a layer every 5 layer) may be too simple to handle some complex side wall shapes with severe optical distortion. Here, we propose a simple dynamic programming algorithm to choose the number and the location of layers based on error criteria.

Since there are less middle layers in the new approximation shape, every point $A(x, y, z)$ in the original profile has a projected point $A'(x', y', z)$ on the line $C'D'$ of new side wall surface with the same height, where C' is the closest points in the new shape to A with height higher than A, and D' is the closed points in the new shape to A with height lower than A. Note that A' and A could be the same if A is on the selected layer, i.e., $C' = C$ and $D' = D$. A 2D example (cross section of one side wall) is shown in Fig. 6, where realistic 3D cases are analyzed in the implemented algorithm. In this paper, we use the distance of the A to A', $d(A, A')$ as the error function to measure how close our approximation shape to the original shape. Note that, our method is not limited to this error function. Other error functions could be used also, such as $1/d(A, A_r) - 1/d(A', A_r)$, where A_r is a reference point and this function correlates to free space Green's function. Actually, our algorithm is flexible enough to use any error function correlated to the physical location of points.

Suppose the number of layers in the original etching profile is n, and the number of points on each layer is k.

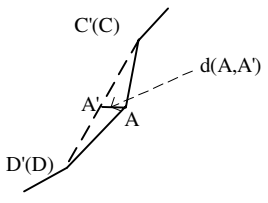


Fig. 6. Original points and projected points in a cross section view of one side wall surface.

Side Wall Layer Selection Problem : Given n layers and k points as described above, user specified error bound ϵ (or user specified number of layers), select m layers, where $m \geq 2$ and must include the first (top) and nth (bottom) layers, such that

$\sum_{A \in S} d(A, A') < \epsilon$ (or minimize $\sum_{A \in S} d(A, A')$ for user specified m), where S is the set of all points in the original layer, and A' is the projected point of A on the side wall surfaces formed by new m layers with the same height.

Side Wall Layer Selection Algorithm: The algorithm is based on dynamic programming. First, we precomputed a $n \times n$ table ER which stores the information of error functions for every two layers. $ER[i, j]$ for $i < j$ is the sum of error function for all points on layers from $i + 1$ to $j - 1$ if layer i and j are directly connected. $ER[j, i] = ER[i, j]$ and $ER[i, i] = 0$. It is easy to see that $ER[i, i+1] = 0$. Note that we only need to compute and store half of the table ER.

Let us define a two-dimensional table T, where each entry $t[i, j]$ is the minimum sum of error functions of points on layers from 1 to j when i middle layers are selected and the last middle layer is located at layer j (which implies the layer structure is 1, ..., j, n). Note that i is from 0 to $n-2$, and j is from 1 to $n-1$. $t[i, j]$ is computed as the following recursive formula

$$t[i,j] = \begin{cases} 0, \text{if } i = 0 \text{ and } j = 1 \\ \infty, \text{if } i \geq j \text{ or } (i = 0 \text{ and } j \neq 1) \\ min_{k=1,\ldots,j-1}(t[i-1,k] + ER[k,j]), \\ \quad \text{if } i > 0 \text{ and } i < j \end{cases} \quad (1)$$

Here is the intuitive explanation how $t[i, j]$ is computed. When we want to choose i middle layers where the last layer is j, we look at all combinations of $i - 1$ middle layers plus a new link between the last layer of $i - 1$ layers and the layer j, and choose the one with minimum error provided that the selection of $i - 1$ layer is optimal. $t[0, 1] = 0$ is obvious from the definition. Since it is not possible to choose i middle layers where the last layer index is less or equal to i, all $t[i, j]$ for $i \geq j$ is infinity. Similar argument for $t[0, j]$ when $j \neq 1$. It is easy to see from Eq. (1) that $t[i, i + 1] = 0$ and $t[1, j] = ER[1, j]$ when $j \neq 1$.

After all $t[i, j]$ entries are computed, the minimum error $ME[i]$ for choosing i middle layers is

$$ME[i] = min_{j=1,\ldots,n-1}(t[i,j] + ER[j,n]), i = 0, \ldots, n-2,$$

which can be treated as $t[i, n]$ from Eq. (1). If the error bound ϵ is given, we select i and corresponding layer assignments such that $ME[i] < \epsilon$ and i is minimum. If the number of layer m is specified, $ME[m]$ directly gives the layer assignment for the minimum error.

The pseudo code of the algorithm is shown in Algorithm 1. The code has taken into consideration that some entries of $t[i, j]$ is infinity. The location of m layers can be found easily with simple back-trace and the code is omitted here due to space limit.

It is not to hard to see that by dynamic programming, the computation time of $t[i, j]$ and $ME[i]$ can be easily done in $O(n^3)$ time and $O(n^2)$ memory. It takes $O(n^3 k)$ time and $O(n^2)$ memory to compute ER table since for each $ER[i, j]$ entry it takes $O(nk)$ to compute the sum of error functions for all points between layer $i + 1$ to $j - 1$, and the projection points need to be recomputed each time for different $ER[i, j]$. Therefore, the total computation time is $O(n^3 k)$ and memory consumption is $O(n^2)$. The optimality of the algorithm under our error function definition is guaranteed due to the optimal substructure of the problem all subsolutions are visited. The detail proof is omitted here due to space constraints.

If we draw a curve with y axis being $ME[i]$ and x axis being i, after removing redundant solutions (if $ME[i] < ME[j]$ and $j > i$, then $ME[j]$ is redundant), it is not surprising that the curve is a monotonically decreasing curve since more layers are selected, less error will be. From extensive experiment, we also found the $ME[i]$ has good correlation with the error of final capacitance matrix, which means our error function is valid. Again, it is possible to use other error functions to computer ER and get better results.

Input: $n * k$ sampling points on n layers, user specified ϵ or m
Output: $m * k$ sampling points on m layers

```
Precompute ER table ;
t[0, 1] = 0 ;
for j = 2 ... n − 1 do
    t[1, j] = ER[1, j] ;
end
for i = 2 ... n − 2 do
    for j = i + 1 ... n − 1 do
        t[i, j] = ER(i, j);
        for k = i + 1 ... j − 1 do
            t[i, j] = min(t[i, j], t[i − 1, k] + ER[k, j];
        end
    end
end
ME[0] = ER[1, n];
for i = 1 ... n − 2 do
    ME[i] = ER[i + 1, n] ;
    for j = i + 2 ... n − 1 do
        ME[i] = min(ME[i], t[i, j] + ER[j, n]) ;
    end
end
return m and the location of m layers based on ME and user
specified ε or m ;
```

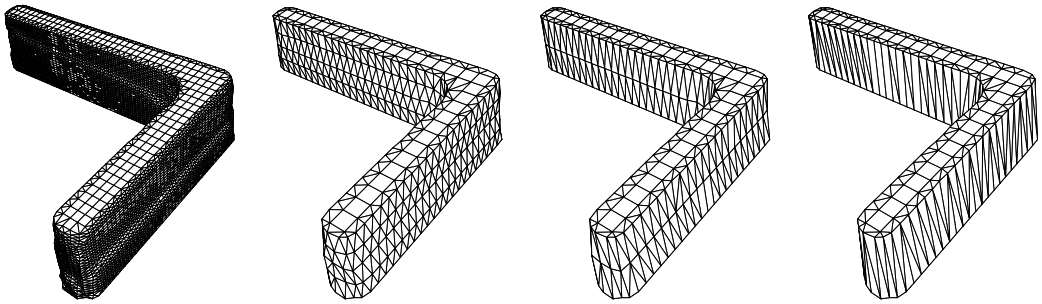
Algorithm 1: Side Wall Layer Selection

To verify our algorithm, Fig. 7 shows an elbow example with different m middle layers selecting from our algorithm.

The comparison results for single elbow are shown in Table III. We found that the result with 5 layers has good accuracy compared with capacitance of the litho/etched one. With the same method, some experimental results are obtained for more other structures, such as signal bus, parallel buses, 1x1 crossing bus, and 2x2 crossing bus. The errors compared to litho/etched profile are also shown in Table III. All of the experiments in this table run on SUN ULTRA SPARCV9 400 MHZ with 2GM memory machine. The following experiments about capacitance extraction also run on the same machine. We found that when the number of the layers is more than 4, both $ME[i]$ curve and capacitance error curves go to flat, which means the approximate capacitance has enough accuracy while the running time and memory have been dramatically reduced.

B. Shape Correction

Even though we can only select few layers from the lithography simulation profile, the conductor shape is still irregular



(a) 37-layer original shape (b) 5-layer approximation (c) 3-layer approximation (d) 2-layer approximation

Fig. 7. One example of side wall layer selection for an elbow-shape conductor

TABLE III

CAPACITANCES ERROR WITH SELECTED M(M=5,3,2) ETCHING LAYERS

	Litho/ Etched 37 layer	5 layer Error (%)	3 layer Error(%)	2 layer Error(%)
Single elbow	-	1.45	1.73	2.30
Single bus	-	0.32	0.72	1.39
Parallel bus	-	1.31	4.80	7.92
1 X 1 bus	-	0.55	1.25	1.94
2 X 2 bus	-	1.14	3.68	5.74
Total time (s)	1404.4	148.4	91.2	72.5
Total memory(MB)	932.3	121.8	75.43	53.84

TABLE IV

CAPACITANCES WITH NEW LPE METHODOLOGY FOR THREE PARALLEL BUSES

Capacitance (aF)	Litho/ Etched	Shape Correction	Error(%)
C_{11}	100.5	101.3	0.79
C_{22}	139.3	140.6	0.93
C_{33}	100.6	101.1	0.50
C_{12}, C_{21}	61.08	61.78	1.15
C_{13}, C_{31}	10.99	11.04	0.45
C_{23}, C_{32}	61.35	61.77	0.68
Time(s)	339.5	2.9	
Memory(MB)	285.6	5.5	

and it can not be handled by current commercial 3D field solver. Shape correction algorithm is introduced here.

The main idea of the shape correction is as follows.

1) Read the original layout profile without process variation and lithography simulation. Keep layout profile in vector E, whose dimension d_E is the number of total boundary edges of the layout profile. For the most selected interconnect pattern, d_E is a small number, i.e., d_E is 4 for the standard bus. Meanwhile, keep lithography simulation results after the side wall selection algorithm described in section IV-A in vector L, whose dimension d_L is the number of selected layers. Based on the previous analysis, we set d_L to be 5 here.
2) For each layer in vector L, find the points in lithography profile with minimum distance to each edge in vector E, and store them into vector F. The dimension of vector F is the same as that of vector E.
3) Fit the boundary wall based on the previous results using least square method (LSM).

The pseudo code for shape correction is omitted due to space limit. The complexity of the algorithm is $O(d_E P)$, where P is the number of the total sampling points on all layers. Note that for selected structures, d_E can be regarded as a constant, and our side wall selection algorithm has reduced P to a relative small number compared to the original litho/etched profile.

Our shape correction algorithm further reduces the size of the input for FastCap. For example, the output shape from lithography simulation is shown in Fig. 8(a), and the output after side wall selection and before fitting the boundary wall with LSM is shown in Fig. 8(b), which is much simpler than before. However, the side wall shape is still not regular, such as rectangles or quadrilaterals. After LSM, we fit the boundary points into known patterns of the standard input format and show the final result in Fig. 8(c). Table IV shows the capacitance values computed by FastCap, as well as the running time and memory usage, for the shape generated by the lithography simulation and shape correction algorithm. The shape correction result shows good accuracy from Table IV. After shape correction, FastCap takes less than 1% time and 3% memory to compute the capacitance. The whole shape correction algorithm is executed on SUN ULTRA SPARCV9 400 MHZ with 2GM memory machine. The total running time of side wall selection and shape correction algorithm is less than 1.5 seconds.

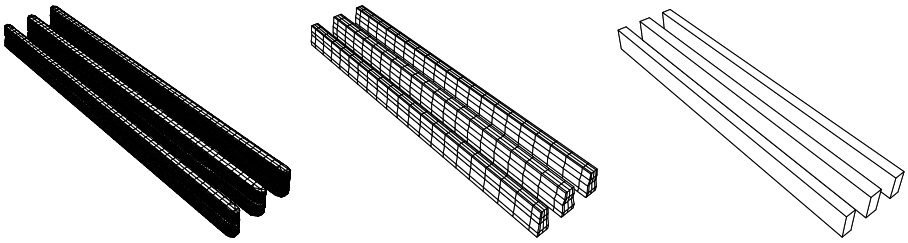
C. Resistance Extraction

In Fig. 2(b), the shape of the lithography simulated interconnect is irregular. In order to accurately compute the resistance of such irregular geometry, we can not directly use the classic equation $R = \rho L/A$, where ρ is resistivity, L is the length of the conductor and A is the area of the cross section.

We discretize the conductor into 3D grids, and build a linear system $GV = I$ [9] based on Kirchoff's Law, where G_i is the element conductor, $V_{i,j,k}$ is the voltage at node i, j, k and I is the independent current source. One model is shown in Fig 9. The linear system is shown as below,

$$\begin{aligned} I \;=\; & (G_1 + G_2 + G_3 + G_4 + G_5 + G_6)V_{i,j,k} \\ & - G_1 V_{i,j-1,k} - G_2 V_{i,j+1,k} - G_3 V_{i-1,j,k} \\ & - G_4 V_{i+1,j,k} - G_5 V_{i,j,k+1} - G_6 V_{i,j,k-1}. \end{aligned}$$

In the equation, $G_i = 1/R_i$. For a regular shape input, all G_i's are the same. But for irregular shape input, each G_i



(a) Original lithography shapes (b) Shapes after side wall layer selection (c) Shapes after shape correction

Fig. 8. One example of shape correction for three parallel buses

could be different. We solve the linear system $GV = I$ to get the node voltage at every grid point. Finally, we can get the average voltage drop along the conductor and use $R = U/I$ to obtain the resistance.

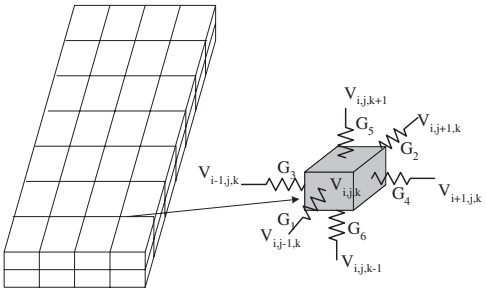


Fig. 9. Resistance computation model.

Table V shows resistance extraction results corresponding to the example shown in Fig. 1. The resistance value based on the original layout profile could have 20% error compared to litho/etched one. Meanwhile, we can observe that our shape correction algorithms are still efficient for resistance extraction, where the error is less than 5%. After shape correction, the conductor profile is regular now. We can use classical equation to obtain the resistance value.

TABLE V
RESISTANCE COMPARISON BETWEEN NEW AND OLD LPE METHODOLOGIES FOR THE EXAMPLE SHOWN IN FIG. 1

Resistance (Ω)	Litho/ Etched	Layout	Error (%)	Shape Correction	Error (%)
R_1	0.29	0.23	20.69	0.30	3.45
R_2	0.23	0.18	21.74	0.24	4.35

D. Inductance Extraction

Table VI gives inductance extraction results corresponding to the example shown in Fig. 1. The inductance values of layout profile and shape correction profile are obtained by FastHenry [10][11]. Based on the results with 10 GHz working frequency in Table VI, we can see that the lithography effect on inductance is insignificant under the current technology. Therefore, we can directly use the inductance of the layout profile.

TABLE VI
INDUCTANCE WITH NEW LPE METHODOLOGY FOR THE EXAMPLE SHOWN IN FIG. 1

Inductance (pH)	Layout Profile	Shape Correction	Error (%)
L_{11}	3.0011	2.9787	0.75
L_{22}	2.2028	2.1834	0.89
L_{12}, L_{21}	1.1732	1.1268	3.95

V. CONCLUSION

In this work, a new LPE methodology is proposed considering lithographic effect. Lithography simulation and shape correction steps including a smart dynamic programming based layer selection scheme are inserted into the traditional LPE methodology to form new LPE methodology. Compared with the traditional methodology, the new methodology will get much more accurate results. The shape correction algorithm significantly reduces the running time of the 3D capacitance solver while keep the good accuracy. Meanwhile, resistance extraction for irregular shape is also presented. Our shape correction algorithm is still efficient for resistance and inductance extraction.

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