Psuedo-Millimeter-Wave Up-Conversion Mixer with On-Chip Balun for Vehicular Radar Systems

Ivan Chee Hong LAI
School of Frontier Sciences
The University of Tokyo
Kashiwa, Japan
Tel : +81 4-7136-3849
Fax : +81 4-7136-3850
e-mail : lai@axcel.k.u-tokyo.ac.jp

Minoru FUJISHIMA
School of Frontier Sciences,
The University of Tokyo
Kashiwa, Japan
Tel : +81 4-7136-3846
Fax : +81 4-7136-3847
e-mail : fuji@k.u-tokyo.ac.jp

Abstract - A low-power, fully integrated 20-26 GHz broadband up-conversion mixer implemented with on-chip Marchand baluns is demonstrated on 90nm CMOS technology in this paper. The baluns employ capacitive coupling between two metal layers and include slotted shields to reduce substrate losses. At 22.1 GHz, the integrated mixer achieves a conversion gain of 2 dB with a maximum power dissipation of only 11.1mW from a 1.2V dc power supply at LO power of 5 dBm.

I Introduction

In the vehicular radar systems operating in the 22-29 GHz frequency range, high frequency up-conversion mixers above 20 GHz are required. Until recent years, CMOS has not been able to achieve this operating frequency and it is necessary to employ compound semiconductors. CMOS technology, besides consuming less power, has the potential to integrate with digital technology. A single-balanced mixer can be used to reduce power consumption because less number of active devices is employed. The single-balanced topology, as used in this work, can also achieve moderate gain and a low noise figure. Less chip area is required since a balun is not required for the IF input, compared to that of the double-balanced mixer. However, this topology has low 1-dB compression point and high input impedance. To our knowledge, existing implementations on CMOS have been limited to 24 GHz with power consumption of 25mW [1]. A fully integrated 20-26 GHz broadband up-conversion mixer with on-chip baluns is demonstrated on 90nm CMOS technology in this paper. The maximum power consumption is 11.1mW from a 1.2V dc supply.

II. Mixer and Balun Design

A. Mixer Design

The mixer topology as shown in Fig. 1 uses a single-balanced design. This design employs a transconductance stage, M1 and switching transistors, M2 and M3. For optimum performance, M1 is biased in the strong inversion and saturation for high g_m. M2 and M3 is sized smaller for reduced noise contributions. The challenge is in the use of the low supply voltage to allow operation. A v_{gs} of 0.67V is used in M1 for maximum g_m, and the v_{th} of M2 and M3 required for switching is 0.35V. As a result, little headroom is left for the signal voltage swing. The mixer circuit operates with an input IF through M1 at a frequency of 2.7 GHz. The differential output RF signal is converted to a single-ended output using a substrate-shielded Marchand-type balun. The balanced LO signal is also provided through a second on-chip balun.

B. Balun Design

The on-chip baluns consist of two multilayered coupled-line sections with slotted substrate shielding for low-losses as shown in Fig. 2. The shield changes the effective permittivity of the balun which consists of composite transmission line structures that allows reduced dimensions due to slow-wave effects [2]. Measurement of the balun test structures terminated directly to 50Ω probe pads demonstrates a broad pass-band with amplitude imbalance within 0.5 dB and phase imbalance within 10 degrees. Although the baluns employed in this mixer circuit do not terminate at 50Ω to the mixer, confidence in the design can be made with the same design software. In Fig. 3, simulation results using the 2.5D simulation software ADS Momentum is shown with the insertion-loss less than 5 dB at the pass-band from 20 GHz to 24 GHz while the phase difference is within 5º from the desired value of 180º. Port 1 refers to the single-ended, while ports 2 and 3 refer to each of the differential ports. The size of the LO and RF baluns are 229μm×229μm and 182μm×212μm, respectively.

III. Experimental Results

The up-conversion mixer was designed and fabricated using a six-metal 90nm CMOS process. Figure 4 shows the micrograph of the fabricated chip. The size is 650μm × 570μm. For the measurements, the LO frequency is varied between 17.3 GHz and 23.3 GHz. This allows an RF output of 20-26 GHz using a 2.7 GHz IF. S-parameter measurements are taken with the circuit bias voltages. Shown in Fig. 5 is the output matching, S_{22}, which has a return loss better than 10 dB for frequencies from 20 GHz to 26 GHz. The matching to LO, S_{11} achieves a minimum of -14.0 dB at 19.4 GHz. Power measurements were taken across the frequency band of interest. The up-conversion mixer exhibits a conversion gain of 2 dB and achieves an input-referred 1-dB compression point of -14.8 dBm. Table I summarizes the performance of the broadband mixer circuit. With emphasis on low power consumption, the performance is comparable to up-conversion mixers fabricated with compound semiconductor technologies.

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V. Conclusions

This work demonstrates a high frequency, fully integrated 20-26 GHz broadband up-conversion single-balanced mixer with on-chip baluns to enable single-ended input and single-ended output. The baluns are constructed with metal 6 and the top pad metal for reduced resistive losses and provide impedance matching to improve conversion gain. Slotted substrate shields are laid under the balun structures to reduce substrate losses. The occupied areas of the baluns are 229μm×229μm and 182μm×212μm for the LO feed and the RF output, respectively. The total die size is 650μm×570μm.

Acknowledgements

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References

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TABLE I. UP-CONVERSION MIXER MEASUREMENTS

Matched RF Frequency	20-26 GHz
IF Frequency	2.7 GHz
Max. Power Gain	2 dB@22.1 GHz
Max. Power Dissipation	11.1mW
IR-RF Isolation	18 dB@22.1 GHz
Input 1-dB Compression Point	-14.8 dBm@22.1 GHz

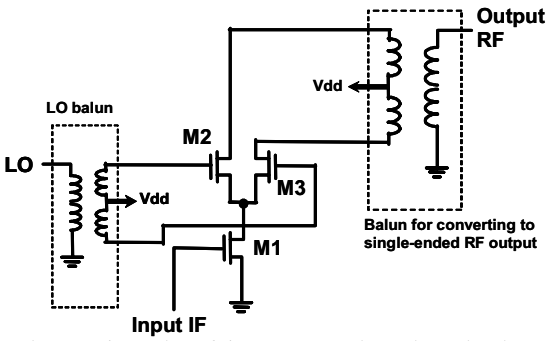

Fig. 1. Schematics of the up-conversion mixer circuit.

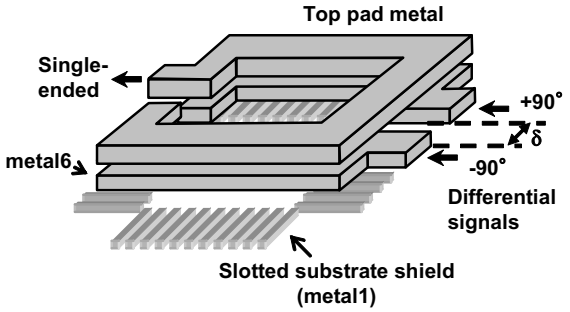

Fig. 2. Multi-layer balun design with substrate shield.

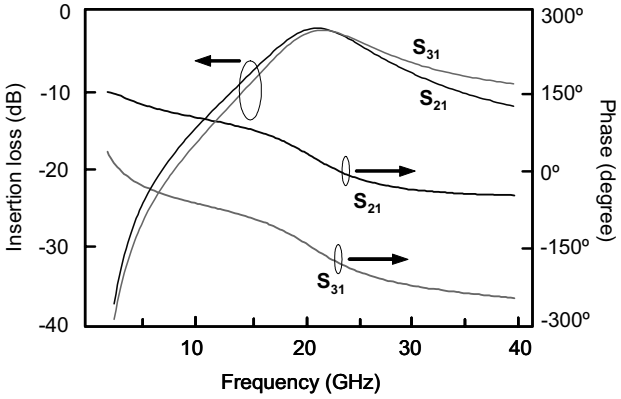

Fig. 3. Simulation results of the output balun using ADS Momentum.

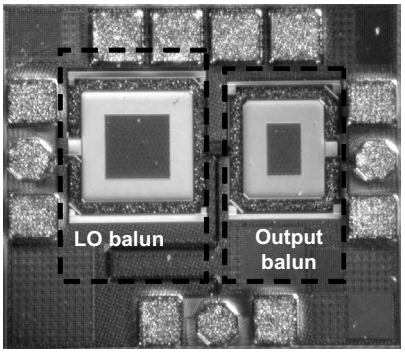

Fig. 4. Micrograph of mixer with on-chip baluns. Chip measures 650μm × 570μm.

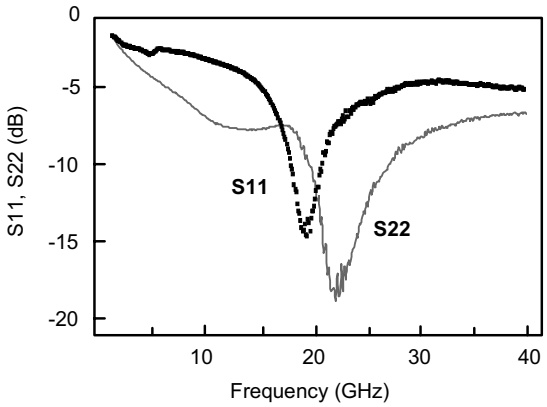

Fig. 5. Measured S11 for LO balun matchings and S22 RF output balun matchings.