

## Designers' Forum

This brandnew event, Designers' Forum, is conceived as a unique program for ASP-DAC to encourage mutual exchange both between and within designers in industry, researchers in the area of EDAs, and EDA developers. Here, designs will be presented focusing on design styles, design issues, and ways to tackle design issues. Panel discussions will also be held for the latest design issues.

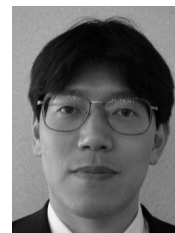
This year, we will have 2 special sessions in ASP-DAC 2006 as follows. 4 presentations related to low power designs, power models, and power estimation frameworks for the real SoC designs will be given by Toshiba, Fujitsu, Hitachi and Renesas, and Samsung in session 5D, "Low Power Design." In session 8D, "Cell processor", 4 presentations will be given focusing on simulations, tests, verifications, power estimation, and design methodology of Cell; and PLL design employed in the Cell processor.

In addition to the special sessions, we will have 2 panel discussions. Session 6D, "Functional Verification -now and future-" will be moderated by Dr. Y. Masubuchi of Toshiba, who has been deeply engaged in the architecture design and verifications of the Cell processor. Three panelists are LSI designers, working for functional verifications in LSI design, and one panelist is from an EDA vendor, developing functional verification tools. Session 9D, "Top 10 design issues seen by LSI designers versus EDA developers", on the other hand, will be moderated by Dr. Y. Hagihara of Sony. Three panelists are managers of SoC and system designs, will focus on the top 10 design issues seen by LSI designers; and 3 panelists are technology officers from 3 major EDA vendors, and they will focus on top 10 design issues seen by EDA developers. Discussions will be led toward the perspectives of the future SoC design issues, comparing with the two top 10 issues seen by both LSI designers and EDA developers.

This Designers' Forum is planned by the Industry Liaison Members of ASP-DAC2006. It is with great pleasure that we acknowledge the contributions to the Designers' Forum, and it is our earnest belief that this forum will promote mutual exchange of designers and EDA researchers and developers, toward nano-meter SoC design issues.



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