# A 0.5-V Sigma-Delta Modulator Using Analog T-Switch Scheme for the Subthreshold Leakage Suppression

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**Abstract - A 0.5-V sigma-delta modulator implemented in a 0.15-µm FD-SOI process with low $V_{TH}$ of 0.1V using analog T-switch (AT-switch) scheme to suppress subthreshold-leakage problems is presented. The scheme is compared with the conventional circuit, which are also fabricated in the same chip. The measurement result demonstrates that the sigma-delta modulator based on AT-switch realizes 6-bit resolution through reducing non-linear leakage effects while the conventional circuit can achieve 4-bit resolution.**

## I Introduction

Recently, low-voltage, low-power yet inexpensive VLSI's are getting focus, and analog building blocks tend to be embedded in scaled digital circuits as a part of SoC implemented with advanced VLSI technology. The International Technology Roadmap for Semiconductors (ITRS) predicts that the threshold voltage ($V_{TH}$) of high-performance logic technology will ever decrease. Hence, techniques for analog circuit implemented with very low-$V_{TH}$ process become more important.

Several sub-1V sigma-delta modulators and ADC's are reported. All are, however, implemented in a high-threshold voltage process [1,2,3]. In this paper, a 0.5-V sigma-delta modulator using analog T-switch (AT-switch) scheme, which can suppress subthreshold leakage in the process with very low $V_{TH}$ of 0.1V, is presented and verified by measurement.

## II. Circuit Design

Fig.1 shows a schematic of a sigma-delta modulator using AT-switch scheme. $M_{1a\sim c}$ and $M_{2a\sim c}$ are the AT-switch that consists of two series-connected MOS's and intermediate voltage controlling MOS. The analog ground is set to $V_{DD}/2$. All MOS switches are driven by non-overlapping clocks whose swing is between $V_{SS}$ to $V_{DD}$. Fig.2 explains why the subthreshold leakage can be suppressed. During the sampling phase, the gate voltage of $M_{3b}$ is set to $V_{SS}$ and that of $M_{3a}$ is set to $V_{DD}$ to cut them off deeply. When the input signal is around $V_{DD}$ the node "A" is set to $V_{IN}$ through $M_{2a}$ and $M_{2b}$. Although $M_{3a}$ is still leaky, the gate-source of $M_{3b}$

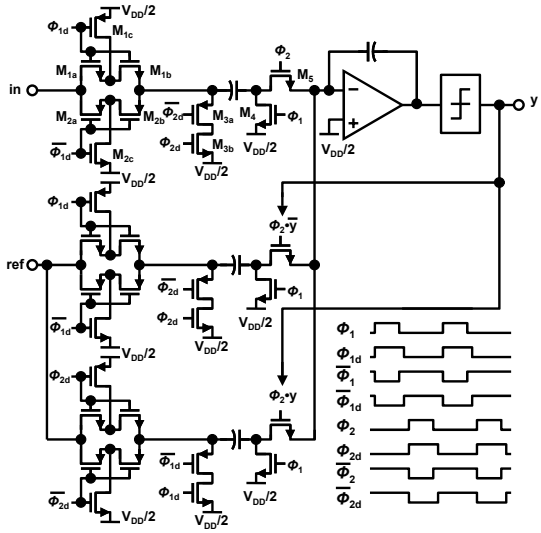


Fig.1. Schematic of a 0.5-V sigma-delta modulator using the AT-switch scheme.

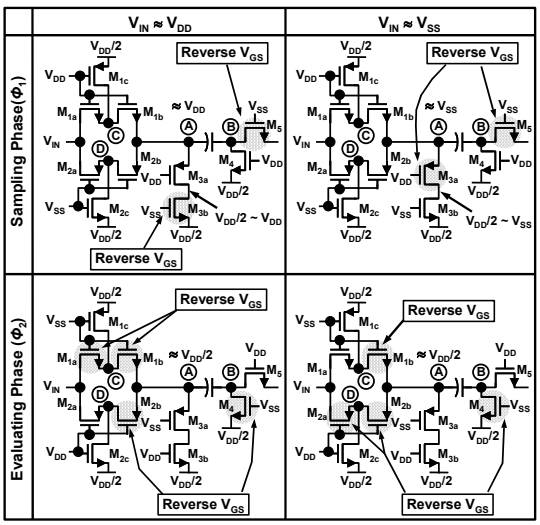


Fig.2. Principle of the AT-switch scheme. Subthreshold leakage is suppressed by reverse-VGS without handling voltage outside the power rails.

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is reversely biased by $V_{DD}/2$ and $M_{3b}$ is completely cut off. When the input signal is around $V_{SS}$, the gate-source of $M_{3a}$ is reversely biased although the $M_{3b}$ is leaky. In this case, $M_5$ is also reversely biased since the node "B" is always set to $V_{DD}/2$ through $M_4$. During the evaluation phase, the gates of $M_{1a}$ and $M_{1b}$ are both set to $V_{SS}$ and the gates of $M_{2a}$ and $M_{2b}$ are set to $V_{DD}$ to cut them off. The node "C" and node "D" are connected to $V_{DD}/2$ in this phase through $M_{1c}$ and $M_{2c}$ respectively. Then, both of the $V_{GS}$ of $M_{1b}$ and $M_{2b}$ are reversely biased and they are deeply cut off even though $M_{1a}$ and $M_{2a}$ are leaky. $M_4$ is also reversely biased since the node "B" is always set to $V_{DD}/2$ through the $M_5$. Since this scheme is insensitive to parasitic capacitances of MOS switches, added parasitic capacitance introduced by the proposed scheme do not affect the operation [4]

## III. Experimental Results

The AT-switch scheme and the conventional scheme are implemented in the same chip. The circuits are operated under 0.5-V supply voltage and at 2-MHz sampling frequency.

Fig.3 demonstrates measured output power spectra. The output spectrum of the conventional scheme is taken at the input level of –7.6dB and the large harmonic tones that degrade SNDR are observed. This is due to the leakage current that introduces non-linear errors. The proposed scheme shows the peak SNDR at the input level of –7.6dB. It is seen that the third order and higher tones are greatly suppressed compared with the conventional circuit.

Fig.4 shows measured SNDR's. The SNDR of the conventional scheme is degraded to 31.5dB, which is below 5-bit resolution, with the power consumption of 71µW. The proposed scheme achieves the peak SNDR of 39.6dB, which realizes more than the 6bit resolution, with the power consumption of 75µW. The peak SNDR and the dynamic range are improved over the conventional approach at the same time. The chip microphotograph of the sigma-delta modulator using the AT-switch scheme is shown in Fig.5 and the area is 130µm×190µm.

## IV. Conclusion

A 0.5-V sigma-delta modulator implemented in a 0.1V-$V_{TH}$ 0.15-µm FD-SOI process using AT-switch scheme is experimentally verified. The modulator using AT-switch realizes 6-bit resolution by reducing non-linear leakage effects caused by the leakage and loss of charge through low-$V_{TH}$ transistors.

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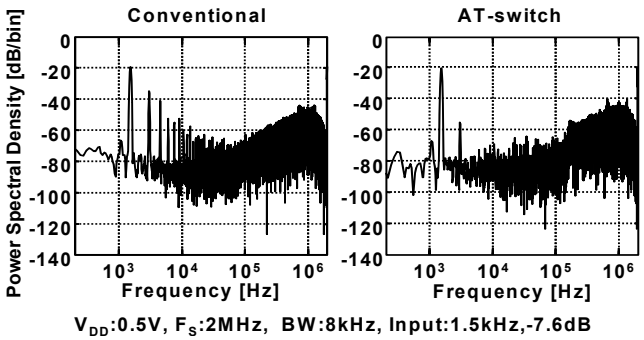


Fig.3. Measured output power spectra of sigma-delta modulators.

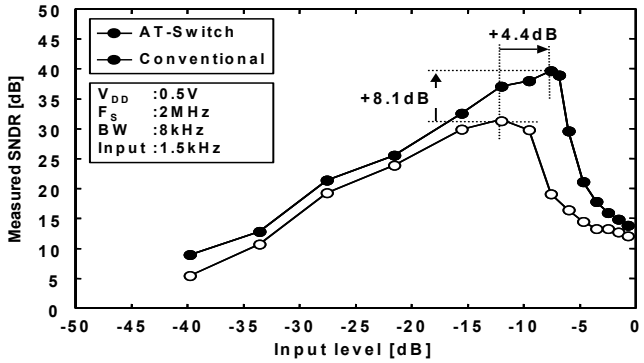


Fig.4. Measured SNDR's.

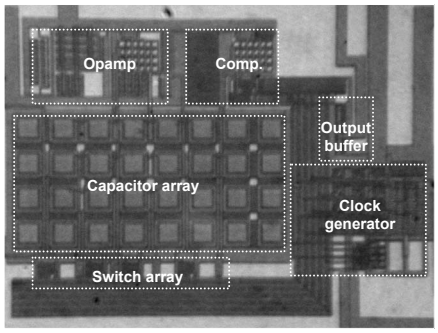


Fig.5. The chip microphotograph of the 0.5-V sigma-delta modulator using AT-switch.