

Optimization of Circuit Trajectories: an Auxiliary Network Approach

Baohua Wang

Dept. of EECS, University of Michigan, Ann Arbor
E-mail: baohuaw@eecs.umich.edu

Pinaki Mazumder

Dept. of EECS, University of Michigan, Ann Arbor
E-mail: mazum@eecs.umich.edu

Abstract—On optimizing circuit trajectories, i.e. continuous paths of circuit parameters, the paper presents an auxiliary network approach, which utilizes Pontryagin’s Minimum Principle. Based on a set of circuit element correspondence rules, the introduced approach establishes an auxiliary network for a given circuit to be optimized, then circuit trajectories are optimized in a process of simulating the given circuit and the auxiliary network. The auxiliary network approach facilitates establishing analytic models in designing high-performance circuits that require fine tuning circuit trajectories. The paper details the theoretical framework of auxiliary network, and provides practical examples of its application in adiabatic circuit design.

I. INTRODUCTION

In designing high-performance circuits, multiple design objectives as diverse as circuit area, timing, power, noise immunity, yield, etc., need be accommodated, which need be aided by the automatic circuit optimization techniques. Traditional optimization concentrated on tuning sets of circuit parameters to maximize circuit performance. The typically considered parameter optimization problem can be described by

$$\text{minimize}_p \int_0^T \Phi(x(t), p, t) dt, \text{ s.t. } \dot{x}(t) = f(x(t), p, t). \quad (1)$$

Here Φ is a cost function, e.g. the square error between the desired transient output of a circuit and its actual output, x is a vector of circuit state variables, T specifies a time duration, and p is a vector of parameters to be tuned, e.g. transistor size, interconnect geometry, etc. The set of circuit state equations have been set as the optimization constraints.

Instead of optimizing circuit parameters, tuning paths of circuit parameters can also significantly improve circuit performance. For example, the voltage waveform that turns on the sense amplifier in a DRAM circuit can be optimized to reduce the sensing time [1]; an adiabatic circuit tunes the power clock waveform to reduce the energy dissipation in charging its loads [2], [3], [4]. This type of optimizations involve tuning different paths or trajectories of circuit parameters, to achieve high performance. Mathematically, a circuit trajectory optimization problem is solved:

$$\begin{aligned} &\text{minimize}_{u(t) \in U} \phi(x(T), T) + \int_0^T \Phi(x(t), u(t), t) dt \\ &\text{s.t. } \dot{x}(t) = f(x(t), u(t), t) \end{aligned} \quad (2)$$

Compared to (1), an optimal vector of time-varying trajectories $u(t)$, for $t \in [0, T]$, instead of a vector of scalar parameters p ,

are chosen from the set of admissible time-varying trajectories U , to minimize the integral cost Φ , plus a cost $\phi(x(T), T)$.

Solving a circuit parameter optimization problem like (1) often employs circuit sensitivity, which can be computed via adjoint network or sensitivity circuit [5, 6]. An example of parameter optimization of VLSI circuits is transistor resizing, which was reported could improve microprocessor performance by as much as 15% [7], [8]. Compared to parameter optimization, optimization of circuit trajectories can improve performance in innovative ways. However circuit trajectory optimization has seldom been investigated.

To solve a circuit trajectory optimization problem as (2), this paper introduces an auxiliary network approach, by utilizing Pontryagin’s Minimum Principle [9]. In the approach, a set of circuit element correspondence rules are used to establish an auxiliary network for the given circuit to be optimized; then the optimal circuit trajectories are solved by simulating the given circuit and the auxiliary network, thus making it possible to employ the state of the art circuit simulation techniques. Auxiliary network also facilitates deriving analytic models in designing high-performance circuits that employ trajectory optimization strategies.

The rest of the paper is organized as follows. Section II introduces a circuit trajectory optimization example, and a solution method of directly employing Pontryagin’s Minimum Principle. Section III presents the theoretical framework of auxiliary network. Section IV gives the applications of auxiliary network in adiabatic circuit design. Section V presents the experimental results.

II. CIRCUIT TRAJECTORY OPTIMIZATION: DIRECT METHOD

This section introduces a circuit trajectory optimization example: power clock optimization, and a solution method of directly using Pontryagin’s Minimum Principle.

A. A Circuit Trajectory Optimization Example

Fig.1 shows two adiabatic circuits: an adiabatic buffer and a stepwise driver [10], [11], and gives a General Adiabatic Multi-driver Model (GAMM). A given adiabatic circuit can be described into the GAMM, by modeling its loads with the GAMM’s Π blocks, and its nonlinear devices with those nonlinear dependent sources G_1, \dots, G_n . In the shown GAMM, node voltages are denoted by capitalized letters, e.g. V_{ks} and \bar{V}_{ks} , while branch voltages are denoted by small letters, e.g. v_s , v_{ks} and v_{rks} . The same convention is used in the rest.

An adiabatic circuit curtails energy dissipation during charging its load by using a timing-varying power clock V_{PC} . Based

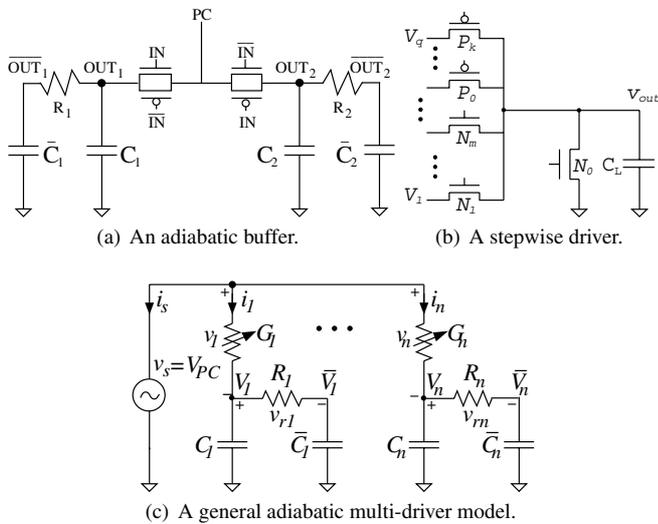


Fig. 1. Two adiabatic circuit examples and a General Adiabatic Multi-driver Model (GAMM).

on the GAMM, the issue of optimizing power clock to minimize the total energy dissipation can be described into the form of (2): replace its cost function Φ by the transient power P :

$$P(V, \bar{V}, V_{PC}, t) = \sum_{k=1}^n \left[(V_{PC} - V_k) i_k(V_{PC}, V_k, t) + \frac{(V_k - \bar{V}_k)^2}{R_k} \right];$$

replace its constraints by circuit equations:

$$\dot{V}_k = f_k \text{ and } \dot{\bar{V}}_k = \bar{f}_k, \text{ for } k = 1, 2, \dots, n, \quad (3)$$

where $f_k = \frac{i_k(V_{PC}, V_k, t)}{C_k} - \frac{(V_k - \bar{V}_k)}{C_k R_k}$ and $\bar{f}_k = \frac{V_k - \bar{V}_k}{R_k C_k}$; set time T to the final charging time; set $\phi(\cdot)$ to zero; the trajectory vector $u(t)$ to be optimized becomes the power clock voltage $V_{PC}(t)$. In other words, one is to shape the power clock waveform, to minimize the total energy dissipation during charging each capacitor from a specified initial voltage to a specified final voltage within a time period T . To solve this power clock optimization problem, having been formulated into (2), the paper employs Pontryagin's Minimum Principle.

B. Pontryagin's Minimum Principle

In using Pontryagin's Minimum Principle (PMP) to solve (2), Hamiltonian H at time t is defined:

$$H(x(t), u(t), \lambda(t), t) = \Phi(x(t), u(t), t) + \lambda(t)^T f(x(t), u(t), t), \quad (4)$$

where λ is a vector of adjoint variables, and $\lambda(T)$ equals to $\partial\phi(x(T), T)/\partial x$, if those partial derivatives exist, otherwise $\lambda(T)$ is unspecified. Then PMP is stated as follows.

Theorem 1 Let $u^*(t) \in U$ be the optimal trajectory, i.e. the solution to (2); $x^*(t)$ the resultant transient circuit waveforms; $\lambda(t)$ the solution to the adjoint equations defined by

$$\dot{\lambda}(t) = - \frac{\partial H(x^*(t), u^*(t), \lambda(t), t)}{\partial x}. \quad (5)$$

Then $u^*(t)$ minimizes H at each time $t \in [0, T]$, that is

$$u^*(t) = \arg \min_{u(t) \in U} H(x^*(t), u(t), \lambda(t), t), \text{ for } t \in [0, T]. \quad (6)$$

C. Solving the Power Clock Optimization Problem by PMP

Introduce two adjoint variable vectors λ and $\bar{\lambda}$, then from (4), Hamiltonian of the power clock optimization problem is

$$H(V, \bar{V}, V_{PC}, \lambda, \bar{\lambda}, t) = P(V, \bar{V}, V_{PC}, t) + \lambda^T f + \bar{\lambda}^T \bar{f}.$$

According to (5), the adjoint equations are: for $k = 1, 2, \dots, n$,

$$\frac{d\bar{\lambda}_k}{dt} = - \frac{\partial H}{\partial \bar{V}_k} = \beta_k = \frac{1}{R_k} \left[2(V_k - \bar{V}_k) - \frac{\lambda_k}{C_k} + \frac{\bar{\lambda}_k}{\bar{C}_k} \right], \quad (7)$$

$$\frac{d\lambda_k}{dt} = - \frac{\partial H}{\partial V_k} = i_k(V_{PC}, V_k, t) - \left(V_{PC} - V_k + \frac{\lambda_k}{C_k} \right) \frac{\partial i_k}{\partial V_k} - \beta_k.$$

Relation (6) implies that the optimal power clock $V_{PC}(t)$ minimizes H . Therefore $\partial H / \partial V_{PC}$ is set to zero, i.e. for each time $t \in [0, T]$,

$$\frac{\partial H}{\partial V_{PC}} = \sum_{k=1}^n \left[i_k(V_{PC}, V_k, t) + \left(V_{PC} - V_k + \frac{\lambda_k}{C_k} \right) \frac{\partial i_k}{\partial V_{PC}} \right] = 0. \quad (8)$$

The previous procedure has set up a system of differential-algebraic equations (DAEs), consisting of (3), (7) and (8). Under a given initial value of λ , or $\lambda(0)$, the power clock solution to the DAEs optimally drives the capacitors from the specified initial voltages to some final voltages. To reach the specified final capacitor voltages, the value of $\lambda(0)$ need be determined in an iterative procedure, e.g. using the Newton-Raphson method.

The previous procedure by directly employing PMP is less convenient, as in trajectory optimization of even a small circuit, all the previously exemplified steps need be conducted to build the DAEs. The other issue is that as several methods exist in formulating circuit equations, e.g. sparse tableau approach and modified nodal analysis, the built DAEs can have different forms, which can hardly spur insight into the underlying trajectory optimization issue. Hence this paper presents an alternative approach of using auxiliary network, which is established for a given circuit from a set of circuit element correspondence rules. Then a circuit trajectory optimization problem is solved by simulating the given circuit and its auxiliary network.

III. THE AUXILIARY NETWORK

This section presents the theoretic framework of auxiliary network for solving the circuit trajectory optimization issue.

A. Trajectory Optimization Template

Problem (2) is extended to a template problem that includes equality constraints:

$$\begin{aligned} & \text{minimize } \phi(x(T), T) + \int_0^T \Phi(x(t), y(t), u(t), t) dt \\ & \text{s.t. } \dot{x}(t) = f(x(t), y(t), u(t), t) \\ & \quad g(x(t), y(t), u(t), t) = 0 \end{aligned} \quad (9)$$

Here g consists of equality constraints, x consists of the regular state variables, and y consists of the other variables.

By Lagrange multiplier theory [9], eliminate g from (9)'s constraints via a Lagrange multiplier vector μ . Then the

template problem is transformed to the same form as (2), with the objective function of (2) replaced by $\phi(x(T), T) + \int_0^T [\Phi(x, y, u, t) + \mu^T g(x, y, u, t)] dt$, and its constraints replaced by $\dot{x}(t) = f(x(t), y(t), u(t), t)$. Then using PMP leads to the optimal conditions for the template problem (9):

$$-\frac{\partial H(x, y, u, \mu, \lambda, t)}{\partial x} = \dot{\lambda}(t) \quad (10a)$$

$$\frac{\partial H(x, y, u, \mu, \lambda, t)}{\partial y} = 0 \quad (10b)$$

$$u^* = \arg \min_{u \in U} H(x, y, u, \mu, \lambda, t) \quad (10c)$$

where H is the Hamiltonian:

$$H(x, y, u, \mu, \lambda, t) = \Phi(x, y, u, t) + \mu^T g(x, y, u, t) + \lambda^T f(x, y, u, t).$$

The paper names (10c) the minimization condition. From the optimal conditions in (10), the paper derives an auxiliary network for a given circuit trajectory optimization problem, by exploiting the regularity of circuit equations.

B. The Set of Circuit Constraints

For a given circuit, Kirchhoff's current and voltage laws are described by $A^T i_b = 0$ and $AV = v_b$. Here A is the branch versus nodal incidence matrix, with each row corresponding to one branch in the circuit, and each column one node in the circuit, excluding the datum node. In a row, +1 corresponds to the source node, and -1 the destination node. i_b and v_b are the vectors of branch currents and voltages, and V the vector of node voltages. For a branch x , i_x and v_x indicate its branch current and voltage.

The branch constitutive relations (BCR's) for the capacitive and inductive branches in the circuit are given by $i_c = C\dot{v}_c$ and $v_l = L\dot{i}_l$, where C and L are the capacitance and inductance matrices. The two sets of BCR's correspond to the f part in (9). BCR's for the other branches are given in the form of $g(i_q, v_q, u, t) = 0$, which correspond to the g part in (9). Here $i_c, i_l, i_q \subset i_b$ and $v_c, v_l, v_q \subset v_b$. Note that a BCR can have the trajectory vector u and time t as its dependent variables.

Incorporate the mentioned circuit constraints consisting of

$$\dot{v}_c = C^{-1}i_c, \dot{i}_l = L^{-1}v_l, A^T i_b = 0, v_b - AV = 0, g(i_q, v_q, u, t) = 0$$

into the template (9), then Hamiltonian H , named the circuit Hamiltonian, results:

$$H = \Phi(i_\Phi, v_\Phi, u, t) + [\lambda_c^T, \lambda_l^T] \begin{bmatrix} C^{-1}i_c \\ L^{-1}v_l \end{bmatrix} + [\mu_i^T, \mu_v^T, \mu_q^T] \begin{bmatrix} A^T i_b \\ v_b - AV \\ g(i_q, v_q, u, t) \end{bmatrix}, \quad (11)$$

where $i_c, i_q, i_\Phi \subset i_b$, $v_l, v_q, v_\Phi \subset v_b$ and $i_c \cap i_q, v_l \cap v_q = \emptyset$. i_Φ and v_Φ are branch currents and voltages dependent by cost function Φ . u is the trajectory vector to be optimized, μ the vector of Lagrange multipliers, and λ the vector of adjoint variables.

The following derives the auxiliary network.

C. The Topology of the Auxiliary Network

Firstly determine the topology of the auxiliary network. From the circuit Hamiltonian H in (11), one has $\frac{\partial H}{\partial V} = -A^T \mu_v$. Then applying (10b) for node voltage vector V leads to the optimal condition $\frac{\partial H}{\partial V} = -A^T \mu_v = 0$. Rename μ_v to \hat{i}_b , and also define a branch voltage vector \hat{v}_b by $\hat{v}_b = A\hat{V}$, i.e.

$$A^T \hat{i}_b = 0 \quad \text{and} \quad \hat{v}_b = A\hat{V}, \quad (12)$$

where \hat{V} is the renaming of μ_i to manifest a vector of node voltages, and renaming μ_v to \hat{i}_b is to manifest a vector of branch currents.

Conclusion 1 Vectors \hat{V} , \hat{v}_b and \hat{i}_b , by satisfying (12), correspond to the vectors of node voltages, branch voltages and currents for an auxiliary network that has the same topology as the circuit to be optimized.

Since a circuit and its auxiliary network have the same topology, the same branch names are used in the two circuits. Next step is to determine the BCR's of the constructed auxiliary network, from the optimal conditions in (10).

D. The Capacitive and Resistive Branches

For the capacitive branches c in the original circuit, assume $v_c \cap v_\Phi, i_c \cap i_\Phi = \emptyset$ (these can always be satisfied with some simple circuit transformations). Differentiate the circuit Hamiltonian H in (11) with respect to i_c and v_c :

$$\frac{\partial H}{\partial v_c} = \frac{\partial \mu_v^T v_b}{\partial v_c} = \hat{i}_c \quad \text{and} \quad \frac{\partial H}{\partial i_c} = C^{-1} \lambda_c + \frac{\partial \mu_i^T A^T i_b}{\partial i_c}.$$

$\frac{\partial H}{\partial i_c}$ can then be simplified as $\frac{\partial H}{\partial i_c} = C^{-1} \lambda_c + \hat{v}_c$, since $\frac{\partial \mu_i^T A^T i_b}{\partial i_c} = \frac{\partial (A\mu_i)^T i_b}{\partial i_c} = \frac{\partial \hat{v}_b^T i_b}{\partial i_c} = \hat{v}_c$. Optimal condition (10a) implies $\dot{\lambda}_c = -\frac{\partial H}{\partial v_c}$, and (10b) implies $\frac{\partial H}{\partial i_c} = 0$, hence, $\dot{\lambda}_c = -\hat{i}_c$ and $C^{-1} \lambda_c + \hat{v}_c = 0$. Then it follows that $\hat{i}_c = C\hat{v}_c$.

Conclusion 2 For the capacitive branches c in the original circuit, branches c in the auxiliary network remain as capacitive with BCR's given by $\hat{i}_c = C\frac{d\hat{v}_c}{dt}$.

Consider a resistive branch r in the original circuit, whose BCR can generally be given by $g_r(v_r, u, t) - i_r = 0$. Denote the Lagrange multiplier for this BCR as μ_{qr} , a component of μ_q in (11). Differentiate the circuit Hamiltonian H with respect to i_r and v_r :

$$\frac{\partial H}{\partial i_r} = \hat{v}_r - \mu_{qr} + \frac{\partial \Phi}{\partial i_r} \quad \text{and} \quad \frac{\partial H}{\partial v_r} = \hat{i}_r + \mu_{qr} \frac{\partial g_r}{\partial v_r} + \frac{\partial \Phi}{\partial v_r}.$$

Since optimal condition (10b) implies $\frac{\partial H}{\partial i_r} = 0$ and $\frac{\partial H}{\partial v_r} = 0$,

Conclusion 3 Corresponding to a resistive branch r in the original circuit, of BCR given by $g_r(v_r, u, t) - i_r = 0$, branch r in the auxiliary network has its BCR specified with $\hat{i}_r = -\left(\hat{v}_r + \frac{\partial \Phi}{\partial i_r}\right) \frac{\partial g_r}{\partial v_r} - \frac{\partial \Phi}{\partial v_r}$.

If the cost function Φ does not depend on branch current i_r and branch voltage v_r , branch r in the auxiliary network is simply a linear resistor of conductance $-\frac{\partial g_r}{\partial v_r}$.

E. The Dependent Source Branches

Consider a dependent source example: the voltage controlled voltage source (VCVS), with controlling branch 1 and controlled branch 2. The BCR's of the two branches are given by $i_1 = 0$ and $g_2(v_1, X) - v_2 = 0$, with X denoting any other dependent variables. The Lagrange multipliers for the two BCR's are μ_{q1} and μ_{q2} , which are components of μ_q in (11). Assume $i_1 \cap i_\Phi$, $i_2 \cap i_\Phi$, $v_1 \cap v_\Phi$ and $v_2 \cap v_\Phi$ are empty set \emptyset , otherwise use simple circuit transformations to make the assumptions true. Optimal condition (10b) implies the partial derivatives of circuit Hamiltonian H with respect to i_1 , v_1 , i_2 and v_2 are zero, hence,

$$\begin{aligned} \frac{\partial H}{\partial i_1} = \hat{v}_1 + \mu_{q1} = 0, \quad \frac{\partial H}{\partial v_1} = \hat{i}_1 + \mu_{q2} \frac{\partial g_2}{\partial v_1} = 0, \\ \frac{\partial H}{\partial i_2} = \hat{v}_2 = 0, \quad \frac{\partial H}{\partial v_2} = \hat{i}_2 - \mu_{q2} = 0. \end{aligned}$$

Conclusion 4 *a VCVS element in the original circuit corresponds to a CCCS element, or a current controlled current source, in the auxiliary network, with the roles of "controlling" and "controlled" exchanged. For a branch controlled by multiple sources in the original circuit, each controlling branch in the original circuit will correspond to a controlled source branch in the auxiliary network.*

For nonlinear storage elements in the original circuit, the corresponding BCR's in the auxiliary network can be derived by using the charge or flux representations of BCR's. Table I shows the derived circuit element correspondence rules, the Lagrange multipliers and the adjoint variables. In the table, a Lagrange multiplier with subscript qx indicates it associates to branch x 's BCR.

The auxiliary network has incorporated the first two set of optimal conditions in (10). It can be conveniently established from the derived circuit element correspondence rules. In principle, the auxiliary network customizes the optimal conditions in (10), by exploiting the regularity of circuit equations.

F. Discussions on Auxiliary Network

A circuit trajectory optimization problem can be solved by simulating the original circuit and its auxiliary network, meantime imposing minimization condition (10c). For a typical circuit trajectory optimization problem that has specified the initial and final voltages/currents of the storage elements, the optimal trajectories can be found by an iterative procedure shown in Fig.2.

In certain trajectory optimization cases that the terminating state for a storage element can be in a specified interval, instead of a fixed value, Lagrange multiplier theory [9] can be employed to formulate a template problem. Usually changing terminating conditions only requires modifying some sources in the auxiliary network, and does not affect its circuit element types.

In using auxiliary network for circuit trajectory optimization, timing-varying circuits need be simulated. Simulating timing-varying circuits is also required in circuit parameter optimization problems, when circuit sensitivities are computed using adjoint network or sensitivity circuit [5, 6].

1. The initial voltages/currents for the storage elements in the auxiliary network are guessed first.
2. Simulate the original circuit and its auxiliary network under the given initial states for the storage elements in both circuits.
3. At every simulation time step t , the optimization trajectory vector $u(t)$ is determined by the minimization condition (10c).
4. At the final simulation time T , if the reached voltages or currents for those storage elements in the original circuit match their specified values, the optimal trajectories are found. Otherwise, modify the initial voltage/current values using the Newton-Raphson method, and go to Step 2 to begin the next run of simulation.

Fig. 2. The auxiliary network approach for circuit trajectory optimization.

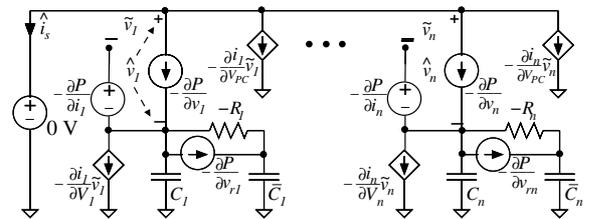


Fig. 3. The auxiliary network for the GAMM.

IV. THE AUXILIARY NETWORK APPLICATIONS

This section demonstrates the applications of auxiliary network in adiabatic circuit optimization.

A. Power Clock Optimization

The power clock optimization problem in Section II is again solved, however, by utilizing the auxiliary network of the GAMM in Fig.1(c). The cost function Φ in the template problem (9) becomes the transient power P , represented with branch voltages and currents by $P = \sum_{k=1}^n (v_k i_k + v_{rk}^2 / R_k)$.

Fig.3 shows the auxiliary network of the GAMM, established from the circuit element correspondence rules in Table I. In the auxiliary network, the linear resistors and nonlinear dependent sources in the original circuit become negative linear resistors and dependent sources, the power clock source in the original circuit changes to a voltage source of magnitude $-\frac{\partial P}{\partial i_s}$, i.e. the zero voltage source input in Fig.3, and the capacitors remain. When $\frac{\partial i_k}{\partial v_{PC}} = -\frac{\partial i_k}{\partial v_k}$, the auxiliary network will be simpler.

According to the minimization condition (10c), V_{PC} minimizes the circuit Hamiltonian H , defined in (11). Therefore $\frac{\partial H}{\partial V_{PC}} = 0$. Since only item $\mu_{qs}(v_s - V_{PC})$, which corresponds to the power clock source branch, relates to V_{PC} in the circuit Hamiltonian H , a simplified minimization condition results

$$\frac{\partial H}{\partial V_{PC}} = -\mu_{qs} = \hat{i}_s = 0. \quad (13)$$

The auxiliary network in Fig.3 and the minimization condition (13) can be verified are simplified forms of the optimal conditions given by (7) and (8). In general, the optimal

TABLE I
CIRCUIT ELEMENT CORRESPONDENCE RULES IN ESTABLISHING A CIRCUIT'S AUXILIARY NETWORK.

Elements & BCR's in Original Circuit		Elements & BCR's in Auxiliary Network		λ or μ
C	$i_c = C \frac{dv_c}{dt}$	C	$\hat{i}_c = C \frac{d\hat{v}_c}{dt}$	$\lambda_c = -C\hat{v}_c$
L	$v_l = L \frac{di_l}{dt}$	L	$\hat{v}_l = L \frac{d\hat{i}_l}{dt}$	$\lambda_l = -L\hat{i}_l$
R	$i_r = g_r(v_r, u, t)$	-	$\hat{i}_r = -\left(\hat{v}_r + \frac{\partial\Phi}{\partial i_r}\right) \frac{\partial g_r}{\partial v_r} - \frac{\partial\Phi}{\partial v_r}$	$\mu_{qr} = \hat{v}_r + \frac{\partial\Phi}{\partial i_r}$
VS	$v_s = vs(u, t)$	VS	$\hat{v}_s = -\frac{\partial\Phi}{\partial i_s}$	$\mu_{qs} = -\hat{i}_s$
CS	$i_s = cs(u, t)$	CS	$\hat{i}_s = -\frac{\partial\Phi}{\partial v_s}$	$\mu_{qs} = -\hat{v}_s$
VCVS	$i_1 = 0 \quad v_2 = g_2(v_1, X)$	CCCS	$\hat{v}_2 = 0 \quad \hat{i}_1 = -\hat{i}_2 \frac{\partial g_2}{\partial v_1}$	$\mu_{q1} = -\hat{v}_1 \quad \mu_{q2} = \hat{i}_2$
VCCS	$i_1 = 0 \quad i_2 = g_2(v_1, X)$	VCCS	$\hat{i}_2 = 0 \quad \hat{i}_1 = -\hat{v}_2 \frac{\partial g_2}{\partial v_1}$	$\mu_{q1} = -\hat{v}_1 \quad \mu_{q2} = \hat{v}_2$
CCVS	$v_1 = 0 \quad v_2 = g_2(i_1, X)$	CCVS	$\hat{v}_2 = 0 \quad \hat{v}_1 = -\hat{i}_2 \frac{\partial g_2}{\partial i_1}$	$\mu_{q1} = -\hat{i}_1 \quad \mu_{q2} = \hat{i}_2$
CCCS	$v_1 = 0 \quad i_2 = g_2(i_1, X)$	VCVS	$\hat{i}_2 = 0 \quad \hat{v}_1 = -\hat{v}_2 \frac{\partial g_2}{\partial i_1}$	$\mu_{q1} = -\hat{i}_1 \quad \mu_{q2} = \hat{v}_2$

conditions for a circuit trajectory optimization problem can have various forms, depending on how the circuit equations for the original circuit are established, e.g. by sparse tableau approach, nodal analysis, modified nodal analysis, etc. Auxiliary network, however, physically implements the optimal conditions for a circuit trajectory optimization problem, and has only one configuration. The auxiliary network can lead to more simplified optimal conditions, compared to the previous direct method.

B. Transistor Sizing for Stepwise Driver

For the stepwise driver in Fig.1(b), constant power supplies V_1, \dots, V_q continuously deliver charges to its load, by sequentially turning on transistors $N_1 \dots P_k$. At any time, only one transistor is made on, by applying a short voltage pulse on its gate. Fig.4(a) shows the stepwise driver model, which uses power clock $V_{PC}(t)$ to describe the effective supply voltage produced by V_1, \dots, V_q , and G_r to model the on-transistor.

Under fixed supply voltages V_1, \dots, V_q , each transistor in the stepwise driver can be sized to minimize the total energy dissipation during charging the load to voltage V_{DD} within time period T . This sizing issue can be formulated as a circuit parameter optimization problem. However the paper formulates it as a trajectory optimization problem, to be solved by the auxiliary network approach.

The width, drain-source voltage drop and driving current of the transistor that charges the loading capacitor at time t are denoted by continuous functions $w(t)$, $v_r(t)$ and $i_r(t)$, respectively. As shown in Fig.4(a), the supply voltage at time t is denoted by a continuous function $V_{PC}(t)$, which closely approximates the effective supply voltage produced by V_1, \dots, V_q . Similarly $w(t)$ is a close approximation to the time-varying widths of the on-transistors in $N_0 \dots P_k$.

Without loss of generality, assume that the transistor driving current is proportional to its width, i.e. G_r 's BCR is given by $w(t)g_r(V_{out}(t), t) - i_r(t) = 0$, where $g_r(\cdot)$ denotes the driving current of the reference transistor. The energy consumed in turning on all the driving transistors is modeled as $\frac{N}{T} \int_0^T \alpha V_{DD} w(t) dt$, where α is a factor relating gate width to the energy consumed in turning on it, and N is the number of transistors to be sized. The objective function of transistor sizing is the total energy dissipation, given by

$$\int_0^T \Phi(\cdot) dt = \int_0^T \left[v_r(t) i_r(t) + \frac{\alpha N V_{DD}}{T} w(t) \right] dt \quad (14)$$

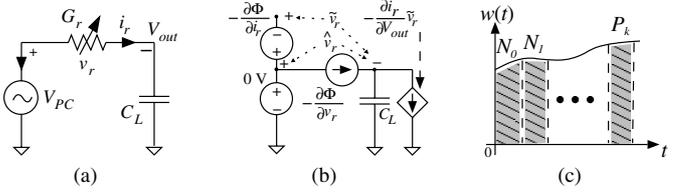


Fig. 4. Transistor sizing of the stepwise driver: (a).Continuous time-domain circuit model; (b).The auxiliary network; (c).The implementation of transistor sizing.

Fig.4(b) shows the auxiliary network, established from the circuit element correspondence rules in Table I. Using the minimization condition (10c) leads to $\frac{\partial H}{\partial w} = \frac{\partial\Phi}{\partial w} + \mu_{qr} g_r(V_{out}, t) = 0$, where μ_{qr} is the Lagrange multiplier associated to G_r 's BCR, and $\mu_{qr} = \tilde{v}_r$. The minimization condition is simplified to

$$\tilde{v}_r g_r(V_{out}, t) = -\frac{\alpha N V_{DD}}{T}. \quad (15)$$

The approach in Fig.2 can then be employed to obtain the optimal trajectory of transistor width $w(t)$. In employing the approach, the initial voltage for C_L in the auxiliary network need be iteratively updated, to satisfy the two voltage conditions $V_{out}(0) = 0$ and $V_{out}(T) = V_{DD}$ for C_L in the original circuit. In actually sizing the transistors, $w(t)$ is broken into N pieces, and each transistor in the stepwise-driver has its width sized to the average value of $w(t)$ in the corresponding piece, as illustrated by Fig.4(c). In [11], rules of thumb are given for sizing transistor in the stepwise driver. These rules, however, assume a uniform power supply voltage distribution, i.e. $V_{PC}(t)$ is a ramp voltage source, as the voltage increment in each step is a constant.

V. EXPERIMENTAL RESULTS

First the paper gives an example of power clock optimization of an adiabatic buffer. The tested adiabatic buffer is modeled by the GAMM in Fig.1(c), with only one driving block included, i.e. using G_1 to denote one of the transmission gates, and using C_1 , R_1 and \bar{C}_1 to model the active driving block of the adiabatic buffer. Consequentially the auxiliary network in Fig.3 need include only one block. Here $R_1 = 200 \Omega$ and $C_1 = \bar{C}_1 = 30$ fF. The paper used $0.13 \mu\text{m}$ MOSFET models.

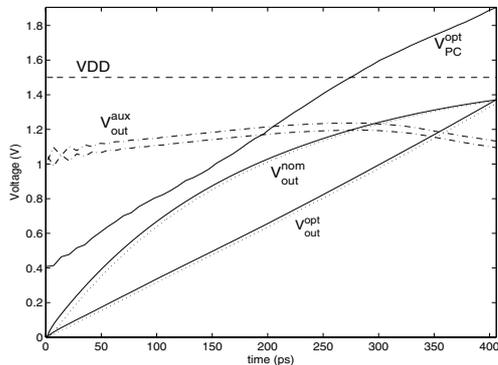


Fig. 5. An example of power clock optimization for an adiabatic buffer.

TABLE II
MULTI-DRIVER POWER CLOCK OPTIMIZATION EXAMPLES.

Name	\hat{C} (fF)	\hat{R} (Ω)	\hat{C} (fF)	P (mW)	OP(mW)	Improv.
Cir1	136.9	70.7	254.2	0.429	0.200	53.2%
Cir2	185.7	169.8	188.8	0.411	0.208	49.3%
Cir3	151.8	60.8	258.9	1.035	0.507	50.9%
Cir4	163.4	46.6	230.6	2.034	1.102	45.8%
Cir5	125.2	76.6	206.6	0.547	0.392	28.3%
Cir6	185.3	181.0	199.1	0.969	0.493	49.1%
Cir7	126.8	120.8	154.1	0.710	0.383	46.1%
Cir8	225.3	63.2	320.0	0.895	0.529	40.9%

Fig.5 shows the simulation results. V_{PC}^{opt} denotes the optimal power clock obtained using the approach in Fig.2. V_{out}^{aux} indicates the output voltages of the two capacitors in the auxiliary network. V_{out}^{opt} indicates the output voltages of the two capacitors in the original circuit when driven by V_{PC}^{opt} , while V_{out}^{nom} indicates the output voltages, when the circuit is driven by a 1.5 V VDD . The chosen time duration T is 406 ps. Using the optimal power clock leads to an average power consumption of $106.6 \mu\text{W}$, while using the constant supply leads to a value of $164.6 \mu\text{W}$, which is 54.4% more than the optimal solution.

Table II shows the power clock optimization results for the GAMM with more than two driving blocks. In the table, \hat{C} , \hat{R} and \hat{C} are the average values of the Π -load parameters for each tested circuit. P denotes the average power consumption in charging the loads, by using a constant power supply to drive the tested circuit, while OP denotes the value, by using the optimal power clock. As indicated by the last column, around 25% to 50% power consumption reductions were observed by using the optimal power clocks.

Fig.6 shows the results of using auxiliary network in transistor sizing for a stepwise driver. The driver has a 150 fF load that need be charged to 1.5 V in 0.6ps. Instead of using the ramp source in [11], the paper uses a 2 V 300 MHz sinusoidal power clock source. The driver has five stages, therefore 5 driving blocks need be sized. V_{out}^{opt} is the output voltage of the driver under the optimal transistor sizing. V_{out}^{aux} is the output voltage of the capacitor in the auxiliary network, which is shown in Fig.4(b). $w(t)$ in the rightmost diagram is the optimal transistor sizing in the time domain. It uses a unit driving block as the reference. This continuous sizing curve need be transformed into 5 pieces for the 5 blocks as illustrated in Fig.4(c).

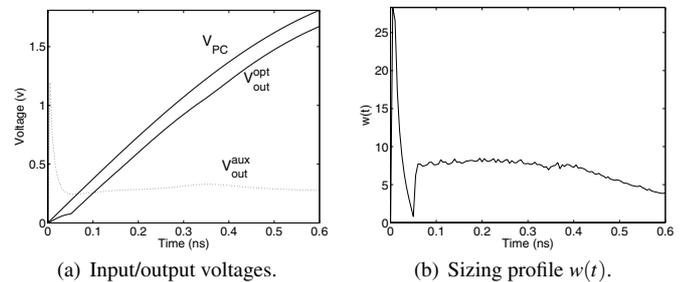


Fig. 6. An example of stepwise driver transistor sizing.

VI. CONCLUSIONS

On circuit trajectory optimization issue, the paper introduced an auxiliary network approach, by utilizing Pontryagin's Minimum Principle. By the approach, a given circuit's auxiliary network is established from a set of circuit element corresponding rules; then the optimal trajectories are found by a process of simulating the given circuit and its auxiliary network. The approach was demonstrated more convenient than the method that directly employs Pontryagin's Minimum Principle to establish DAEs. It can lead to more simplified optimal conditions. Auxiliary network facilitates the establishment of analytical models in designing high-performance circuits that require optimizing circuit trajectories. The paper demonstrated the application of auxiliary network in optimizing adiabatic circuits.

REFERENCES

- [1] N. Wang, "On the design of mos dynamic sense amplifiers," *IEEE Trans. Circuits Syst.*, vol. 29, no. 7, pp. 467–477, Jul. 1982.
- [2] W. Athas, L. Svensson, J. Koller, N. Tzartzanis, and E. Ying-Chin Chou, "Low-power digital systems based on adiabatic-switching principles," *IEEE Trans. VLSI Syst.*, vol. 2, no. 4, pp. 398–407, Dec. 1994.
- [3] A. Dickinson and J. Denker, "Adiabatic dynamic logic," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 311–315, Mar. 1995.
- [4] B. Wang and P. Mazumder, "On optimality of adiabatic switching in mos energy-recovery circuit," in *Proc. IEEE Int. Symp. Low-Power Electronics and Design*, Aug. 2004, pp. 236–239.
- [5] S. W. Director and R. A. Rohrer, "The generalized adjoint network and network sensitivities," *IEEE Trans. Circuit Theory*, vol. 16, no. 3, pp. 318–323, Aug. 1969.
- [6] D. Hocevar, P. Yang, T. Trick, and B. Epler, "Transient sensitivity computation for mosfet circuits," *IEEE Trans. Computer-Aided Design*, vol. 4, no. 4, pp. 609–620, Oct. 1985.
- [7] C. Visweswariah and A. Conn, "Formulation of static circuit optimization with reduced size, degeneracy and redundancy by timing graph manipulation," in *Proc. IEEE Int. Conf. Computer-Aided Design*, Nov. 1999, pp. 244–251.
- [8] G. Northrop and P-F. Lu, "A semi-custom design flow in high-performance microprocessor design," in *Proc. Design Automation Conference*, June 2001, pp. 426–431.
- [9] D. P. Bertsekas, *Dynamic Programming and Optimal Control*, 2nd ed. Athena Scientific, 2001.
- [10] M. Alioto and G. Palumbo, "Power estimation in adiabatic circuits: a simple and accurate model," *IEEE Trans. VLSI Syst.*, vol. 9, no. 5, pp. 608–615, Oct. 2001.
- [11] L. Svensson and J. Koller, "Driving a capacitive load without dissipating fcv^2 ," in *Proc. IEEE Int. Symp. Low-Power Electronics and Design*, Oct. 1994, pp. 100–101.