A Built-in Power Supply Noise Probe for Digital LSIs

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1. Introduction

Dynamic power-supply noise has emerged as a critical piece of low voltage designs in current 130-nm and coming sub-100-nm CMOS technologies. On-chip measurements of dynamic power-supply and ground distributions within a large scale digital circuit can provide precious knowledge for establishing reliable design guides of power-supply systems[1]. This paper introduces a design example of a standard logic cell based digital circuit incorporating a built-in noise detection technique[2].

2. Design of built-in noise detector

Figure 1(a) shows a built-in power supply noise probing architecture. Power supply and ground noises in a digital circuit often show strong position dependences arising from the interaction of time-varying digital activity distributions and frequency-domain transfer properties of on-chip and off-chip parasitic impedance notworks. The architecture enables to profile the time-domain variations of noise intensity as well as the frequency-domain emphasis of noise distributions in power-supply/ground grids. A noise detector structure given in Figure 1(b) fits this purpose, consisting of a source follower (SF) that senses noise voltage and a transconductance transistor (Gm) that converts SF's output voltage to a current signal read externally as Iout. Because of the small device count in this simple front-end structure, the size of a detector is comparable to a standard flip-flop cell and thus placed within a cell row of a standard cell-based digital circuit.

Detailed design of noise detector circuits is shown in Figure 2. In addition to a source follower ($M1, M2$) and a single MOSFET common-source amplifier ($M3$), switch MOSFETs for shuttering by signal *SHU*, $M4$, and for selective activation by signal *SEL*, $M5, M6, M7$, are provided.

The source followers (SF) of n-channel and p-channel senses voltage fluctuation on the nearest digital power-supply *DVDD* and ground *DGND* wirings, respectively, and the common-source amplifier continuously translates it to a current-mode noise signal that is transmitted on a shared current bus *IBUS* and then read out through a current mirror by an external oscilloscope with a termination resistor. One of the detectors sharing *IBUS* can be activated at the same time while all the others are cut off.

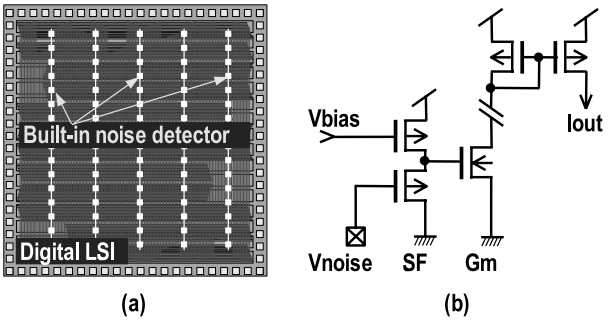

Figure 1: (a) Chip architecture incorporating built-in noise probing technique and (b) SF+Gm noise detector.

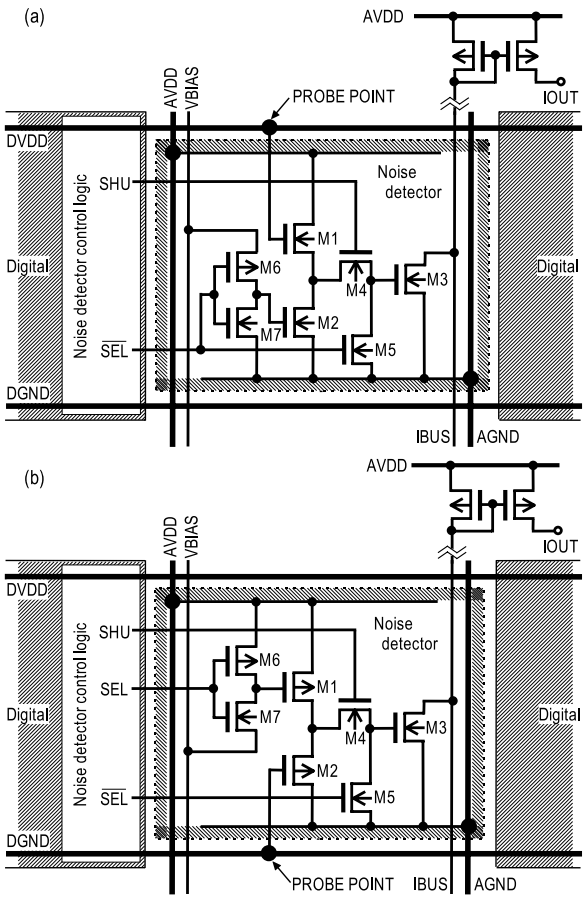

Figure 2: Built-in noise detector circuits for probing (a) power-supply and (b)ground wirings.

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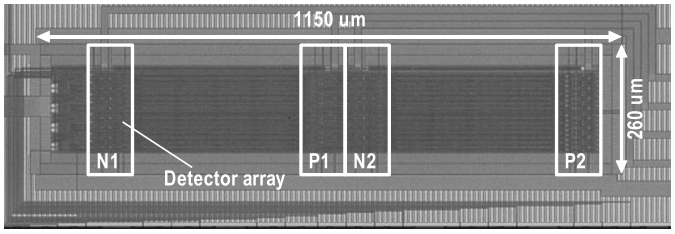

Figure 3: Magnified chip photograph.

The physical layout of the detector can be adjusted to that of a standard logic cell library and its area can be comparable with a few DFF cells.

3. Measurements

A test chip was prepared for the built-in detectors. Two pairs of n-type and p-type detectors for 1.8-V digital circuits were designed with 2.5-V and 1.8-V MOSFETs in a 0.18-μm CMOS, 5LM, multi-oxide, triple-well on P-type bulk substrate technology, where the sizes of MOSFETs were chosen to obtain the noise measurement bandwidth and gain of roughly 1 GHz and 1.0, respectively. A magnified photo of a test chip is given in Figure 3.

Noise waveforms on power-supply and ground rails by the built-in noise detector located in the middle of the 12-th cell row are shown in Figure 4, where a shift register in the test chip was selectively activated. Negative drops on power-supply wirings right after both rise and fall edges of the clock signal are dynamic noises resulting from the switching operations of DFF cells, along with positive counterparts on ground wirings.

Figure 5 extracts the heights of voltage drop at a rise clock edge corresponding to roughly 3.125 ns in Figure 4, where Vdd_drop shows negative peaks measured from 1.8 V while Vgnd_drop gives positive peaks from 0.0V. The location of an active shift register in the 32 logic cell rows is identified by the cell-row number. Both gain-calibrated 2.5-V and 1.8-V detectors show consistent results, which proves the certainty of the built-in noise detection technique.

Observations show that Vdd_drop is larger than 50 mV when a shift register in any cell row is active, and takes the maximum when that in the same 12-th cell row as the active built-in detector is active. On the other hand, Vgnd_drop is normally negligible other than the shift register at 11-th and/or 12-th cell row are active, which both share the ground wiring that the detector is probing. The significantly localized distribution found in ground noise is due to the presence of a substrate.

4. Conclusions

The design of compact noise detector circuitry that could be embedded and arrayed within a high-density large-scale digital circuit was demonstrated. In-depth characterization of dynamic power-supply and ground

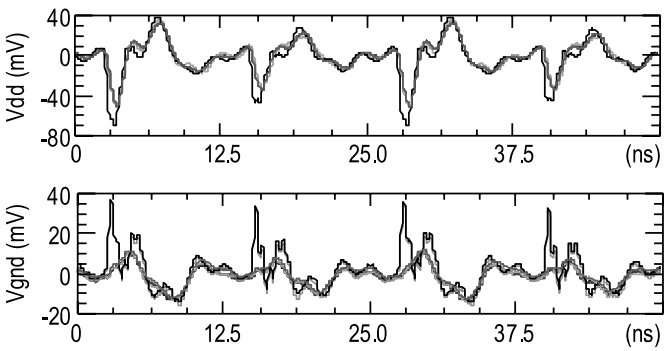

Figure 4: Noise waveforms on power-supply (upper) and ground (lower) wirings measured by detectors on 12-th cell row, where vertical axes show difference from nominal voltage of 1.8 V and 0.0 V, respectively.

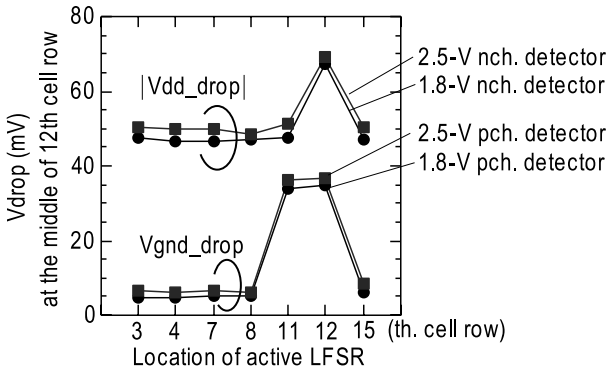

Figure 5: Dynamic voltage drop on power-supply wirings, Vdd_drop, and ground wirings, Vgnd_drop, measured from 1.8 V and 0.0 V, respectively.

noises by the built-in noise detection technique can validate and/or calibrate dynamic power-supply analysis (IR drop) methodologies that are becoming requisite to nanometer scale digital integrated circuits.

Acknowledgments

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References

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[2] M. Nagata, T. Okumoto, K. Taki, "A Built-in Technique for Probing Power Supply and Ground Noise Distribution within Large-Scale Digital Integrated Circuits," *IEEE J. Solid-State Circuits*, vol.40, No.4, pp.813-819, Apr.2005.