EECS31L/CSE31L

Winter 2009

Graphical Tutorial for Xilinx ISE and ModelSim

1. Introduction

This tutorial aims to give a step by step introduction to creating a project in **Xilinx ISE** and simulating it on **ModelSim**. The design is implemented in a given VHDL file.

2. Pre-requisites

Xilinx ISE and ModelSim should be installed and integrated on the system. You should also have the template files provided to you as part of the assignment[1].

3. Lab Assignments

All of your lab assignments will be from the examples of textbook *VHD*L *fo*r *Digita*l *Desig*n by Vahid and Lysecky. The description of your assignments will also be made available to you through EEE. The templates and the first assignment are available on EEE at **Dropbox → AssignmentName → CourseFiles**.

4. Project creation

1. In Xilinx ISE, every design is described by a project. Hence, the first step involves starting a new project. Open New project creation wizard from the **File → New Project** menu. This should open a dialog box like shown in Figure 1. You would notice that the default location of your project directory is C:\Xilinx\10.1 (or the directory you installed Xilinx ISE WepPACK). However, it is generally a good idea to change it to something personal like C:\myProjDir\ as in the figure.

[1] Xilinx WebPACk and Modelsim installation guide will be uploaded to EEE

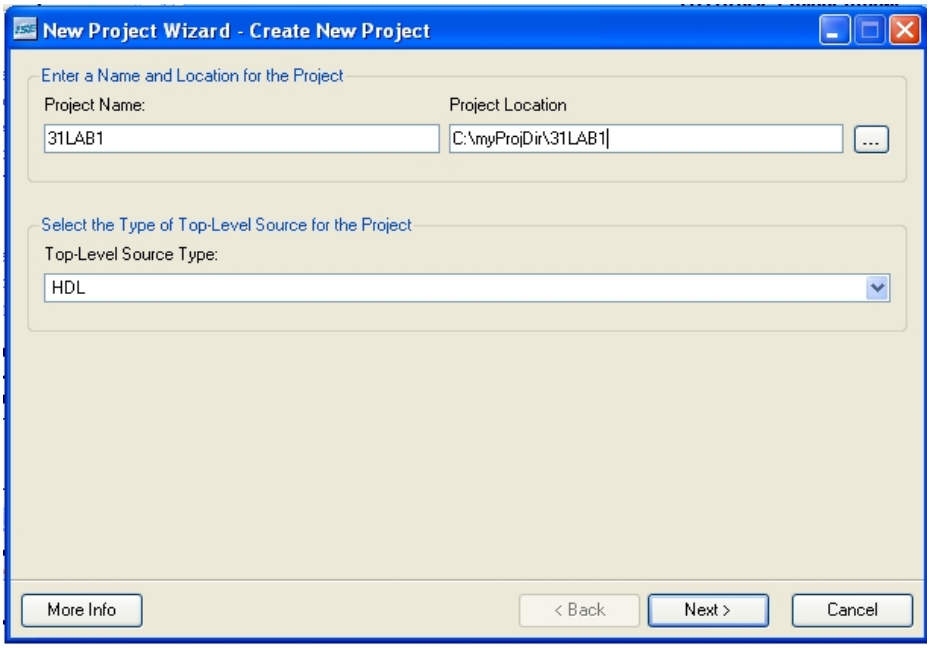

Figure 1: New project creation wizard

The **Top-Level Source Type** should be selected as **HDL** since we will describe our design using VHDL. Add the project name in the text box entry.

2. The next dialog box will be something like in Figure 2.

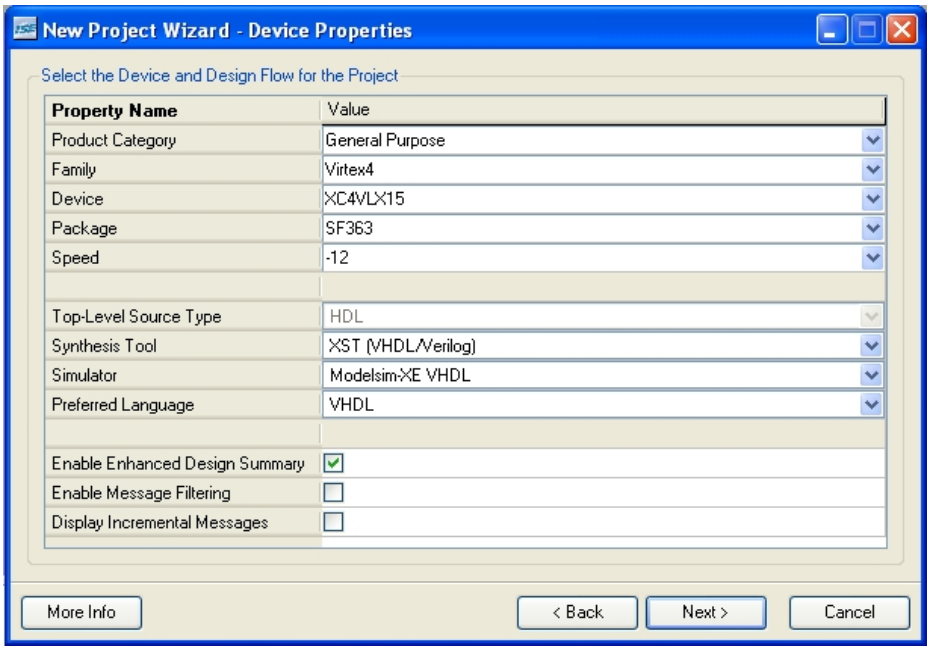

Figure 2: New project creation wizard –Device Properties

We will not be running our design on a real hardware. Therefore, most of the details here regarding device properties can be ignored. However, make sure that the **Synthesis Tool** is selected as **XST (VHDL/Verilog)**, **Simulator** as

ModelSim-XE VHDL and **Preferred Language** should be **VHDL**.

Next few windows will ask to create a new source file for the project. However, those steps can be ignored and no file may be added as we already have a VHDL file for our project. That file will be later added to the project once we have created it. Completing the rest of wizard's options should create a new project in the Xilinx ISE.

3. Once the project has been created there should be two panels on the left side of Xilinx ISE window. The upper panel shows the files included in the project and the lower panel shows the processes that can be run for a file selected in the upper panel. Since we don't have any file included in the project as of now, the upper panel will not show any file. A new source file can be created or an existing one added using the option in the lower panel. Or it can be added by right clicking in the upper panel as shown in Figure 3.

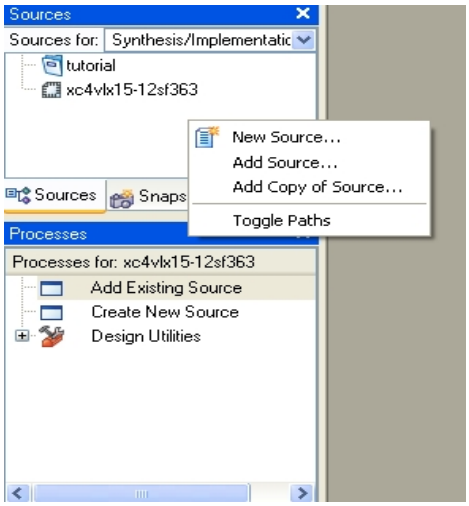

Figure 3: Add Source in the project

The given VHDL file may now be added to the project. The recommended option is to **Add Copy of Source**.

After the file is included, Xilinx ISE window should appear like shown in Figure 4.

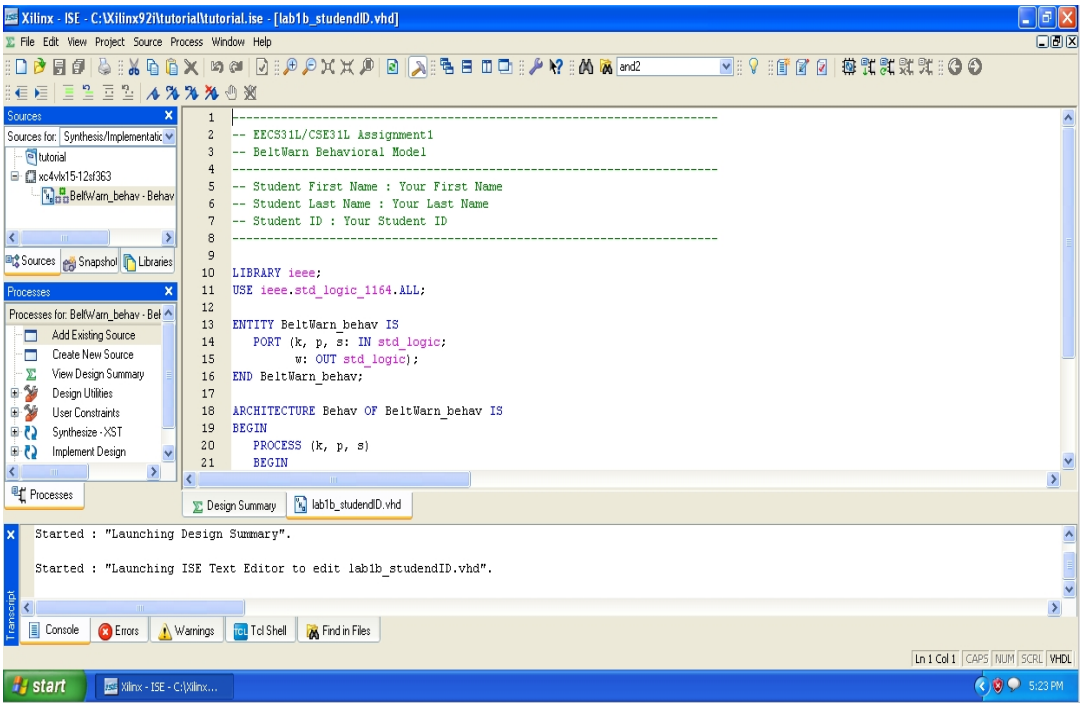

Figure 4: New project created

5. Design Implementation

You may now add the architectural description in the VHDL file. To check for the correctness of your VHDL code, you may consider checking the syntax. This can be done by clicking this option in the lower left panel of the processes. This is shown in Figure 5.

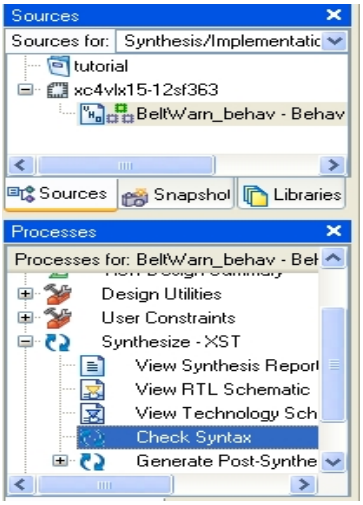

Figure 5: Syntax checking

6. Simulation

1. Once you have implemented your design in the VHDL file and checked for the syntax correctness, you should test your design for its behavior. This can be done by simulating your design with various inputs. Double click **Create New Source** to create a testbench for your design. Select **VHDL Test Bench** as shown in Figure 6 while creating new file. You will then be asked to associate this test bench with a file. Since you have created only a single file till now, this list will have only one file. Select that file and finish this wizard. A file will be created and you may add your test vectors in the file.

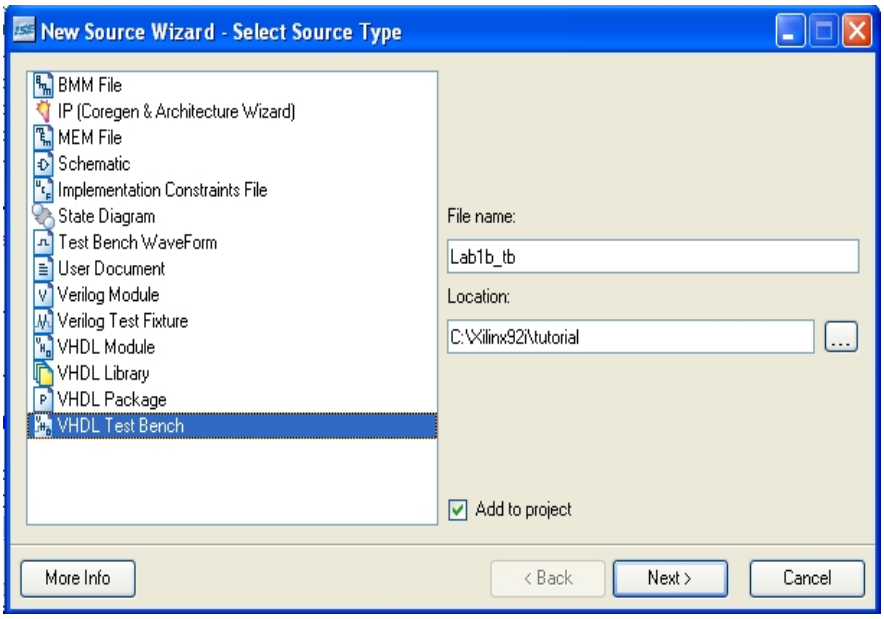

Figure 6: Adding Testbench to the project

2. To run the simulation for your design using this new test bench, select **Behavioral Simulation** as in Figure 7.

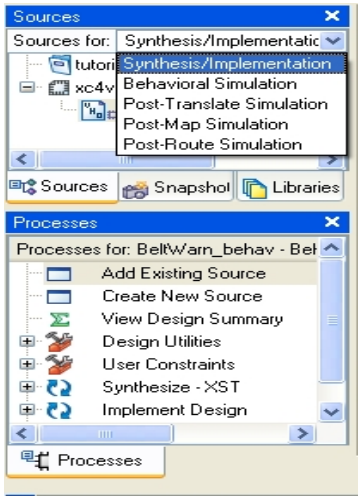

Figure 7: Selecting Behavioral Simulation

Select your testbench file in the upper left panel. The lower panel will then

show you an option to simulate your design like in Figure 8.

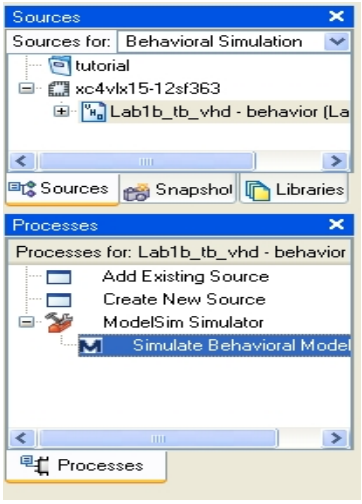

Figure 8: Starting simulation

Double clicking **Simulate Behavioral Model** will open ModelSim and your design will be simulated as per your testbench. ModelSim would look something like in Figure 9[2].

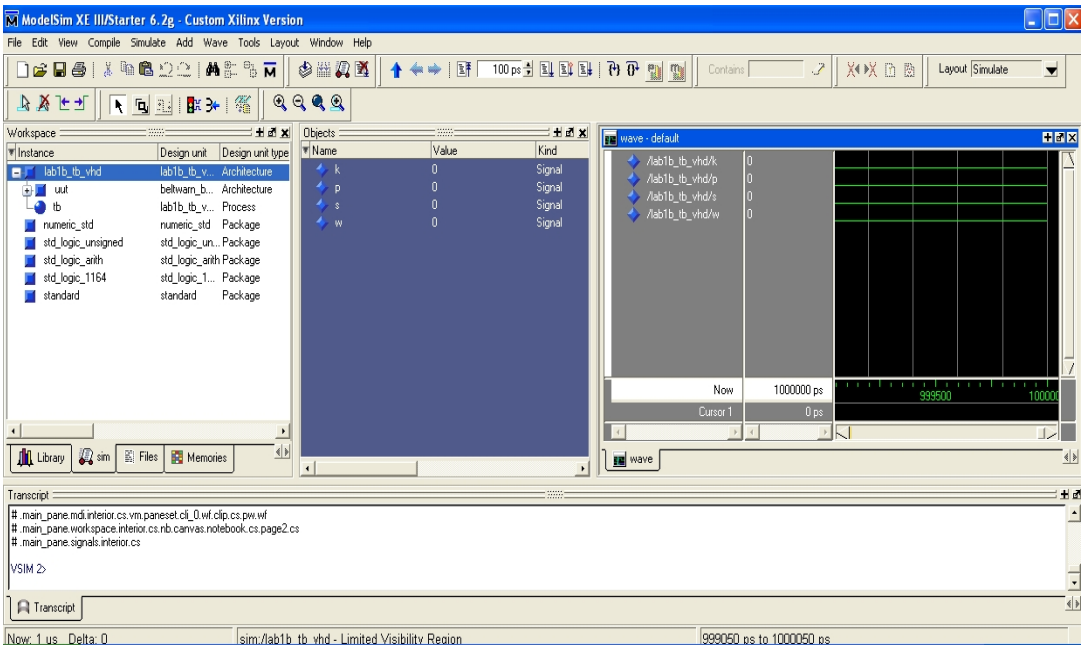

Figure 9: ModelSim Window -The rightmost panel is the test waveform

To inspect the waveform generated, you may consider enlarging it. If your design passes all test vectors, good job! Else you can modify your design or

[2] Note that your testbench was not tested for syntax validity by Xilinx ISE. This is because this check will be performed by ModelSim when it starts. If there is an error in your testbench, it will be shown in the lower console panel of ModelSim. Inspect this panel once if you think your testbench did not run

the testbench to test it again.

3. If your design passes the simulation, you can repeat the above steps to implement another description of your design. You will be required to add files for design description and for testbench.

7 Submission

After finishing your assignment, you need to upload only the moodified template files in the EEE. The dropbox for the first assignment is Dropbox → **AssignmentName** → AssignmentSubmission. You are NOT required to submit your testbench or your project.

8 Further Reading

There are many good tutorials over the web. Xilinx also has some tutorial documents for reference.

1. Quick Start tutorial :
   http://www.xilinx.com/itp/xilinx10/books/docs/qst/qst.pdf
2. In-depth tutorial :
   http://www.xilinx.com/support/techsup/tutorials/tutorials10.htm