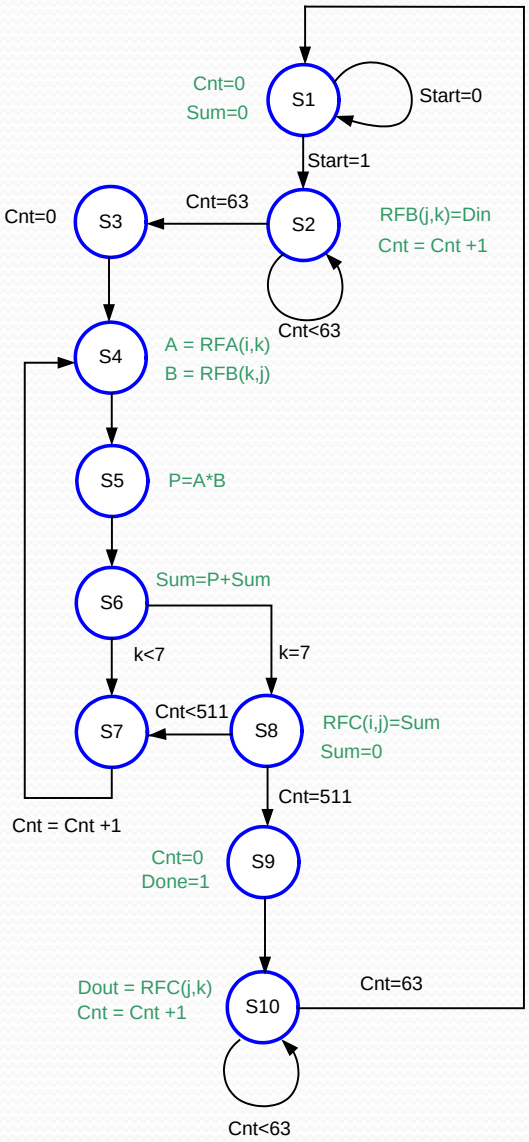
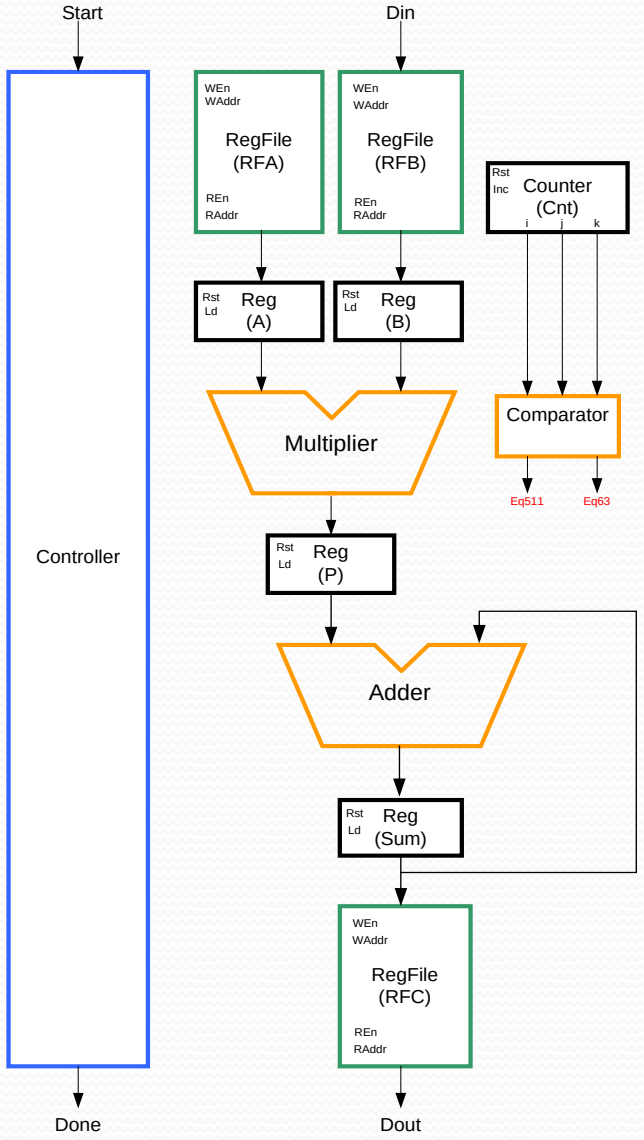
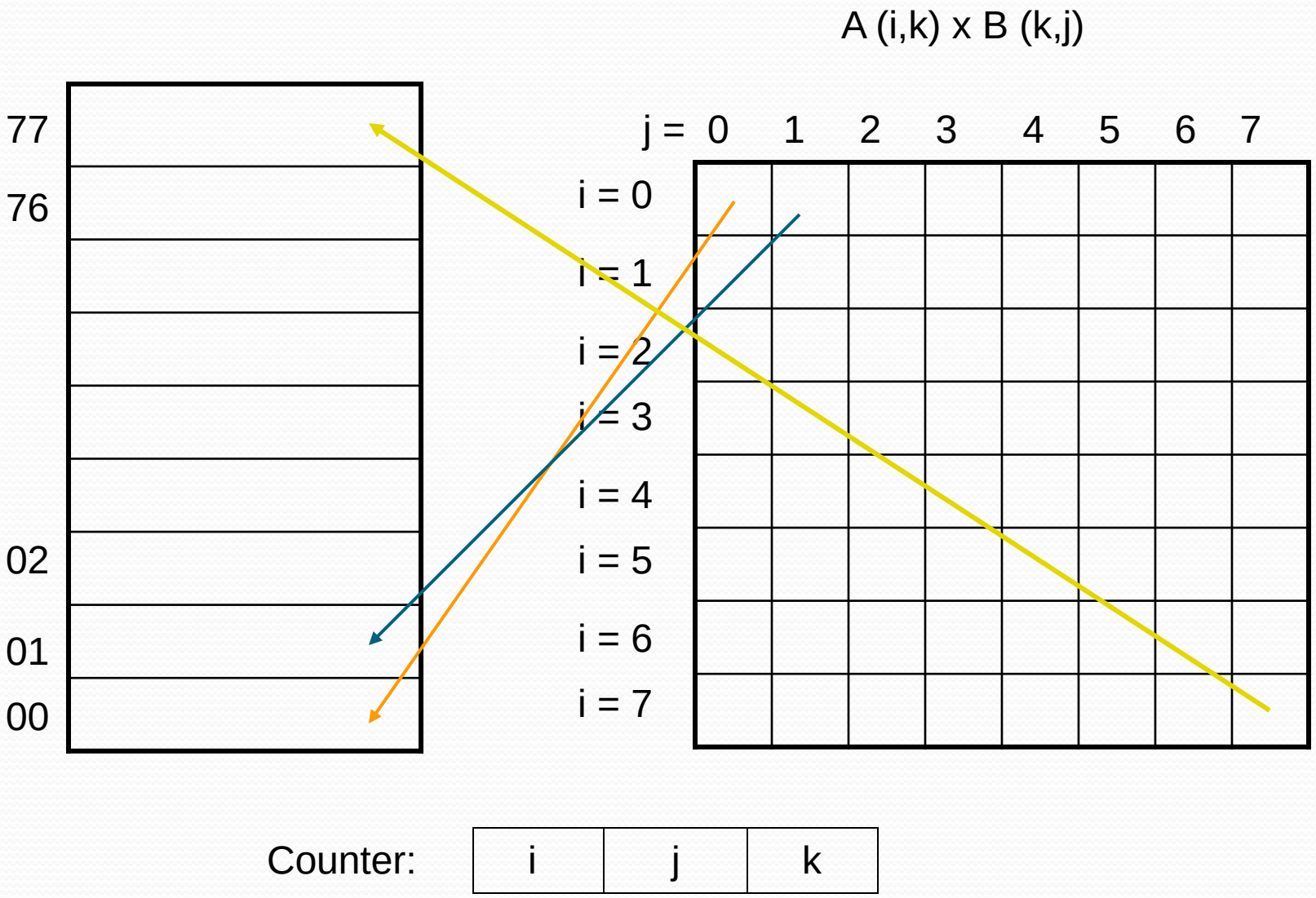
Matrix-Multiply FSMD





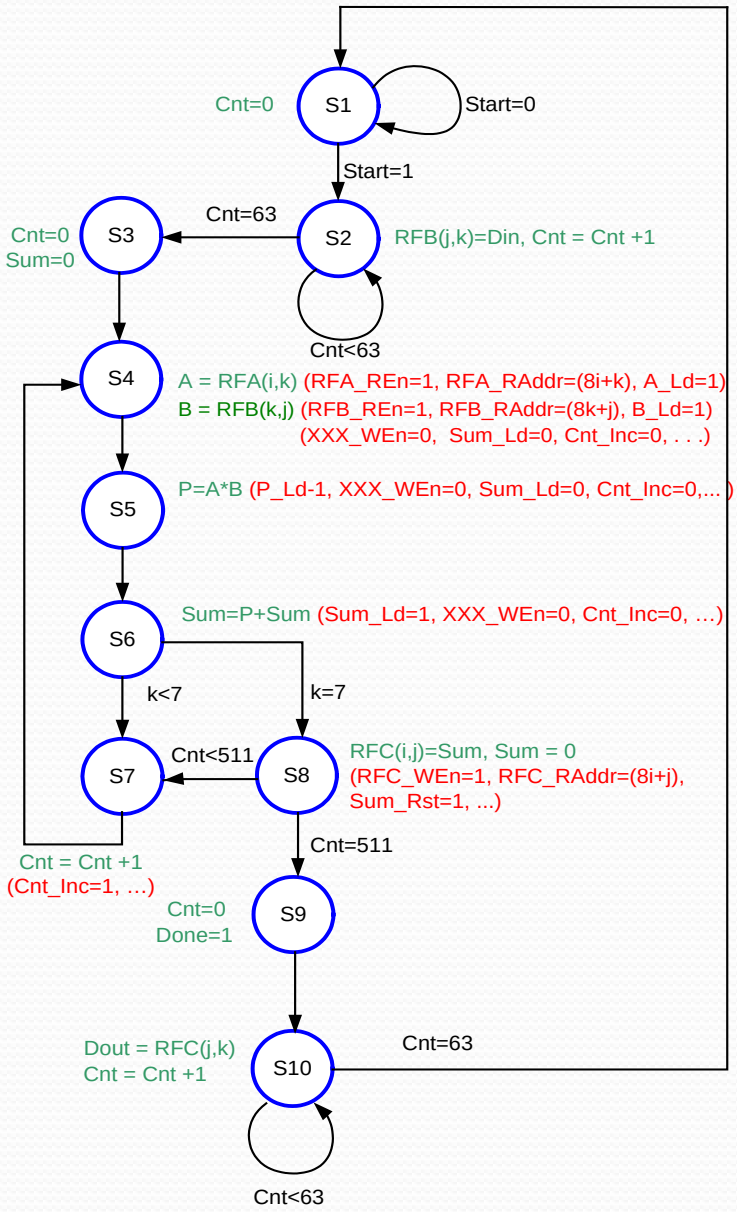
Matrix Storage

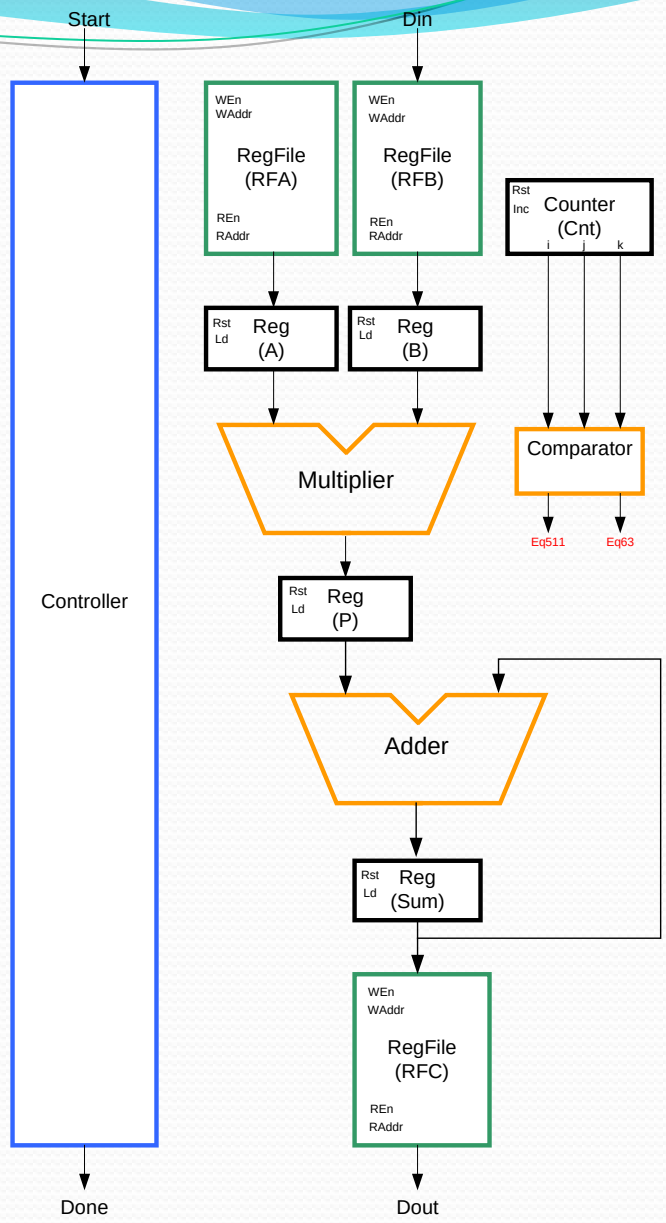


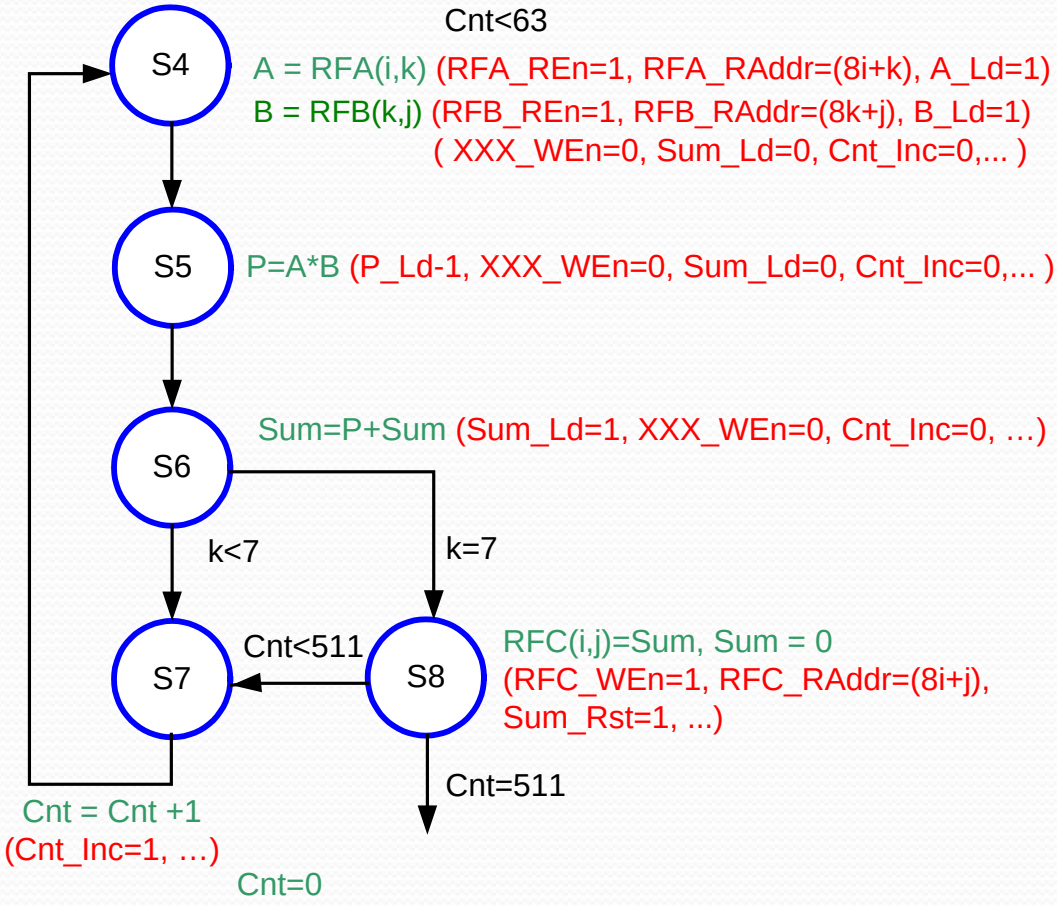
Counter:

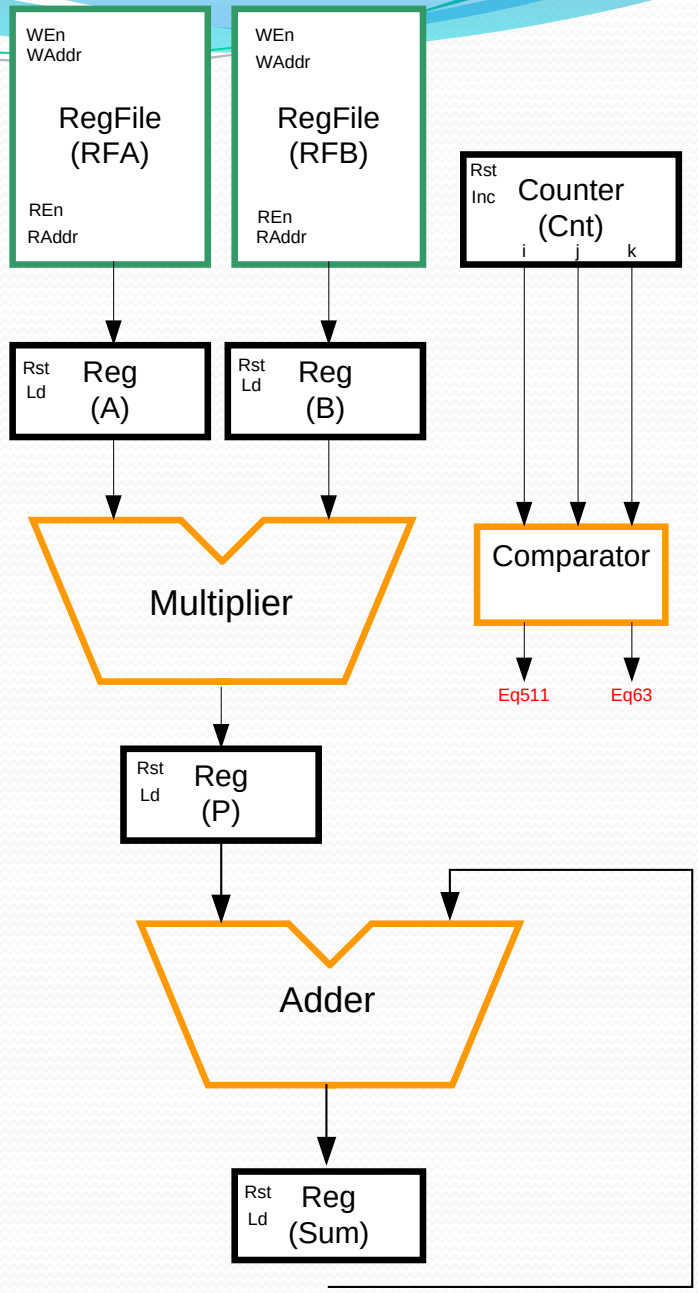
i	j	k

Matrix-Multiply Controller






Cnt<63
S4
A = RFA(i,k) (RFA_REn=1, RFA_RAddr=(8i+k), A_Ld=1)
B = RFB(k,j) (RFB_REn=1, RFB_RAddr=(8k+j), B_Ld=1)
(XXX_WEn=0, Sum_Ld=0, Cnt_Inc=0,...)
S5
P=A*B (P_Ld-1, XXX_WEn=0, Sum_Ld=0, Cnt_Inc=0,...)
S6
Sum=P+Sum (Sum_Ld=1, XXX_WEn=0, Cnt_Inc=0, …)
k<7
k=7
S7
Cnt<511
S8
RFC(i,j)=Sum, Sum = 0
(RFC_WEn=1, RFC_RAddr=(8i+j),
Sum_Rst=1, ...)
Cnt=511
Cnt = Cnt +1
(Cnt_Inc=1, …)
Cnt=0

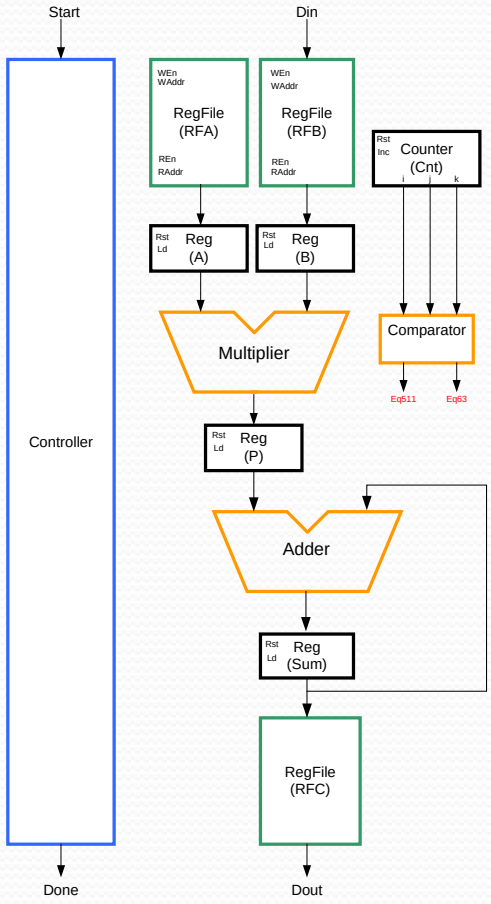

WEn
WAddr
RegFile
(RFA)
REn
RAddr
WEn
WAddr
RegFile
(RFB)
REn
RAddr
Rst
Inc
Counter
(Cnt)
i
j
k
Rst
Ld
Reg
(A)
Rst
Ld
Reg
(B)
Multiplier
Comparator
Eq511
Eq63
Rst
Ld
Reg
(P)
Adder
Rst
Ld
Reg
(Sum)

Matrix-Multiply Structure

```
ENTITY MatrixMult IS
   PORT (
         Clk :    in std_logic;
         Start :  in std_logic;
         Din :    in INTEGER;
         Done :   out std_logic;
         Dout :   out INTEGER
        );
END MatMul;


ARCHITECTURE MatrixMult_struct OF
MatrixMult IS

COMPONENT Multiplier IS
…
COMPONENT Adder IS
…
COMPONENT Counter IS
…
COMPONENT Comparator IS
…
COMPONENT Reg is
…
COMPONENT RegFile IS
…
COMPONENT Controller IS
…
END COMPONENT;
SIGNAL Cnt_Inc, Cnt_Rst, Sum_Ld, Sum_Rst:std_logic;
SIGNAL A_Ld, A_Rst, B_Ld, B_Rst:std_logic;
SIGNAL mult_out: INTEGER;
SIGNAL adder_out, : INTEGER;
SIGNAL i_s, j_s, k_s: std_logic_vector(2 downto 0);
…
```




```
BEGIN

Sum: Reg PORT MAP ( …… );
A: Reg PORT MAP (……);
B: Reg PORT MAP (……);
P: Reg PORT MAP (……);

Controller_1: Controller PORT MAP (……);

RFA: RegFile PORT MAP (……);

RFB: RegFile PORT MAP (……);

RFC: RegFile PORT MAP (……);

Counter_1: Counter PORT MAP (……);

Comparator_1: Comparator PORT MAP (……);

Mult_1: Multiplier PORT MAP (……);

Adder_1: Adder PORT MAP (……);


END MatrixMult_struct;
```