Principles Of
Digital Design

Digital Design Lab Example

Car Locator Example

Optimizing the Car Locator

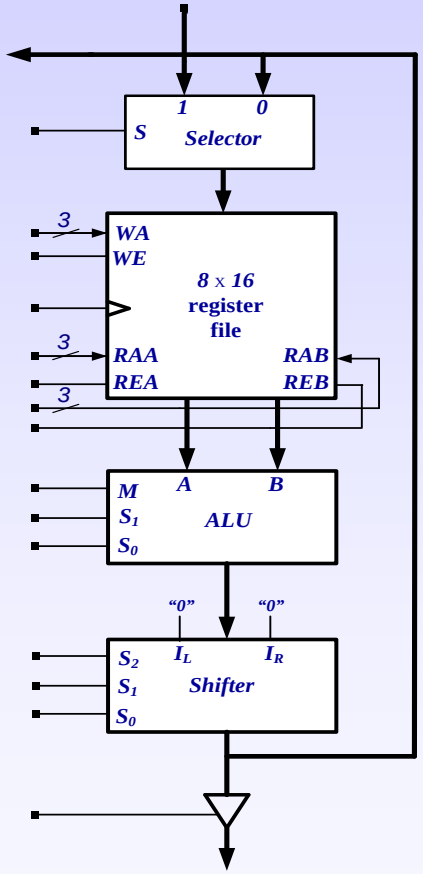
- **The following equation for a constantly accelerating car is given. Minimally change the given datapath to calculate the equation in a shorter time.**

$$X = \frac{at^2}{2} + V_0\, t + X_0$$

- Constant acceleration (**a**):5$^{m}/_{s^2}$
- An initial velocity ($\mathbf{v_0}$): 2$^{m}/_{s}$,
- Starting location ($\mathbf{x_0}$): 4m,
- Time (**t**): 8 sec,

Delays:

- 8x16 Register File: 17 ns, 1 ns setup time
- ALU (ALU): 20 ns from input to output
- 16-bit Shifter: 10 ns from input to output
- 2-to-1 Selector: 5 ns from input to output
- Register: 4 ns, 1 ns setup time



The Datapath

M	S_1	S_0	ALU Operations
0	0	0	Complement A
0	0	1	AND
0	1	0	EX-OR
0	1	1	OR
1	0	0	Decrement A
1	0	1	Add
1	1	0	Subtract
1	1	1	Increment A

ALU operations

S_2	S_1	S_0	
0	0	0	Pass
0	0	1	Pass
0	1	0	Not used
0	1	1	Not used
1	0	0	Shift left
1	0	1	Rotate left
1	1	0	Shift right
1	1	1	Rotate right

Shifter operations

Clock to Clock Delay

- **Total delay for the current datapath:**

$$X = \frac{at^2}{2} + V_0\, t + X_0$$

Clock to Clock Delay :

Load RegFile:	17 ns
ALU Operation:	20 ns
Shifter Operation:	10 ns
Selector:	5 ns
RegFile Setup time:	1 ns
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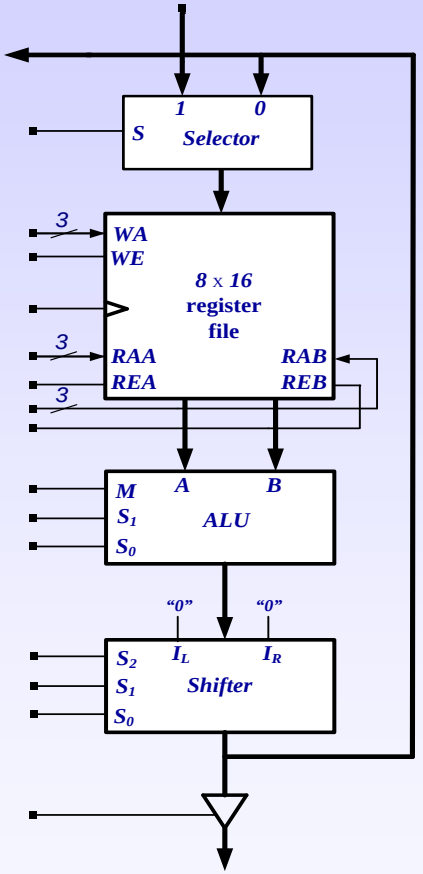
Total Clk to Clk	53 ns

Delays:

- 8x16 Register File: 17 ns, 1 ns setup time
- ALU (ALU): 20 ns from input to output
- 16-bit Shifter: 10 ns from input to output
- 2-to-1 Selector: 5 ns from input to output
- Register: 4 ns, 1 ns setup time



The Datapath

Total Delay

- **Total delay for the current datapath:**

$$X = \frac{at^2}{2} + V_0\, t + X_0$$

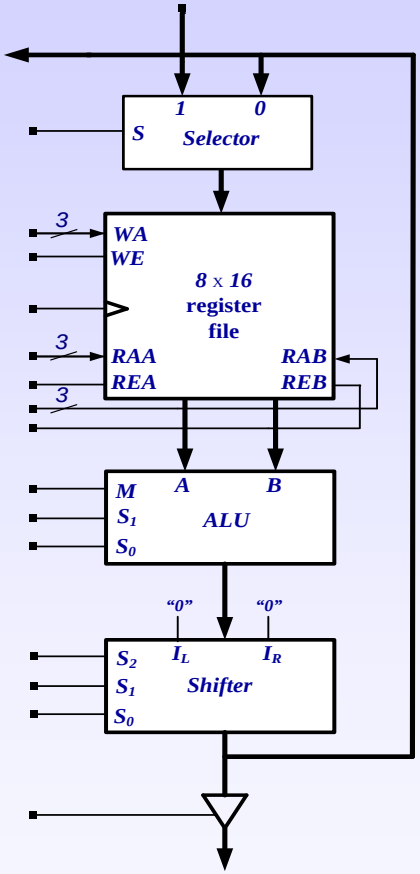
Number of Clocks needed:

1 Clock Cycle :	a X t
1 Clock Cycle :	t X at ÷ 2
1 Clock Cycle:	V_0 X t
1 Clock Cycle:	$\frac{at^2}{2} + V_0 t$
1 Clock Cycle:	$\frac{at^2}{2} + V_0 t + X_0$

Total time needed 5 X Clk to Clk = 265 ns

Delays:

- 8x16 Register File: 17 ns, 1 ns setup time
- ALU (ALU): 20 ns from input to output
- 16-bit Shifter: 10 ns from input to output
- 2-to-1 Selector: 5 ns from input to output
- Register: 4 ns, 1 ns setup time



The Datapath

Optimizing the Car Locator Datapath

- **The total delay for the current datapath:**

$$X = \frac{at^2}{2} + V_0\, t + X_0$$

Optimization: Add Registers in Between RegFile, Alu and Shifter

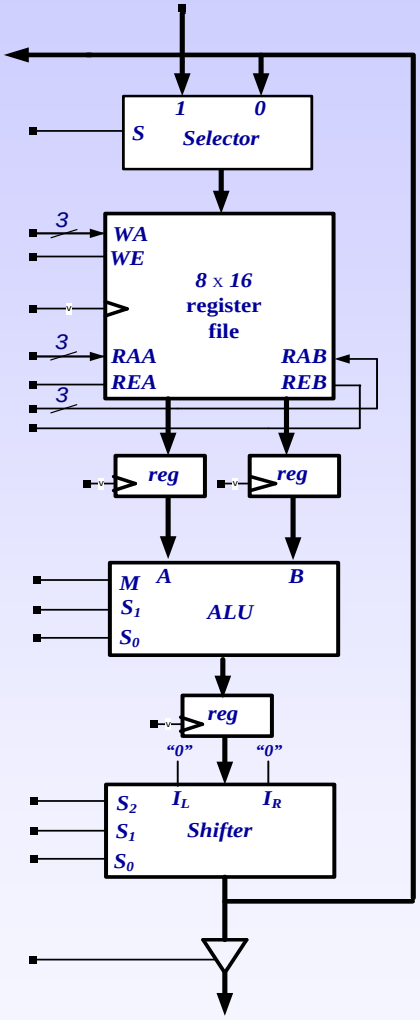
New Clock to Clock Delay : 4 ns + 20 ns + 1ns = 25 ns

Load Register + ALU Operation + Register Setup Time

Every Clock Cycle it Performs :

Delays:

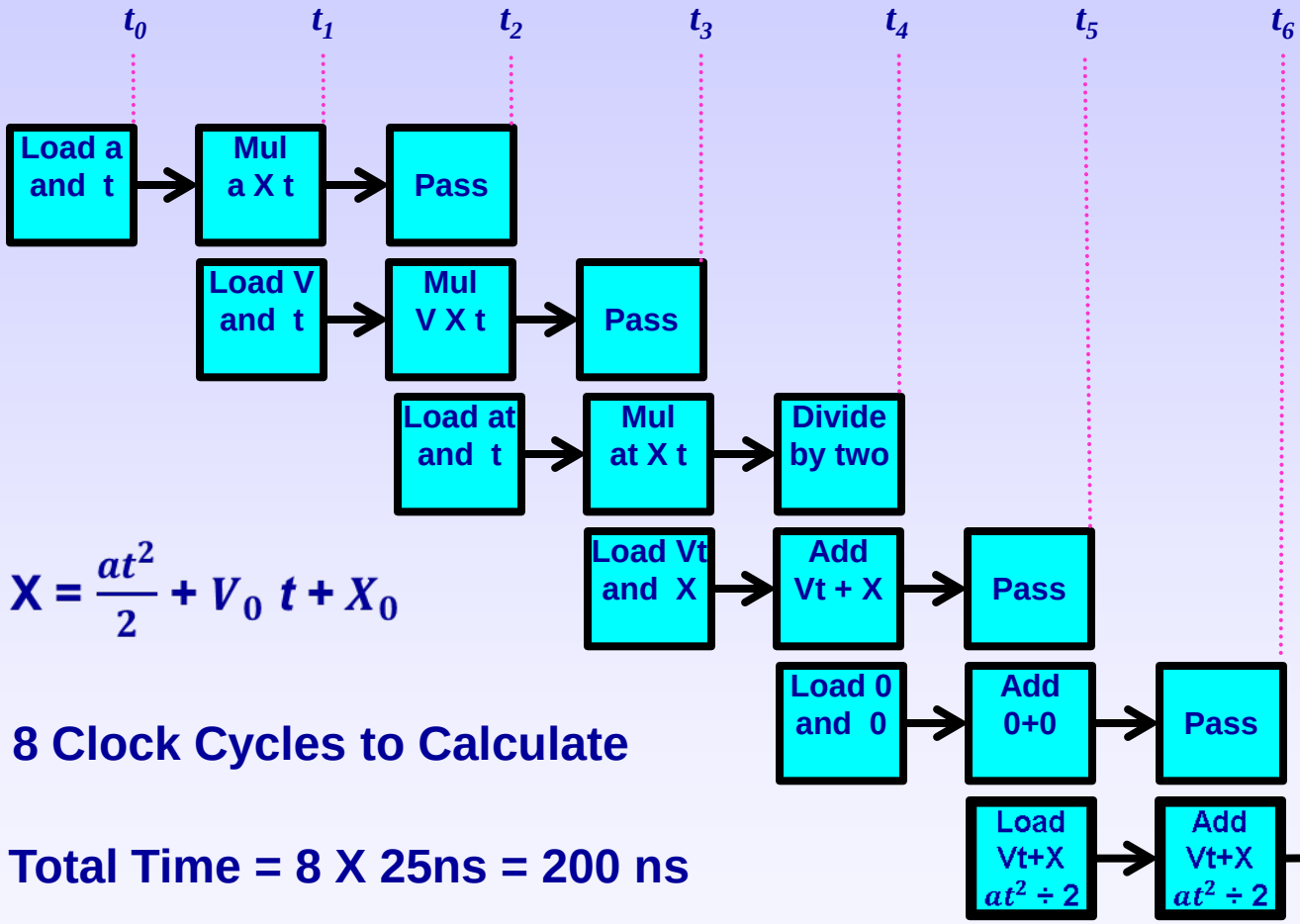
- 8x16 Register File: 17 ns, 1 ns setup time
- ALU (ALU): 20 ns from input to output
- 16-bit Shifter: 10 ns from input to output
- 2-to-1 Selector: 5 ns from input to output
- Register: 4 ns, 1 ns setup time



Modified Datapath

Optimizing the Car Locator DataPath

- The total delay for the current datapath:

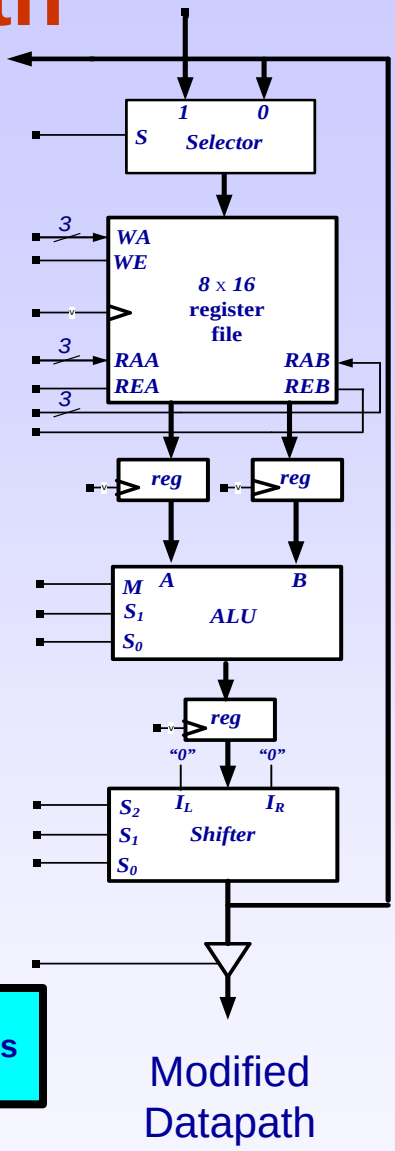


$$X = \frac{at^2}{2} + V_0\, t + X_0$$

8 Clock Cycles to Calculate

Total Time = 8 X 25ns = 200 ns

Total Improvement= 265ns – 200ns= 65ns



Modified Datapath