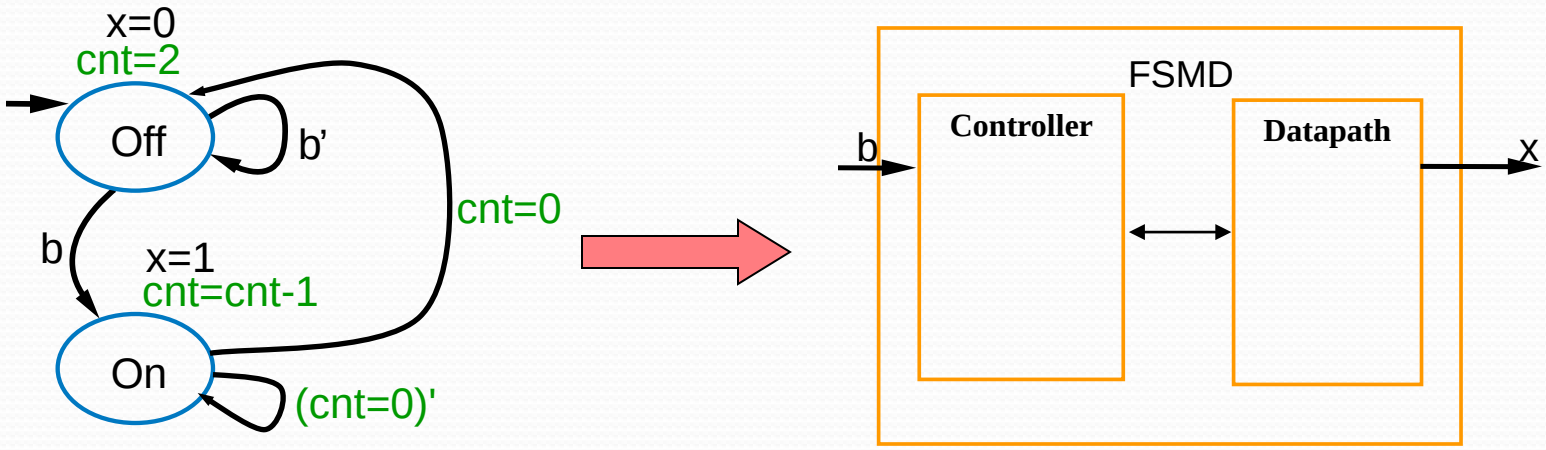
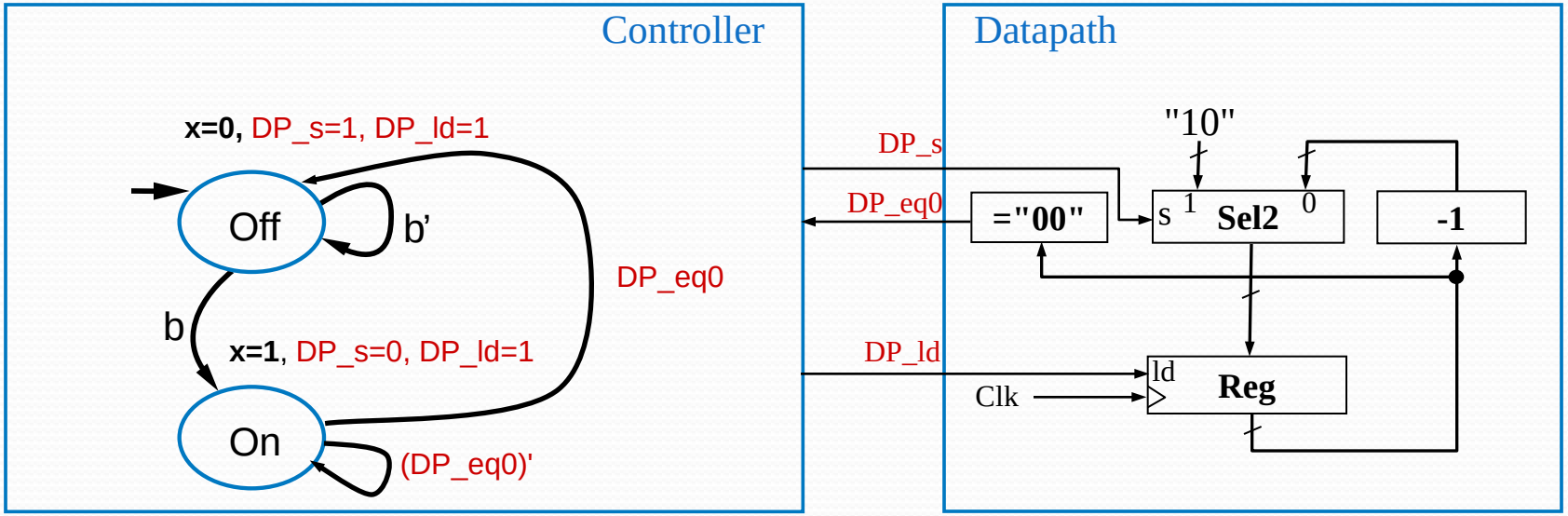
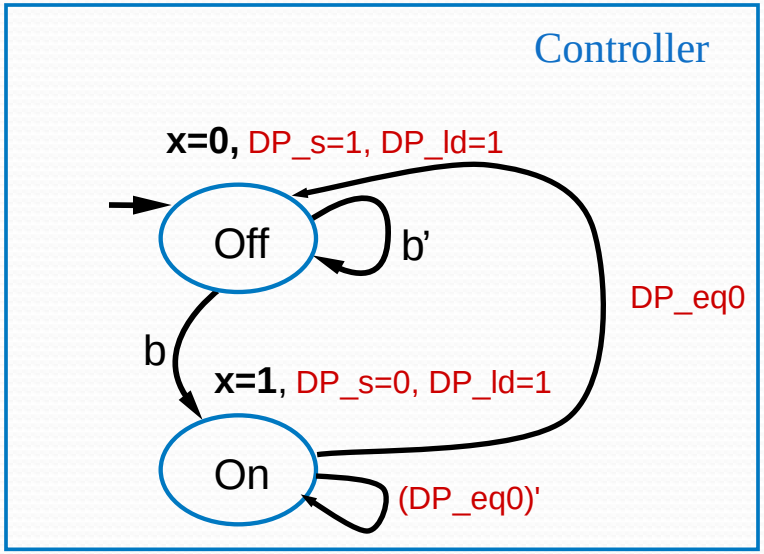
FSMD Structure





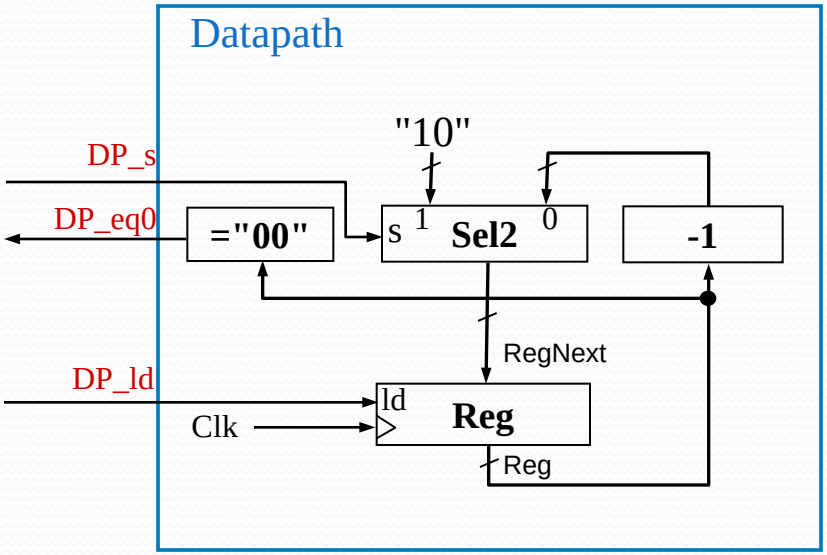
FSMD Controller




```
------ Controller processes ------
CtrlLogic: PROCESS (Currstate, DP_eq0, b)
BEGIN
   CASE Currstate IS
      WHEN S_Off =>
         x <= '0'; DP_s <= '1'; DP_ld <= '1';
         IF (b = '0') THEN
            Nextstate <= S_Off;
         ELSE
            Nextstate <= S_On;
         END IF;
      WHEN S_On =>
         x <= '1'; DP_s <= '0'; DP_ld <= '1';
         IF (DP_eq0 = '1') THEN
            Nextstate <= S_Off;
         ELSE
            Nextstate <= S_On;
         END IF;
   END CASE;
END PROCESS CtrlLogic;

CtrlRegs: PROCESS (Clk)
BEGIN
   IF (Clk = '1' AND Clk'EVENT) THEN
      IF (Rst = '1') THEN
         Currstate <= S_Off;
      ELSE
         Currstate <= Nextstate;
      END IF;
   END IF;
END PROCESS CtrlRegs;
```

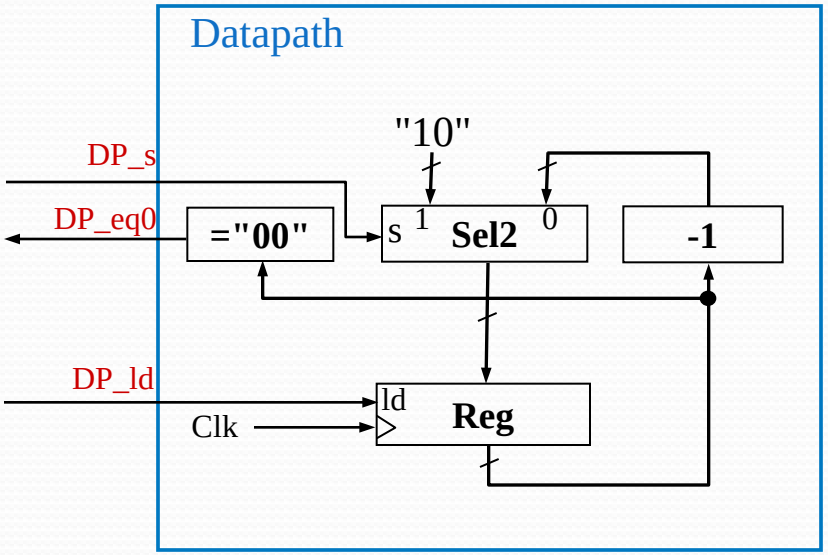
FSMD Datapath

```
...
------ Datapath processes ------

   DPLogic: PROCESS (DP_s, Reg)
   BEGIN
      IF (DP_s = '1') THEN
         RegNext <= "10";
      ELSE
         RegNext <= Reg - "01";
      END IF;
      IF (Reg = "00") THEN
         DP_eq0 <= '1';
      ELSE
         DP_eq0 <= '0';
      END IF;
   END PROCESS DPLogic;

   DPRegs: PROCESS (Clk)
   BEGIN
      IF (Clk = '1' AND Clk'EVENT) THEN
         IF (Rst = '1') THEN
            Reg <= "00";
         ELSIF (DP_ld = '1') THEN
            Reg <= RegNext;
         END IF;
      END IF;
   END PROCESS DPRegs;
...
```



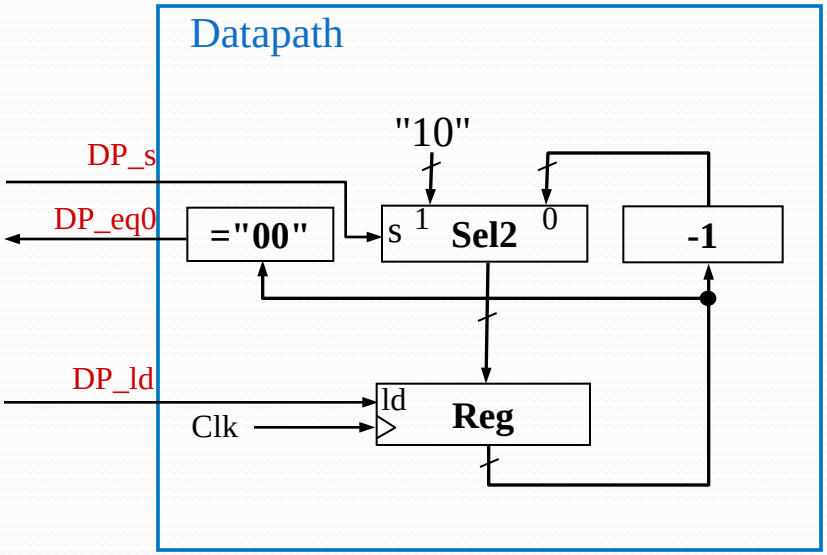
2-Bit Selector

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY 2b_Sel2 IS
   PORT (D0, D1: IN std_logic_vector (1 DOWNTO 0);
         s: IN std_logic;
         Y: OUT std_logic_vector (1 DOWNTO 0));
END 2b_Sel2;

ARCHITECTURE 2b_Sel2_beh OF Sel2 IS
BEGIN

   PROCESS(D1, D0, s)
   BEGIN
      IF (s='0') THEN
         Y <= D0;
      ELSE
         Y <= D1;
      END IF;
   END PROCESS;

END 2b_Sel2_beh;
```



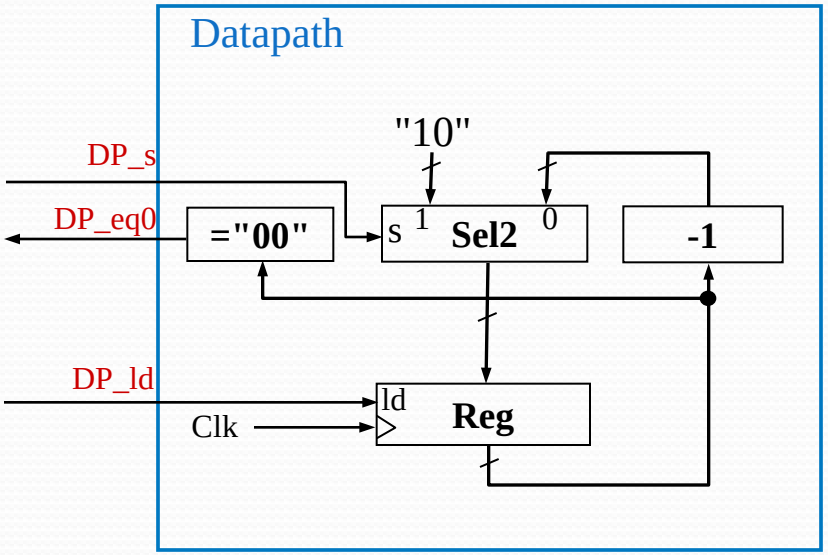
2-Bit Register

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY 2b-Reg IS
   PORT (I: IN std_logic_vector(1 DOWNTO 0);
         Q: OUT std_logic_vector(1 DOWNTO 0);
         Ld,Clk, Rst: IN std_logic );
END 2b-Reg;

ARCHITECTURE 2b-Reg_Beh OF 2b-Reg IS
BEGIN
   PROCESS (Clk)
   BEGIN
      IF (Clk = '1' AND Clk'EVENT) THEN
         IF (Rst = '1') THEN
            Q <= "00”;
         ELSE IF (Ld = ‘1’) THEN
            Q <= I;
         END IF;
      END IF;
   END PROCESS;
END 2b-Reg_Beh;
```



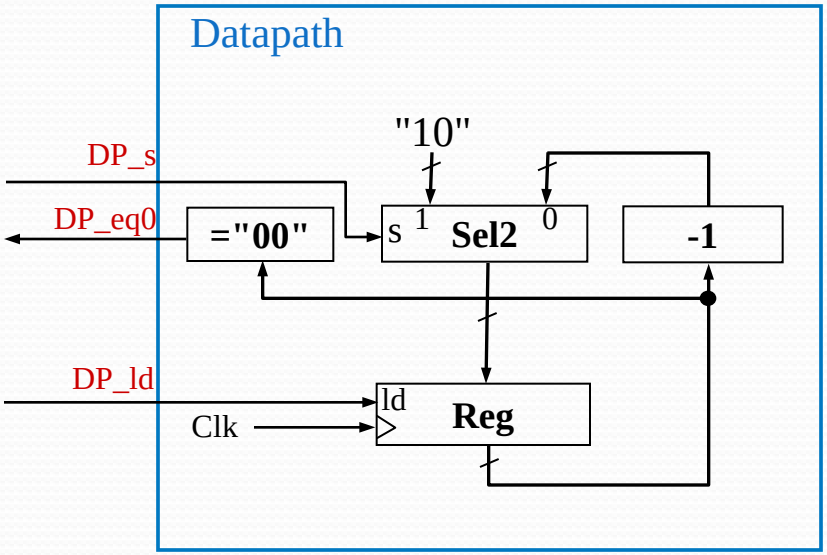
2-Bit Subtractor

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY 2b-Sub IS
   PORT (A, B: IN std_logic_vector(1 DOWNTO 0);
         S: OUT std_logic_vector(1 DOWNTO 0) );
END 2b-Sub;

ARCHITECTURE 2b-Sub_Beh OF 2b-Sub IS
BEGIN
   PROCESS (A, B)
   BEGIN
      S <= A - B;
   END PROCESS;
END 2b-Sub_Beh;
```

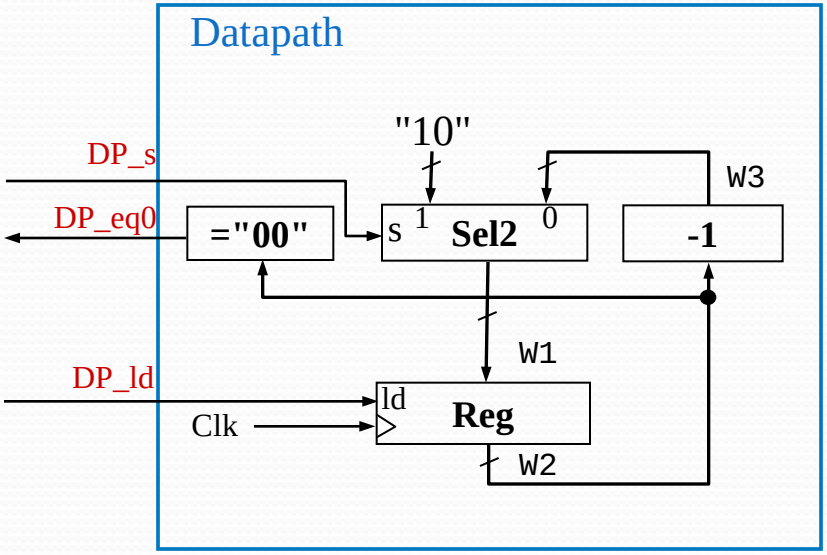


2-Bit Comparator

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;

ENTITY 2b-Comp IS
   PORT (A: IN unsigned(1 DOWNTO 0);
         B: IN unsigned(1 DOWNTO 0);
         Eq: OUT std_logic );
END 2b-Comp;

ARCHITECTURE 2b-Comp_Beh OF 2b-Comp IS
BEGIN
   PROCESS (A, B)
   BEGIN
      IF (A = B) THEN
         Eq<='1';
      ELSE
         Eq<='0';
      END IF;
   END PROCESS;
END 2b-Comp_Beh;
```



FSMD Structure




```
ARCHITECTURE Timer_Struct OF Timer IS

    COMPONENT 2b-Sel2 IS
       PORT (D0, D1: IN std_logic_vector(1 DOWNTO 0);
             Y: OUT std_logic_vector(1 DOWNTO 0);
             s: IN std_logic );
    END COMPONENT;

    COMPONENT 2b-Sub IS
        PORT (A: IN std_logic_vector(1 DOWNTO 0);
              B: IN std_logic_vector(1 DOWNTO 0);
              S: OUT std_logic_vector (1 DOWNTO 0) );
    END COMPONENT;

    COMPONENT 2b-Reg IS
         PORT (I: IN std_logic_vector(1 DOWNTO 0);
               Q: OUT std_logic_vector(1 DOWNTO 0);
               Ld: IN std_logic;
               Clk, Rst: IN std_logic );
    END COMPONENT;

    COMPONENT 2b_Comp IS
          PORT (A, B: IN unsigned (1 DOWNTO 0);
                Eq: OUT std_logic );
    END COMPONENT;

    SIGNAL W3, W2, W1: std_logic_vector(1 DOWNTO 0);

BEGIN
------Controller-----
    StateReg: 2b_Reg: PORT MAP (Nextstate, Currstate, "1",
Clk, Rst);
    CtrlLogic: PROCESS (Currstate, DP_eq0, b)
   . . .
------- Datapath------
    Reg_1: 2b-Reg PORT MAP (W1, W2, DP_ld, Clk, Rst);
    Sub_1: 2b-Sub PORT MAP ( W2, "01", W3);
    Sel2_1: 2b-Sel PORT MAP (W3, "10", W1)
    Comp_1: 2b-Comp PORT MAP (W3, "00", DP_Eq);

END Timer_Struct
```

FSMD Behavior to Structure