Chip Estimator (ChipEst)
Version 1.1

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Abstract

This report describes the guidelines for interfacing with ChipEst (Version 1.1). ChipEst accepts a netlist description of the chip and the desired aspect ratio of the chip and evaluates the height and width of the chip and the locations of the components on the chip. It also provides the worst case delay path on the chip and an estimate of the clock period on the chip. The information provided by ChipEst can be used by any application.

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1 Overview

A top-down VLSI design methodology consists of specifying the behavior of the design and gradually transforming the behavior description to the design layout. Estimation is a very crucial tool in the top-down design methodology. It can be used to to estimate the **physical characteristics of layout** and **accurate timing characteristics** prior to design layout implementation.

ChipEst is a chip level estimator which estimates the physical characteristics and the timing characteristics of a chip. ChipEst consists of two constituents, namely, ChipAreaEst and ChipTimeEst. ChipAreaEst, is the Area estimator in ChipEst, which evaluates the physical characteristics. The physical characteristics include height, width of a chip and geometric information of the components on the chip. ChipTimeEst, is the Timing estimator in ChipEst, which evaluates the timing characteristics. Examples of timing characteristics include the worst case delay path on a chip and an estimate of the clock period on a chip.

Both ChipAreaEst and ChipTimeEst accept a VHDL structural description. This description comprises of a netlist of components. The components are classified into two types, namely, (a) Datapath components, (b) Controller components. The Datapath components operate and manipulate the data. Example of these components include mux, alu, register and register file. The Datapath components are described in a component library such as GENUS. The complete details about the GENUS component library can be obtained in [1]. The Controller components provides controls for the flow of data. They control the operations of the Datapath components.

Both the Datapath components and the Controller components are described as a netlist of logic gates and flipflops and implemented in layout using the standard cell style. In this style, the logic gates and flipflops are layed out into rows and the nets connecting the gates and flipflops are routed in between the rows. By varying the number of rows, the component can be implemented with varying heights and widths. This is known as the Component Shape Function and is shown in Figure 1. The figure shows a component implemented using 2, 3 and 6 rows of standard cells leading to three points on the Component Shape Function.

Given the description of a chip in terms of Datapath components and Controller components, a chip is implemented in layout using macro block style. A macro block style layout model is shown in Figure 2. In this style, the layouts of the components are initially implemented and then the components are arranged on the chip. The nets connecting the components are routed in the space between the components. By varying the arrangement of the components, the height and the width of the chip can be varied. Each of these arrangements lead to a different chip shape. This is called the Chip Shape Function and is shown in Figure 3. The figure shows three different arrangements of the components A, B, C and D leading to three points on the Chip Shape Function.

Given a point on the Chip Shape Function, the height and width of a chip, or in other words, the Chip Aspect Ratio is evaluated. If the aspect ratio of the chip is known, the arrangements of the components on a chip is evaluated. This is known as the Chip Floorplan. The details of the algorithm to determine the Chip Shape Function and the Chip Floorplan can be found in [2].

Each point on the Chip Shape Function leads to a different height and width of the components on a chip. The Chip Floorplan is used to derive the height and the width of the components (geometric information of the component) on the chip, or in other words the Component Aspect Ratio for all the components on a chip. The details of the algorithm to determine the geometric information of the components and Component Aspect Ratio can be found in [2].

Given the Component Shape Function, the netlist description of a chip and the Chip Aspect Ratio, ChipAreaEst, produces height and width estimates for a chip and the Chip Floorplan.

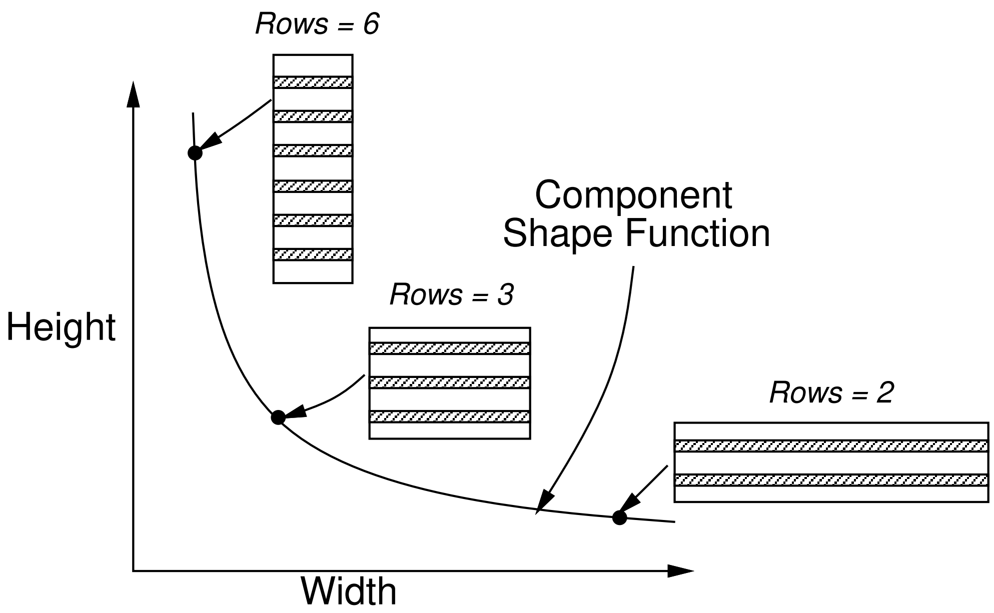


Figure 1: Shape Function of component

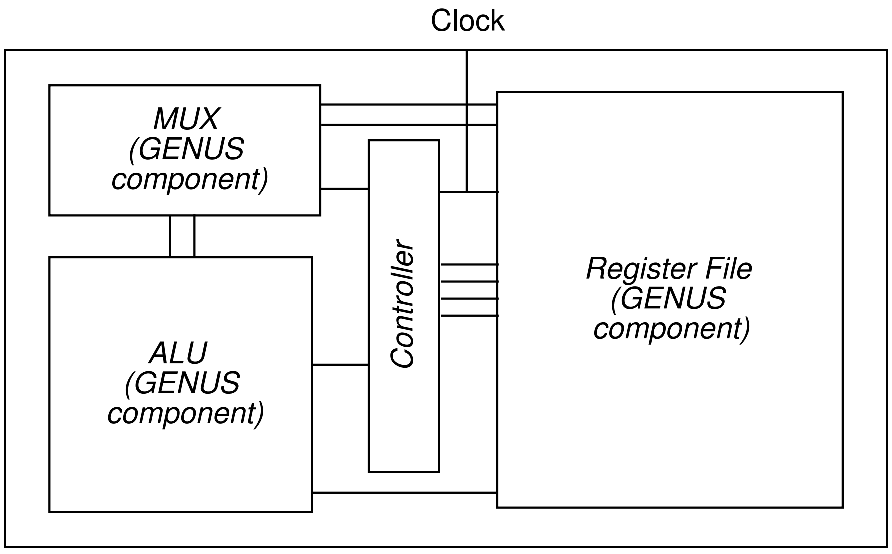


Figure 2: Layout Model of Chip

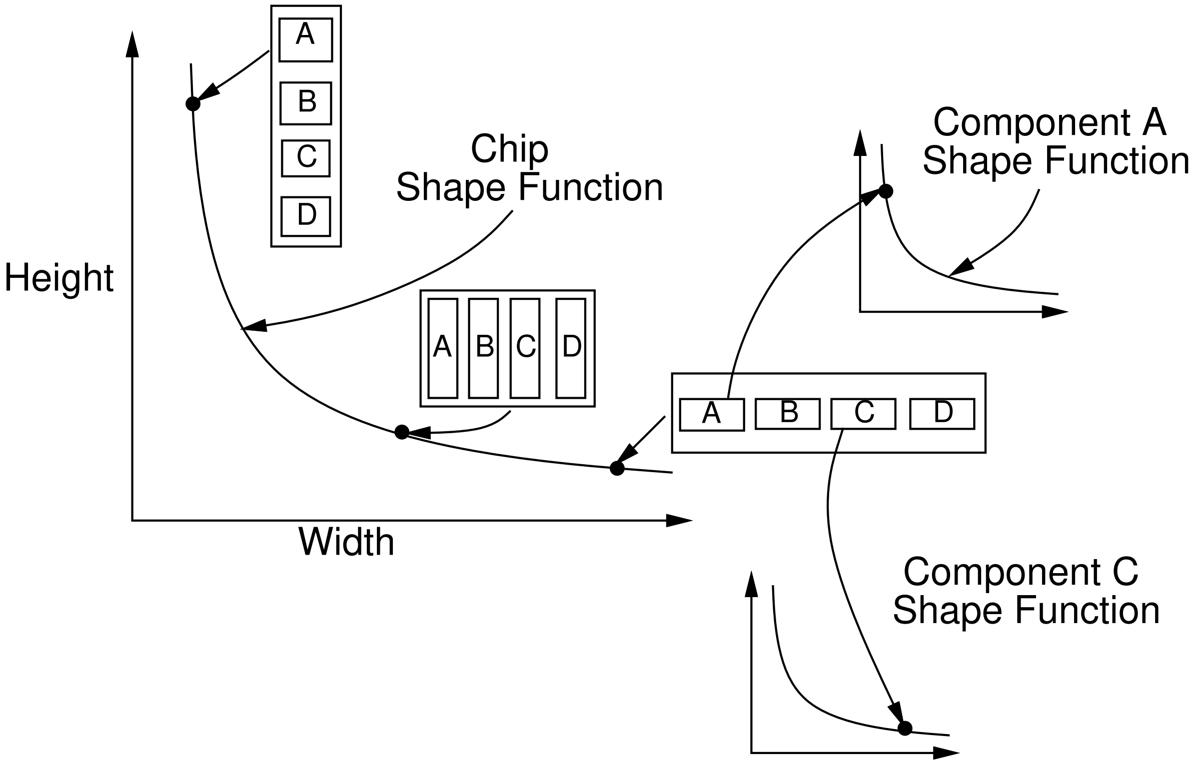


Figure 3: Shape Function of Chip

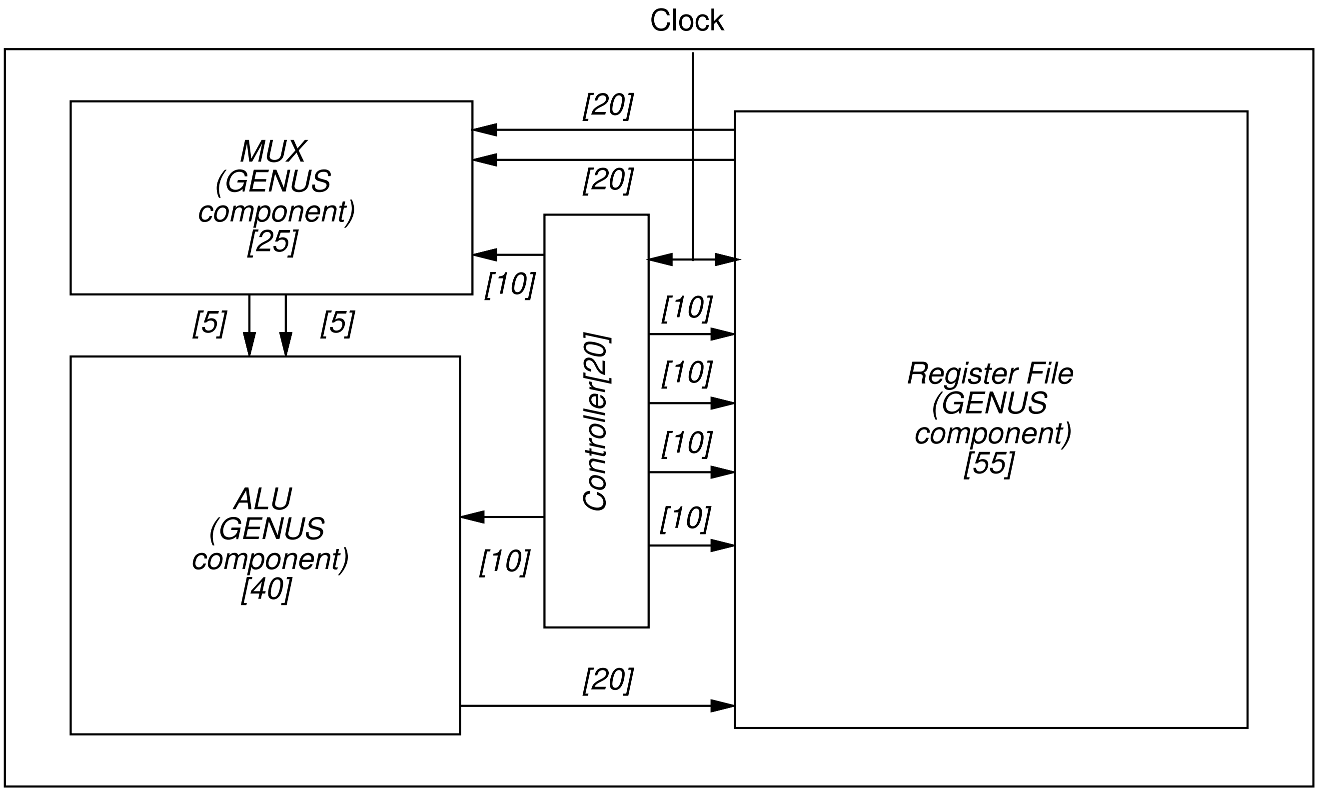
This information is used by ChipTimeEst, the Chip Timing estimator, to evaluate the timing characteristics of a chip. The timing characteristics of a chip are dependent on the delay of a signal on a path between the clocked components on a chip. Example of clocked components include Controller component, Register File Component. The example in Figure 4 shows the delays between the clocked components, Controller and Register File on the various paths.

The delay between clocked components has two main constituents, namely, the delay on the nets in the path connecting the components and the delay of the components in the path.

The component delay is dependent on the type of component and the shape of the component. The ChipAreaEst evaluates the shape of all the components on a chip. A delay value is associated with every point on the Component Shape Function as seen in Figure 5, This new shape function is called the Component Shape-Delay Function. [2] discusses the algorithms used to derive the Component Shape-Delay Function.

In addition to the component delay, the net in the path also contribute to the delay between the clocked components. The net delay is dependent on the length of the nets connecting the components. ChipAreaEst estimates the Chip Floorplan and the geometric information of the components. This helps to evaluate the length of the nets connecting these components. The algorithms used to derive the lengths of the nets are described in [2].

The sum total of the delay of the nets and components in the path leads to the delay between the clocked components. The maximum worst case delay between any two clocked components provides a lower bound on the clock period in a chip. The timing estimates provided by ChipTimeEst includes the lower bound on the clock period and the description of the path on which the maximum worst case delay occurred.



Delay on Paths between Controller and Register File

	Paths	Delay
1	Controller --> ALU --> Register File	145
2	Controller --> MUX --> ALU --> Register File	175
3	Controller --> Register File	85

Figure 4: Path Delays on a Chip

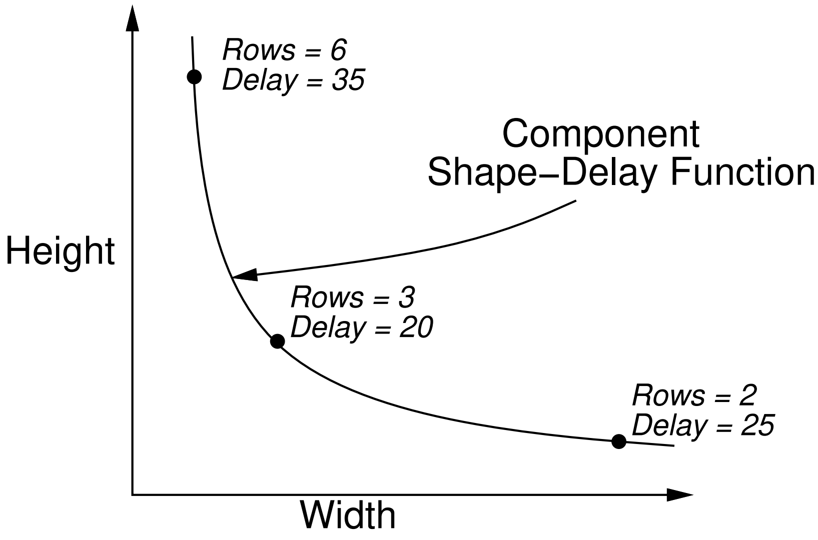


Figure 5: Component Shape-Delay Function

The next section gives a brief description of ChipAreaEst and ChipTimeEst and how they are configured together to produce the ChipEst. Section 3 provides the ChipEst System overview, its input files and the kind of outputs it produces. Section 4, illustrates the usage of ChipAreaEst and ChipTimeEst through a simple example. Appendix A gives the actual interface format that can be used to communicate with ChipAreaEst and Appendix B gives the interface formats for ChipTimeEst.

2 Chip Estimation System

ChipAreaEst and ChipTimeEst can be interfaced with DSE and GENUS as shown in Figure 6. ChipAreaEst obtains the *Chip Netlist* described in Structural VHDL and the desired *aspect ratio*(AR) of a chip from DSE. It also obtains the Component Shape-Delay Function of all the Components in the netlist from GENUS. The *Component File* consists of the Component Shape-Delay Function which is extracted by GENUS from CompEst. (The detailed description of the GENUS to CompEst interface can be obtained in [3]).

Given all the above inputs, ChipAreaEst produces (a) the *Wirelength File* consisting of the wire length of all the nets in the netlist, (b) the *Geometric File* consisting of the height and width of a chip, the Chip Floorplan and the Geometric Information of all the Components. The *Geometric File*, the *Wirelength File* are stored in the *Results Output File*(ROF) for ChipAreaEst.

ChipTimeEst uses the *Wirelength File*, the *Geometric File*, the *Chip Netlist File* and the *Component File* and performs the timing estimation of a chip. It produces the *Timing File* which contains the worst case paths on a chip and the estimated lower bound of the clock period on a chip. The *Timing File* is stored in the *Results Output File*(ROF) for ChipTimeEst. The actual format of the ROF can be obtained in Appendix A and B.

The input information to ChipAreaEst and ChipTimeEst is stored in the *Required Inputs File*(RIF). In general, the input information can be classified into two categories, namely, *mandatory inputs* and *default inputs*.

Mandatory inputs contain essential information without which ChipAreaEst and ChipTimeEst cannot execute. The desired Chip *aspect ratio* (AR), the *Chip Netlist File* and the *Component File*

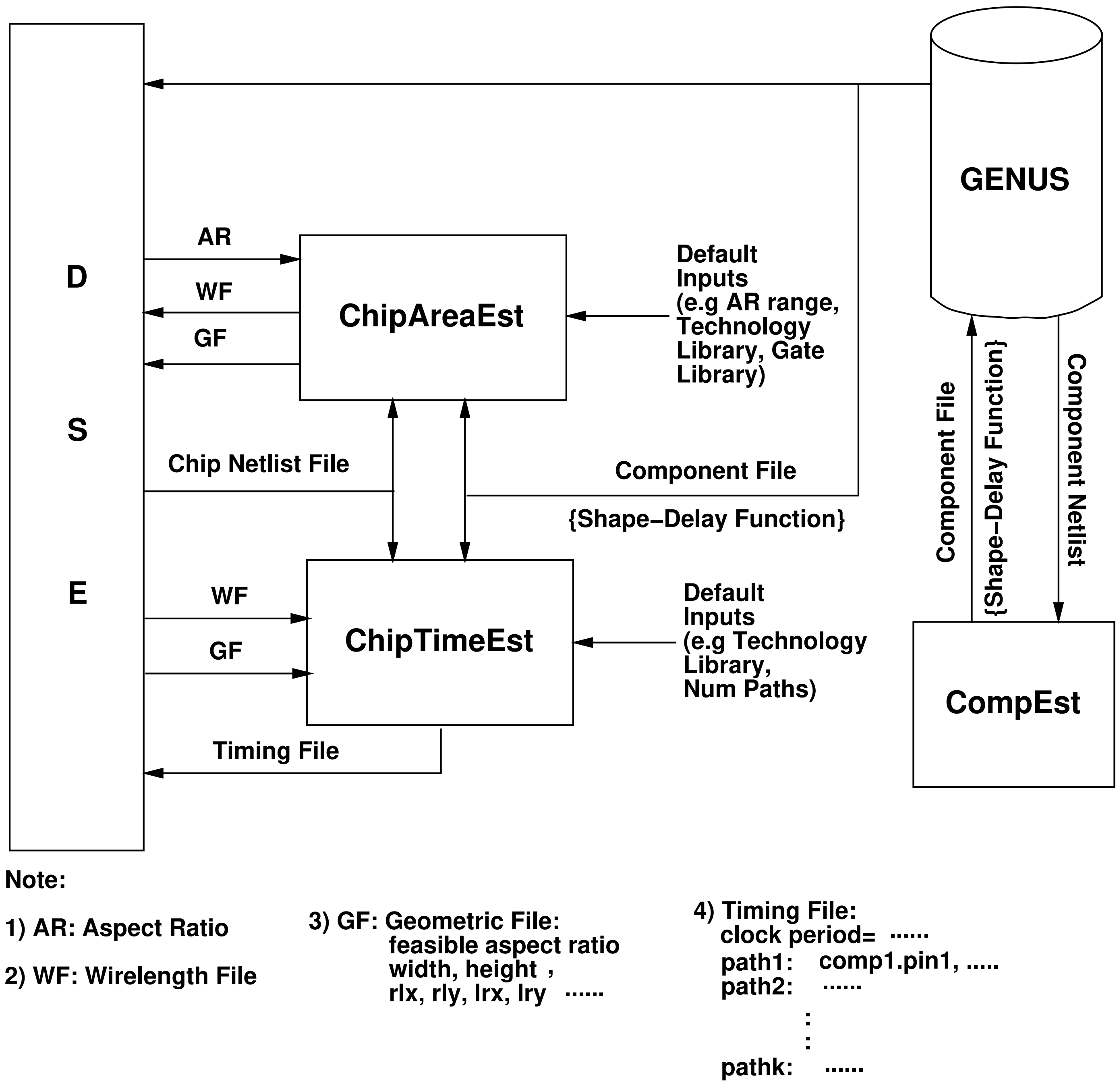


Figure 6: DSE – Chip Estimator Interface

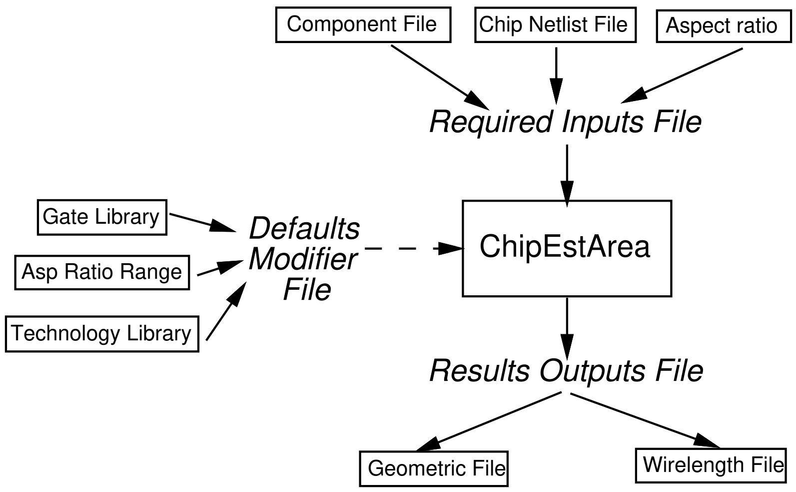


Figure 7: Details of Chip Area Estimator Interface

form the *mandatory inputs* for ChipAreaEst. The *Geometric File*, the *Wirelength File*, the *Chip Netlist File* and the *Component File* form the *mandatory inputs* for ChipTimeEst. The *mandatory inputs* are specified in the *Required Inputs File*(RIF). The exact formats of the mandatory inputs can be obtained in Appendix A and B.

Default inputs contain optional information which may or may not be specified. The specified *default inputs* are present in the *Defaults Modifier File* (DMF). If the *default inputs* are not specified, then ChipEst uses predetermined values for these inputs. An example of the *default inputs* includes the file containing the technology information which specifies the layout design rules and the gate timing characteristics. The exact formats of these default inputs can be obtained in Appendix A and B.

3 Interface Files

This section will examine in detail the information stored in each of the input and output files. It will examine the contents of RIF, ROF and DMF interface files for ChipAreaEst as shown in Figure 7. The exact file formats can be obtained in Appendix A.

It will also examine the RIF, ROF and DMF files for the ChipTimeEst as shown in Figure 8. The exact file formats can be obtained in Appendix B.

3.1 Results Input File for ChipAreaEst

The RIF consists of three types of inputs namely, *Chip Netlist*, *Component File* and *Aspect Ratio.*

The *Chip Netlist* specifies the path name of the netlist file and the file format. The netlist file describes a chip as a connection list of Components. The Components have to be present either in the GENUS Component library, or in the standard cell library.

The *Aspect Ratio* specifies the ratio of the height and width of a chip.

The *Component File* specifies the Component Shape-Delay Function. The information is represented as a width, height, delay tuple. The *Component File* also consists of the Component Name associated with the tuple and the number of tuples for every component.

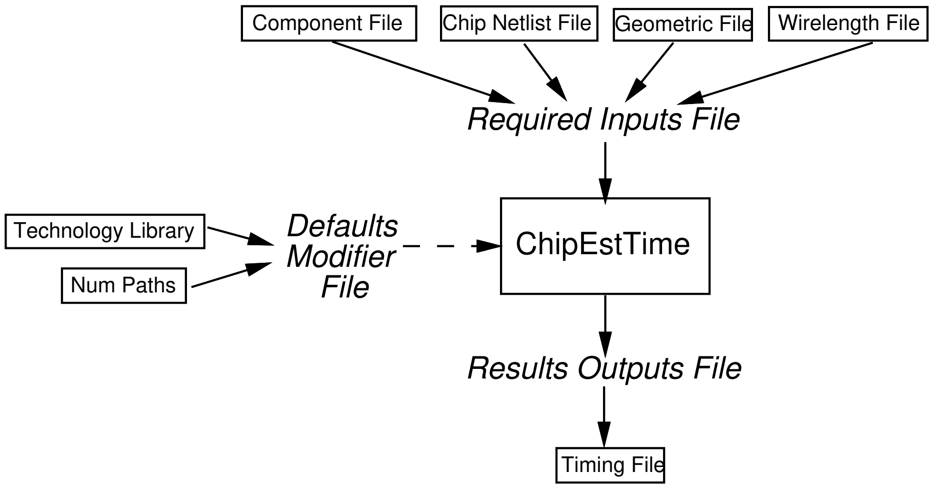


Figure 8: Details of Chip Timing Estimator Interface

3.2 Defaults Modifier File for ChipAreaEst

This file consists of the defaults that need to be modified. Typically, the defaults information includes the *Gate Library*, the *Technology Library* and the *Aspect Ratio Range* for all calculations.

The *Gate Library* specifies the height, width and delay of all logic gates in the Datapath components and the Controller components.

The *Technology Library* specifies the layout design rules, the unit capacitance and resistance on the wires, and the gate output resistance and gate input capacitance information.

The *Aspect Ratio Range* specifies the maximum and minimum aspect ratio that needs to be considered for any calculation.

3.3 Results Output File for ChipAreaEst

The ROF consists of the *Geometric File* and the *Wirelength File*.

The *Geometric File* describes a chip in terms of its width and height. It also contains the Chip Floorplan and the Geometric information of the Components. The information is in the form of a tuple consisting of component name, component x origin, component y origin and component height and width.

The *Wirelength File* indicates the length of each of the nets in the netlist description. The Wirelength File has two (or multiples of two) fields which include the net name and the net wire length.

3.4 Results Input File for ChipTimeEst

The RIF consists of the following four sections : *Geometric File*, *Wirelength File*, *Chip Netlist* and the *Component File*. The *Geometric File* and the *Wirelength File* are identical to the ones produced by ChipAreaEst. The *Component File* and the *Chip Netlist* are identical to the ones used by ChipAreaEst.

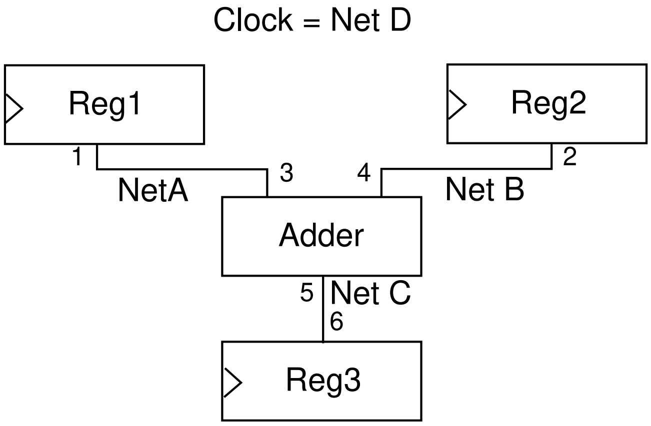


Figure 9: A Tutorial example of a Chip

3.5 Results Output File for ChipTimeEst

The ROF consists of the *Timing File* for a successful ChipEstTime run, which includes the clock information and the worst case path information.

The clock information section consists of the clock net name and the clock period. The CET_NUM_PATHS is used to specify how many worst case paths will be output by ChipTimeEst. For each worst case path the information consists of: (1) the number of pins on the path, and, (2) the list of composite pins on that path.Finally, The composite pin name consists of a component name followed by a dot and concluded by a name of the pin on the component. For example, a composite pin name could be mux2.I0, that specifying the pin I0 on component mux2.

3.6 Defaults Modifier File for ChipTimeEst

This file consists of information whose default values can be modified. It basically can consist of CET_TEC_LIB ,CET_GATE_TIMING_LIB and the CET_NUM_PATHS information.

The CET_TEC_LIB specifies the layout design rules, the unit capacitance and resistance on the wires, and the gate output resistance and gate input capacitance information.

The CET_GATE_TIMING_LIB specifies gate height and width characterstics, also, it specifies the delay characterstics.

The CET_NUM_PATHS information specifies the number of worst case paths that the ChipTimeEst needs to calculate.

4 Tutorial

This section illustrates the RIF and ROF files for a design having an Adder and three 16-bit Registers, which is shown in Figure 9.

In order to obtain the estimates of the physical characteristics of the chip from ChipAreaEst, the RIF needs to be constructed. The following RIF can be used for this purpose by ChipAreaEst :

```
%CHIP NETLIST
CEA_NETLIST_FILENAME : example.vhdl
CEA_NETLIST_FORMAT : VHDL

%DESIRED ASPECT RATIO
CEA_ASPECT_RATIO : 1.0

%COMPONENT FILE
CE_COMPONENT_NAME : Adder
CE_NUM_TUPLES : 2
CE_SHAPE_TUPLE : 30.0,40.0
CE_COMPONENT_DELAY: 20
CE_SHAPE_TUPLE : 45.0,25.0
CE_COMPONENT_DELAY: 25
CE_COMPONENT_NAME : Register
CE_NUM_TUPLES : 1
CE_SHAPE_TUPLE : 20.0,29.0
CE_COMPONENT_DELAY: 10
```

The results of ChipAreaEst are present in ROF. The following ROF is obtained by ChipAreaEst for the example shown in Figure 9:

```
%GEOMETRIC FILE
CEA_CHIP_WIDTH : 70.0
CEA_CHIP_HEIGHT : 60.0
CEA_COMPONENT_NAME : ADDER
CEA_COMPONENT_XLEFT : 0
CEA_COMPONENT_YLEFT : 0
CEA_COMPONENT_XRIGHT : 45.0
CEA_COMPONENT_YRIGHT : 25.0

CEA_COMPONENT_NAME : REG1
CEA_COMPONENT_XLEFT : 0
CEA_COMPONENT_YLEFT : 30.0
CEA_COMPONENT_XRIGHT : 20.0
CEA_COMPONENT_YRIGHT : 59.0

CEA_COMPONENT_NAME : REG2
CEA_COMPONENT_XLEFT : 25.0
CEA_COMPONENT_YLEFT : 30.0
CEA_COMPONENT_XRIGHT : 55.0
CEA_COMPONENT_YRIGHT : 59.0
```

CEA_COMPONENT_NAME : REG3
CEA_COMPONENT_XLEFT : 50.0
CEA_COMPONENT_YLEFT : 30.0
CEA_COMPONENT_XRIGHT : 70.0
CEA_COMPONENT_YRIGHT : 59.0

%WIRELENGTH FILE
CEA_NET_NAME : NET A
CEA_NET_WIRELENGTH : 5.0
CEA_NET_NAME : NET B
CEA_NET_WIRELENGTH : 8.0
CEA_NET_NAME : NET C
CEA_NET_WIRELENGTH : 50.0

In order to obtain the timing estimates of the design shown in Figure 9, ChipTimeEst has to be executed. Before executing ChipTimeEst the RIF for ChipTimeEst has to be constructed. The following RIF can be used for that purpose :

%CHIP NETLIST
CET_NETLIST_FILENAME : example.vhdl
CET_NETLIST_FORMAT : VHDL

%GEOMETRIC FILE
CEA_CHIP_WIDTH : 70.0
CEA_CHIP_HEIGHT : 60.0
CEA_COMPONENT_NAME : ADDER
CEA_COMPONENT_XLEFT : 0
CEA_COMPONENT_YLEFT : 0
CEA_COMPONENT_XRIGHT : 45.0
CEA_COMPONENT_YRIGHT : 25.0

CEA_COMPONENT_NAME : REG1
CEA_COMPONENT_XLEFT : 0
CEA_COMPONENT_YLEFT : 30.0
CEA_COMPONENT_XRIGHT : 20.0
CEA_COMPONENT_YRIGHT : 59.0

CEA_COMPONENT_NAME : REG2
CEA_COMPONENT_XLEFT : 25.0
CEA_COMPONENT_YLEFT : 30.0
CEA_COMPONENT_XRIGHT : 55.0
CEA_COMPONENT_YRIGHT : 59.0

```
CEA_COMPONENT_NAME : REG3
CEA_COMPONENT_XLEFT : 50.0
CEA_COMPONENT_YLEFT : 30.0
CEA_COMPONENT_XRIGHT : 70.0
CEA_COMPONENT_YRIGHT : 59.0

%WIRELENGTH FILE
CEA_NET_NAME : NET A
CEA_NET_WIRELENGTH : 5.0
CEA_NET_NAME : NET B
CEA_NET_WIRELENGTH : 8.0
CEA_NET_NAME : NET C
CEA_NET_WIRELENGTH : 50.0

%COMPONENT FILE
CE_COMPONENT_NAME : Adder
CE_NUM_TUPLES : 2
CE_SHAPE_TUPLE : 30.0,40.0
CE_COMPONENT_DELAY: 20
CE_SHAPE_TUPLE : 45.0,25.0
CE_COMPONENT_DELAY: 25
CE_COMPONENT_NAME : Register
CE_NUM_TUPLES : 1
CE_SHAPE_TUPLE : 20.0,29.0
CE_COMPONENT_DELAY: 10
```

The results of ChipTimeEst are present in ROF. The following ROF is obtained by ChipTimeEst for the example shown in Figure 9:

```
%TIMING FILE
CET_CLOCK_NAME :Net D
CET_CLOCK_PERIOD :60.0
CET_NUM_PATHS :4
CET_PATH_NUM_PINS : 4
CET_PATH_LIST : Reg2.2, Adder.4, Adder.5,Reg3.6
```

5 Appendix A

ChipEstArea Users Manual – 7 December 1993 ("U. C. Irvine")

ChipEstArea – Performs Chip level Area Estimation

SYNOPSIS

ChipEstArea [**-D** *Defaults* Modifier File Name] **-I** *Required* Inputs File name **-O** *Results* Output File Name

DESCRIPTION

ChipEstArea performs a Area Estimation for the chip level whose netlist description in VHDL format has been given. **ChipEstArea** uses two types of information, a set of mandatory inputs and any defaults that need to be modified. Given this information, ChipEstArea produces the outputs in a file.

The mandatory inputs are present in the file whose name is given by Required Inputs File(RIF). The RIF consists of netlist file, component file and the desired aspect ratio information.

The results are stored in the Results Outputs File (ROF). The ROF consists of either a status code if ChipEstArea did not run to completion or the results of the ChipEstArea run, otherwise. The ROF for a successful run consists of geometric file and the wire length file.

The defaults that have been modified are stored in the Defaults Modifier File(DMF). The defaults that can be modified include the technology library, the gate library name and the aspect ratio bounds.

OPTIONS

-D Defaults Modifier File Name This is an optional input. This option specifies the name of the DMF. The file would contain information that would need to redefine any default entries.

-I Required Inputs File Name This is a mandatory input. This option specifies the name of the RIF. The RIF file contains information that are mandatory for running ChipEstArea.

-O Results Output File Name This option specifies where the results of ChipEstArea should be located. It species the name of the Results Output File (ROF). ROF contains the status code is ChipEstArea failed, otherwise, it contains the results of the ChipEstArea run.

FILE FORMAT

Each file consists of a pre-determined number of sections. The information in a section form a close knit group. Each section consists of a header line followed by a list of field name-value pairs, one per line.
The header line begins with a "%" followed by the header information. Each field line consists of a field name, a separator ("COLON"), and a field value in this order. Field names in component information section have "CEA_" prefix. Field values could be a single word or a list of words separated by comma delimiter.

FILES

Required Inputs File

The RIF consists of three sections namely, chip netlist, component file and desired aspect ratio.

The chip netlist specifies the path name of the netlist file and the file format. The netlist file describes the chip as a connection list of components. The components have to be either present in the GENUS component database, or their details have to hierarchically described in another netlist file.

The chip netlist section has two fields (in this order):

CEA_NETLIST_FILENAME : file path name /*file name*/
CEA_NETLIST_FORMAT : VHDL /*netlist format */

The desired aspect ratio specifies the height to width ratio of the chip.

The desired aspect ratio has one field:

CEA_ASPECT_RATIO : float /*aspect ratio */

The component file specifies the component shape function and delay obtained from GENUS for a number of aspect ratios. Each point on the shape function is represented by a shape tuple consisting of height, width and delay. There could be a number of shape tuples, depending on the number of points on the shape function.

The component information section has four (or multiples thereof) fields (in this order):

CE_COMPONENT_NAME : component name /* component name */
CE_NUM_TUPLES : Int /* number of tuples */
CE_SHAPE_TUPLE : float,float,float /* X, Y, T */

Defaults Modifier File This file consists of the defaults that need to be modified. Typically, the defaults information includes the technology library pathname.

The DMF has four fields in the order given below :

CEA_GATE_LIB : file path name /* gate library file name */
CEA_TECH_LIB : file path name /* technology library file name */
CEA_UPPER_ASP: float /* upper aspect ratio */
CEA_LOWER_ASP: float /* lower aspect ratio */

Results Output File

The ROF consists of the geometric file and the wirelength file.
The geometric file describes the chip shape in terms of width and height of the chip. It also describes the location of the components on the chip.

The geometric file has fields in the order given :

CEA_CHIP_WIDTH : float /* chip width (macro) */
CEA_CHIP_HEIGHT: float /* chip height (macro) */

For every component in the netlist the following seven fields exist in the order shown below :

CEA_COMPONENT_NAME : character string /* component name */
CEA_COMPONENT_XLEFT: float /* left x_coordinate */
CEA_COMPONENT_YLEFT: float /* left y_coordinate */

CEA_COMPONENT_XRIGHT: float /* right x_coordinate */
CEA_COMPONENT_YRIGHT: float /* right y_coordinate */

CEA_COMPONENT_WIDTH: float /* component width */
CEA_COMPONENT_HEIGHT: float /* component height */

The wirelength file indicates the length of each of the nets in the netlist description. The net wirelength information section has two (or multiples of two) fields in the order given below :
CEA_NET_NAME : character string /* net name */
CEA_NET_WIRELENGTH: float /* net wire length */

6 Appendix B

ChipEstTime Users Manual – 3 December 1993 ("U. C. Irvine")
ChipEstTime – Perform Chip level Timing Estimation

SYNOPSIS
ChipEstTime [**-D** *Defaults* Modifier File Name] **-I** *Required* Inputs File name **-O** *Results* Output File Name

DESCRIPTION
ChipEstTime performs a Timing Estimation for the chip level netlist whose connectivity description in VHDL format has been given. **ChipEstTime** uses two types of information, Required Inputs which are mandatory and modified defaults. Based on this information ChipEstTime performs Timing Estimation and produces the results in a file.
The Required Inputs are present in the Required Inputs File (RIF) whose name is given by Required Inputs File Name. The RIF consists of four sections namely, the chip netlist, the geometric file, the component file and the wirelength file.
The modified defaults are present in the Defaults Modifier file (DMF). ChipEstTime uses predetermined values for the defaults unless modified by the entries in DMF. DMF consists of technology library information.
The Results Outputs are produced in the Results Outputs File (ROF) whose name is given by Results Outputs File Name. ROF consists of either a status code if ChipEstTime did not run to completion or the results of the ChipEstTime run, otherwise. The RO file for a successful run consists of the timing file consisting of Clock information and worst case path information.

OPTIONS
-D Defaults Modifier File Name This is an optional argument. The entry specifies the name of the file would contain information needed to redefine any default entries.
-I Required Inputs File Name This argument is mandatory for running ChipEstTime. This entry specifies the name of the file containing the required inputs.
-O Results Output File Name Again, this is a mandatory argument. It specifies the name of the file that would contain the results produced by ChipEstTime.

FILE FORMAT
Each file consists of a pre-determined number of sections. The information in a section form a close knit group. Each section consists of a header line followed by a list of field name-value pairs, one per line.

The header line begins with a "%" followed by the header information. Each field line consists of a field name, a separator ("COLON"), and a field value in this order. Field names in component information section have "CET_" prefix. Field values could be a single word or a list of words separated by comma delimiter.

FILES

Required Inputs File

This file contains three sections containing the information about the chip netlist, the geometric file, the component file and the wirelength file.

The chip netlist has 2 fields(in this order)

```
CET_NETLIST_FILENAME : file path name          /* file name */
CET_NETLIST_FORMAT : VHDL                      /* netlist format */
```

The geometric file consists of the height and the width of the chip and the location of the components on the chip.

The geometric file has fields in the order given :

```
CEA_CHIP_WIDTH : float                                /* chip width */
CEA_CHIP_HEIGHT: float                                /* chip height */

CEA_COMPONENT_NAME : character string  /* component name */
CEA_COMPONENT_XLEFT: float              /* left x_coordinate */
CEA_COMPONENT_YLEFT: float              /*left y_coordinate */

CEA_COMPONENT_XRIGHT: float             /* right x_coordinate */
CEA_COMPONENT_YRIGHT: float             /* right y_coordinate */

CEA_COMPONENT_WIDTH: float              /* component width */
CEA_COMPONENT_HEIGHT: float             /* component height */
```

The wirelength file consists of the a net name and its corresponding wirelength value for every net in the netlist description.

The net wirelength description section has 2 fields(or multiples thereof)

```
CET_NET_NAME : character string                   /* net name */
CET_NET_WIRELENGTH : float                   /* net wire length */
```

The component file has four (or more) fields (in this order):

```
CE_COMPONENT_NAME : component name
CE_NUM_TUPLES : Int
CE_SHAPE_TUPLE : float,float,float
```

Defaults Modifier File

This file consists of information whose default values can be modified. It basically can consist of the technology library.

The DMF has three fields

CET_TECH_LIB : character string /* technology library name */
CET_GATE_TIMING_LIB : character string /*timing library name */
CET_NUM_PATHS : int /* number of worst case paths */

Results Output File

This file consists of timing file for a successful ChipEstTime run, which includes the clock information and the worst case path and delay information.
The clock information section consists of the clock net name and the clock period.

The clock information section has 2 fields(or multiples thereof)

CET_CLOCK_NAME : character string /* clock name */
CET_CLOCK_PERIOD : float /* the clock period */
CET_NUM_PATHS : int /* the number of worst case paths */

The worst case path information section consists of the number of pins on the path and the list of composite pins on that path. The composite pin name consists of a component name followed by a dot and concluded by a name of the pin on the component. For example, a composite pin name could be mux2.I0.

The worst case path information section two fields (or multiples thereof) each having the same format :

CET_PATH_NUM_PINS : Int /* the number of pins on the path */
CET_PATH_LIST : composite pin,... /* pin list on the path */

7 References

[1] N. Dutt and P. Jha. Genus: A generic component library for high level synthesis. Technical report, ICS Department, UC Irvine, 1992.

[2] C. Ramachandran. *Area and Delay Estimation Techniques for Top-Down VLSI Chip Design.* PhD thesis, Dept. of ECE, Univ. of California, Irvine, To be submitted in 1994.

[3] C. Ramachandran and F. Kurdahi. Compest interface report. Technical report, ECE Department, UC Irvine, 1993.