ESE Front End

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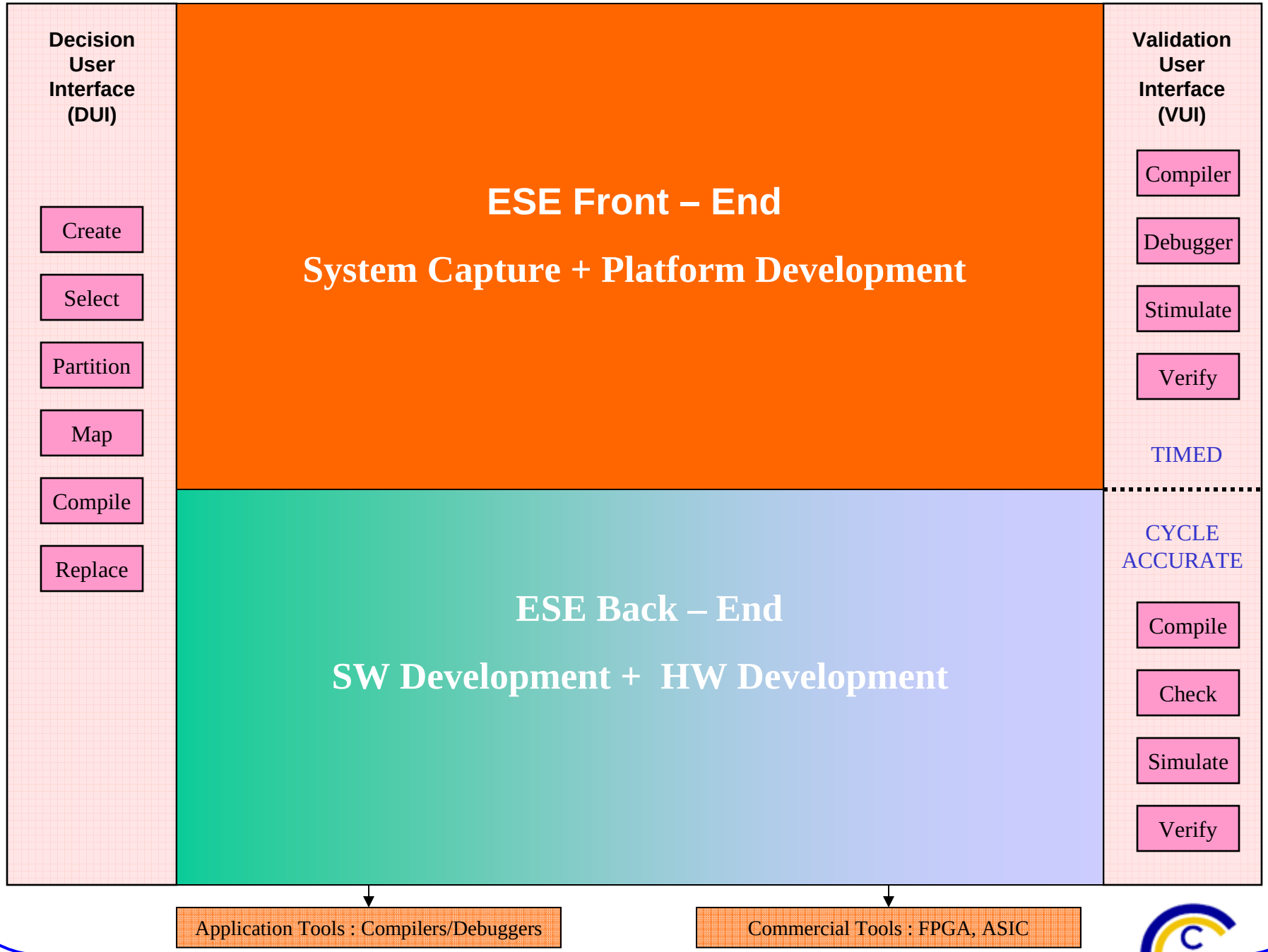
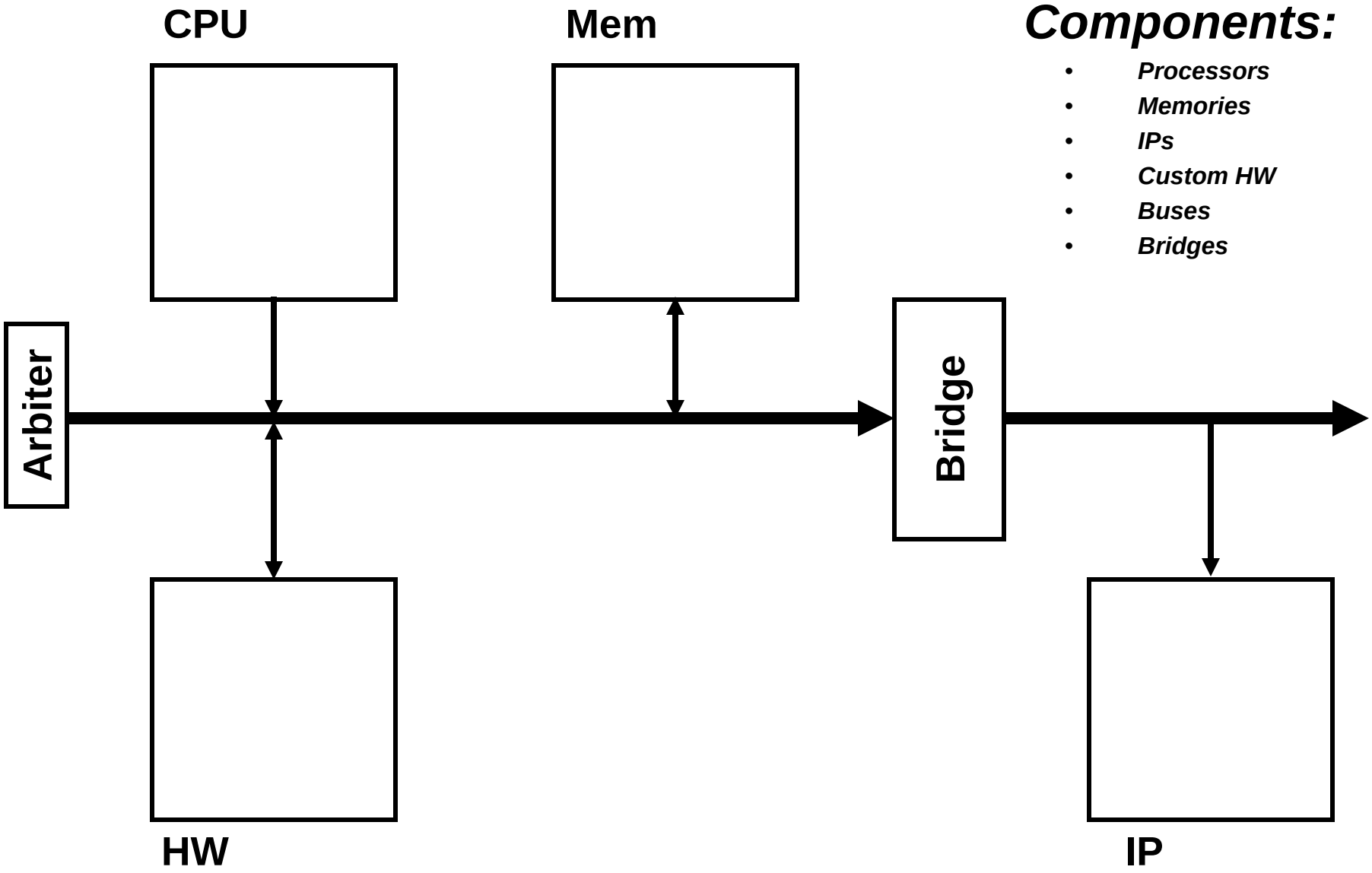
Technology Advantages

- **No basic change in design methodology required**
  - ESE methodology follows present manual design process
- **Productivity gain of more then 1000X demonstrated**
  - Designers do not write models
- **Simple change management: 1-day change**
  - No rework for new design decisions
- **High error-reduction: Automation + verification**
  - Error-prone tasks are automated
- **Simplified globally-distributed design**
  - Fast exchange of design decisions and easy impact estimates
- **Benefit through derivatives designs**
  - No need for complete redesign
- **Better market penetration through customization**
- **Shorter Time-to-Market through automation**

ES Environment



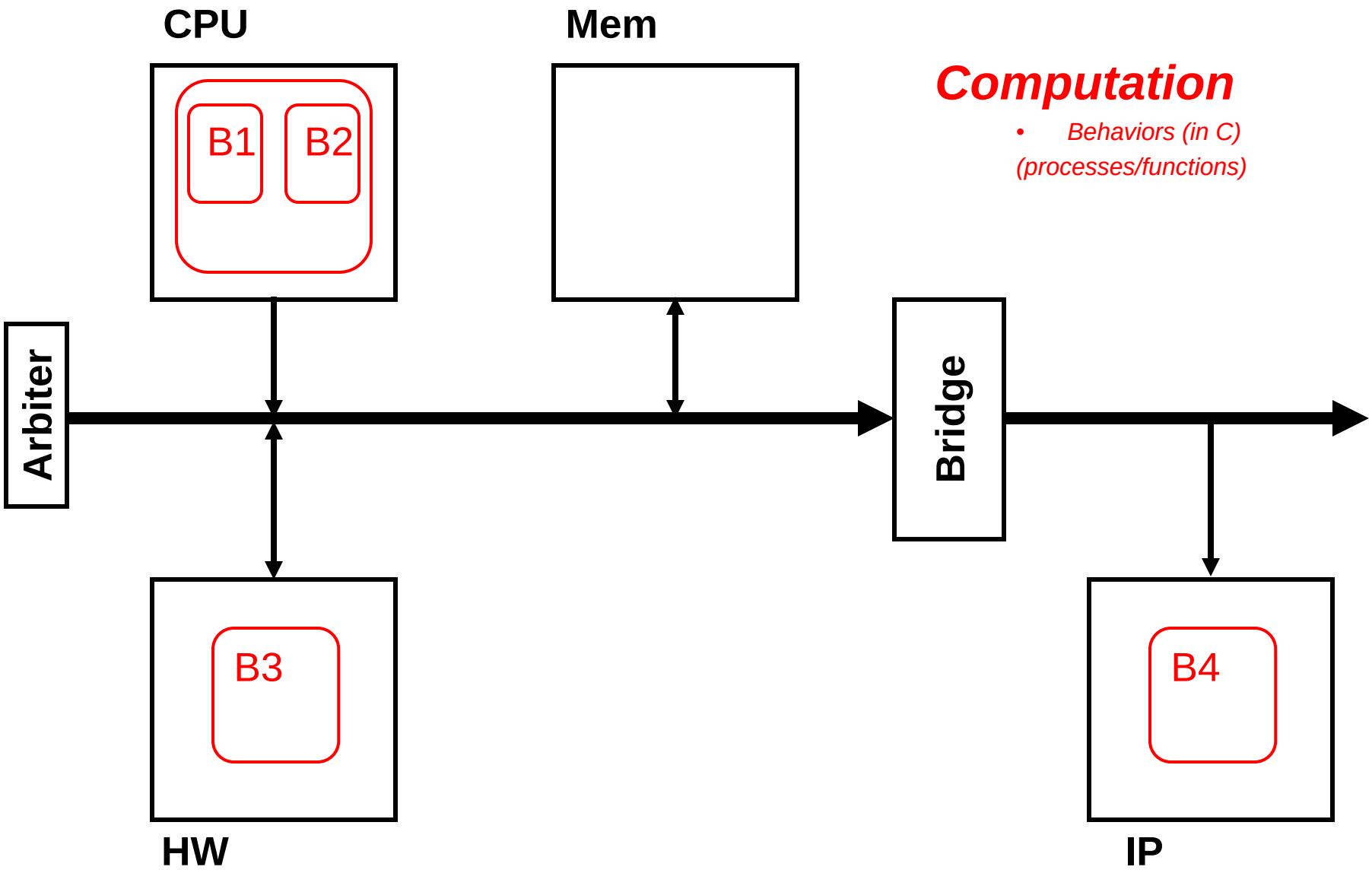
Platform Architecture



Components:

- ***Processors***
- ***Memories***
- ***IPs***
- ***Custom HW***
- ***Buses***
- ***Bridges***

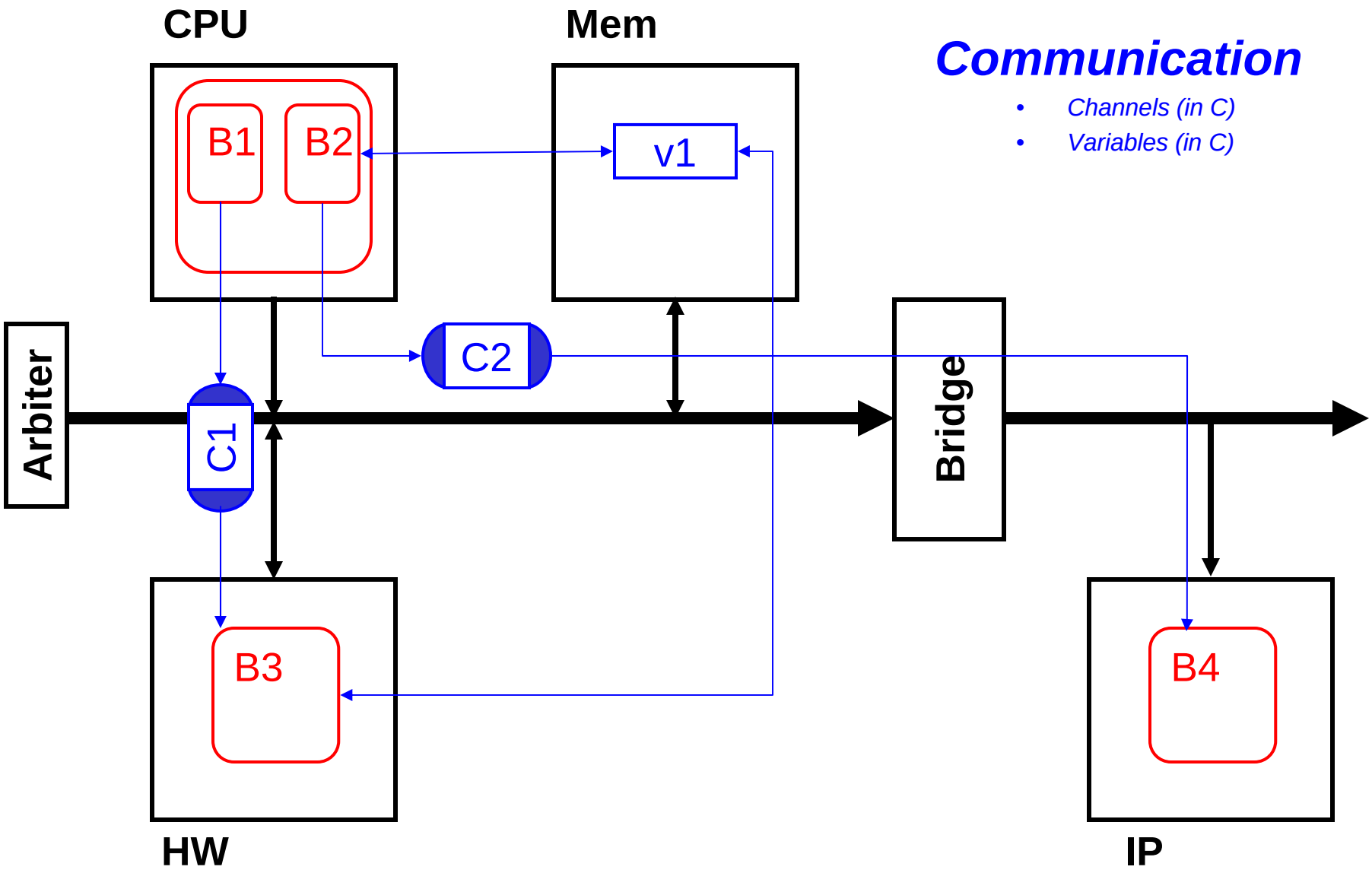
System Definition



Computation

- *Behaviors (in C) (processes/functions)*

System Definition

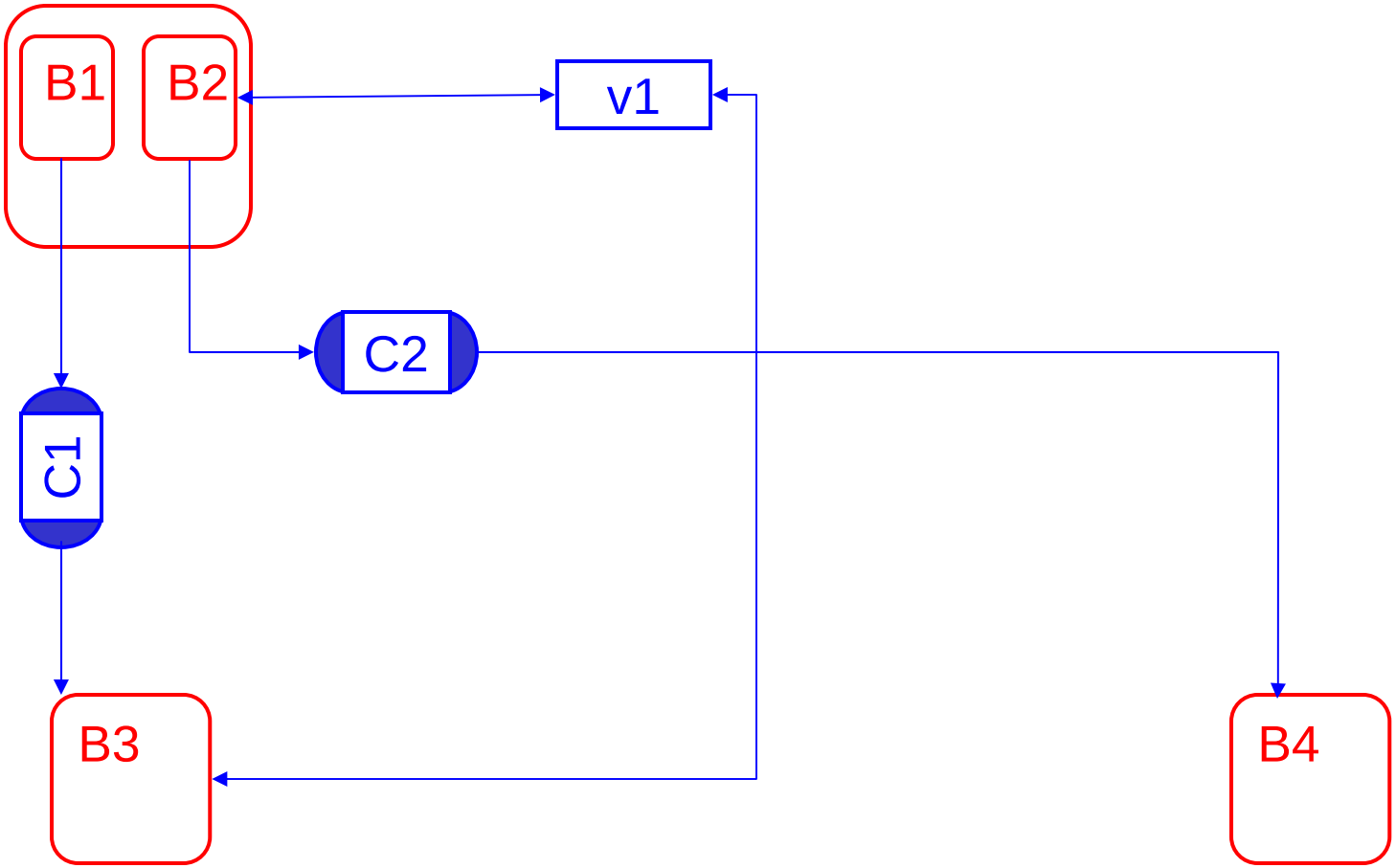


Communication

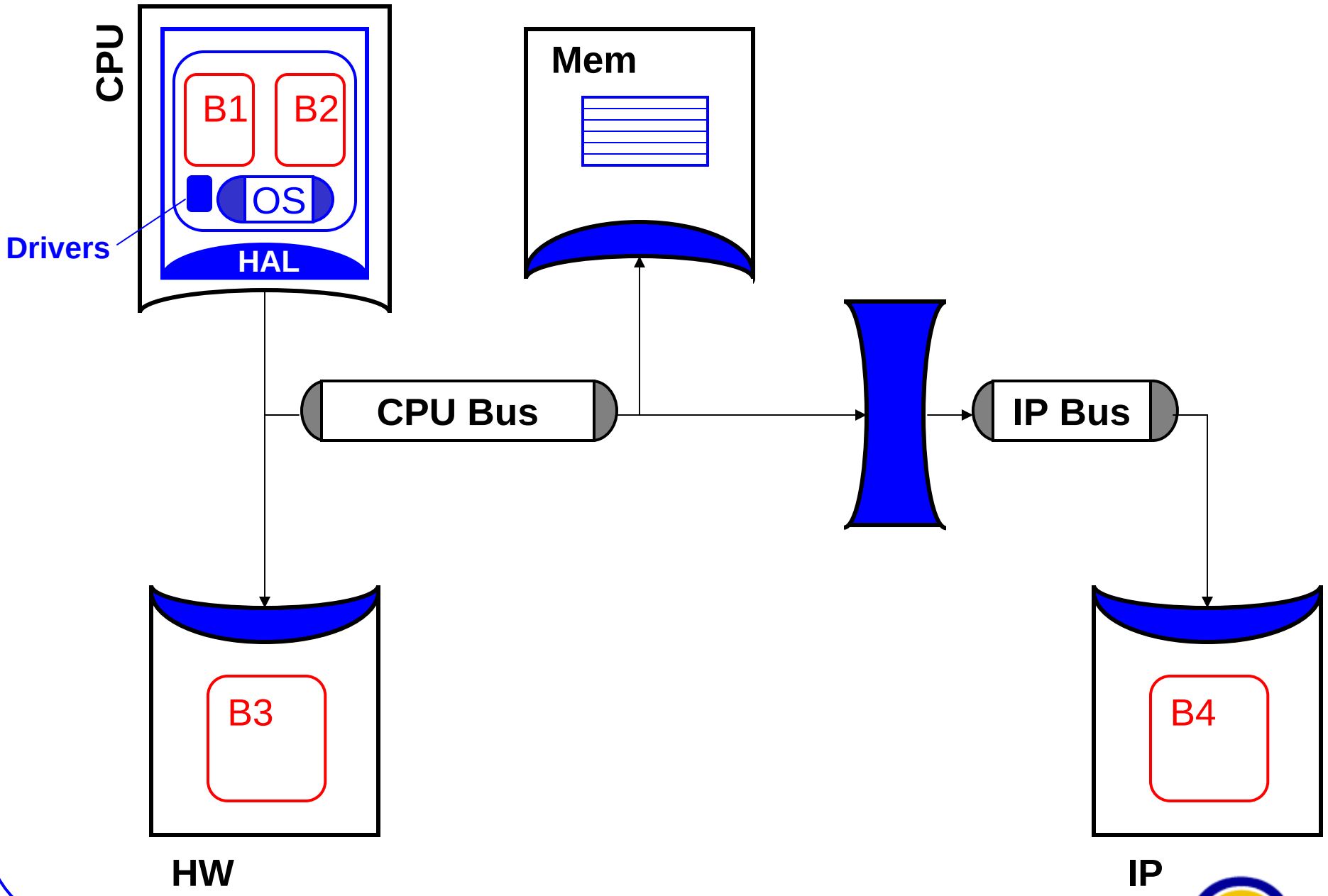
- *Channels (in C)*
- *Variables (in C)*

System Definition* = *(Partial) Platform* + *(Partial) Spec

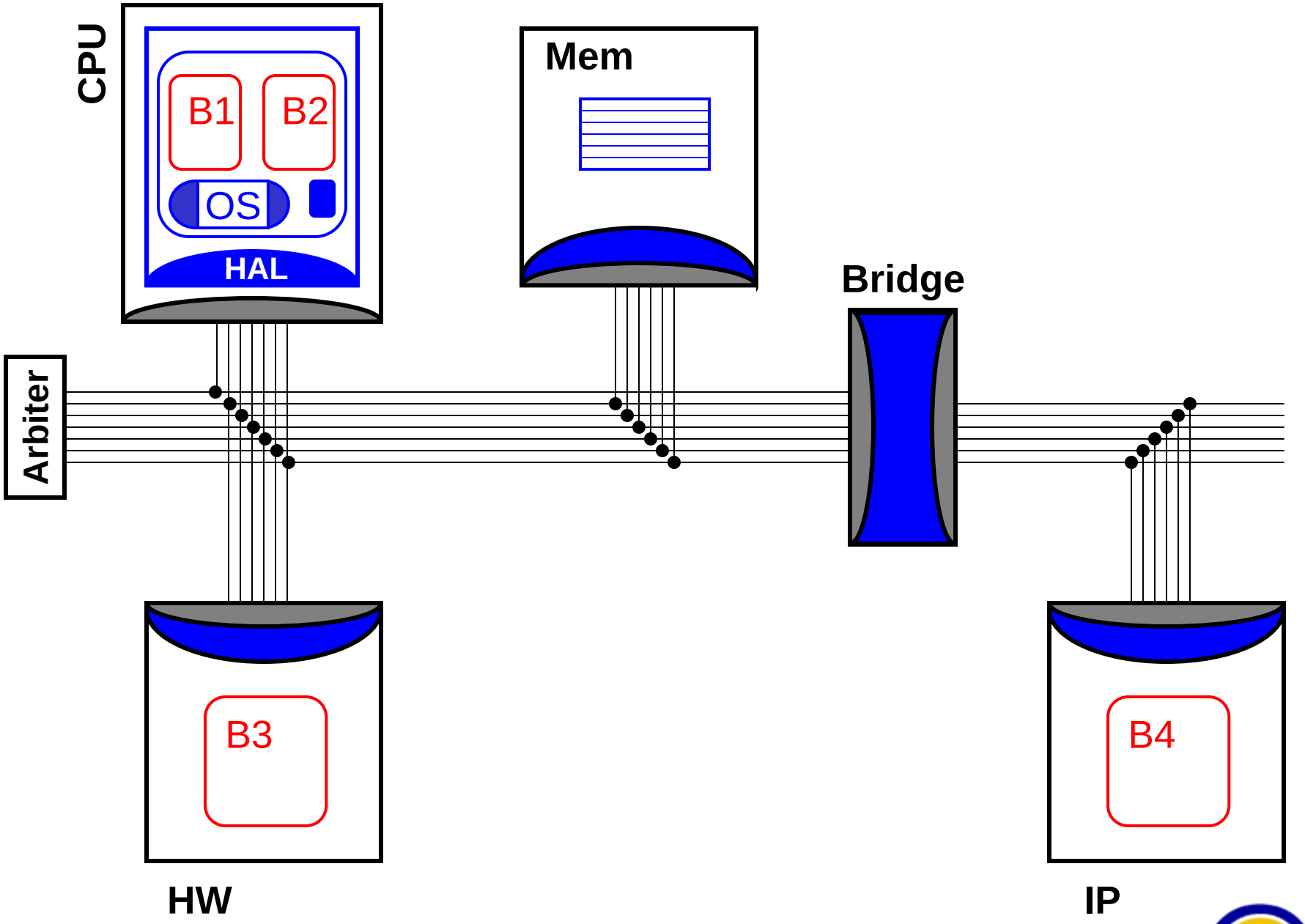
Output: Application Model



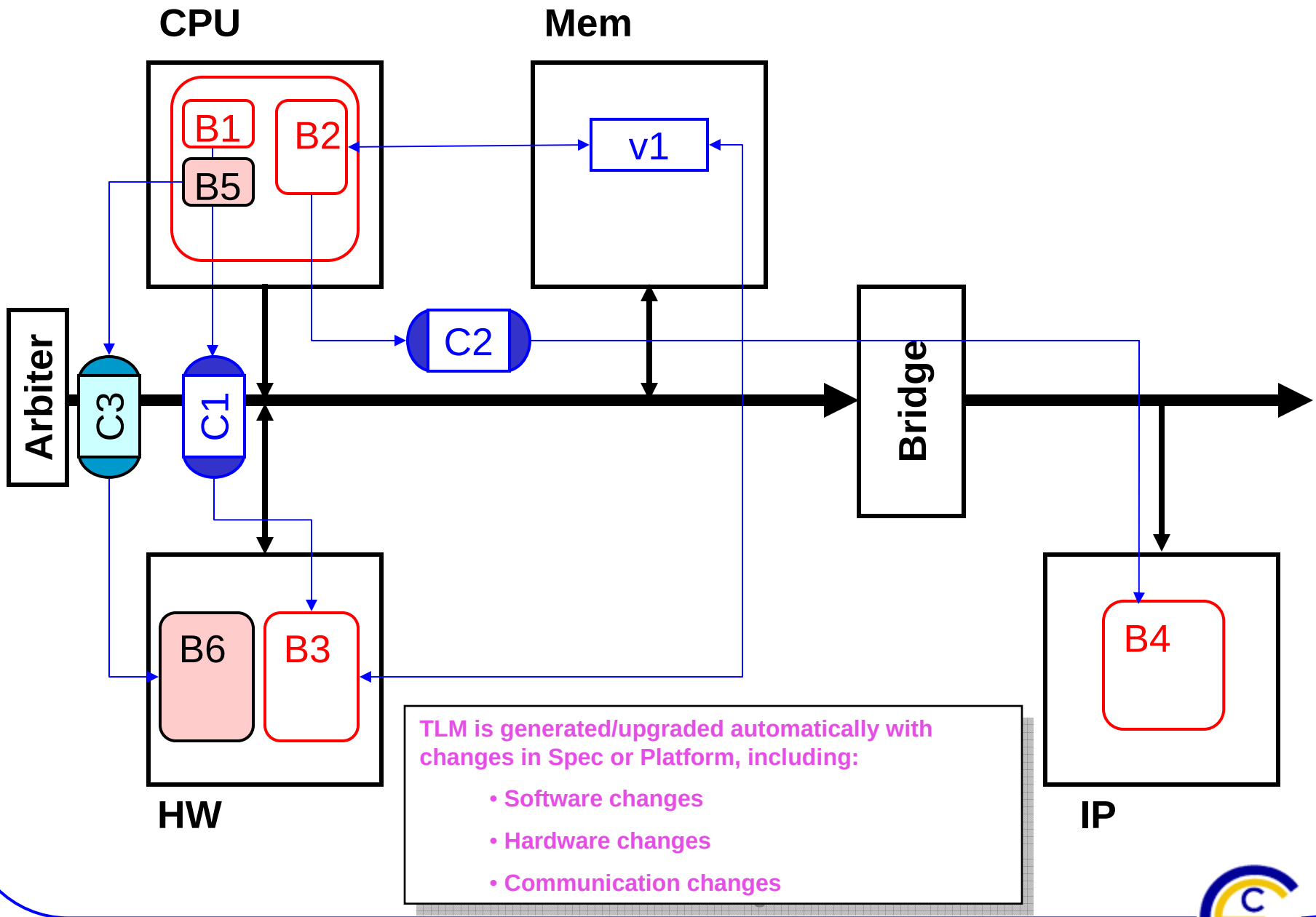
Output: Transaction-Level Model (TLM)



Output: Pin-Accurate Model (PAM)



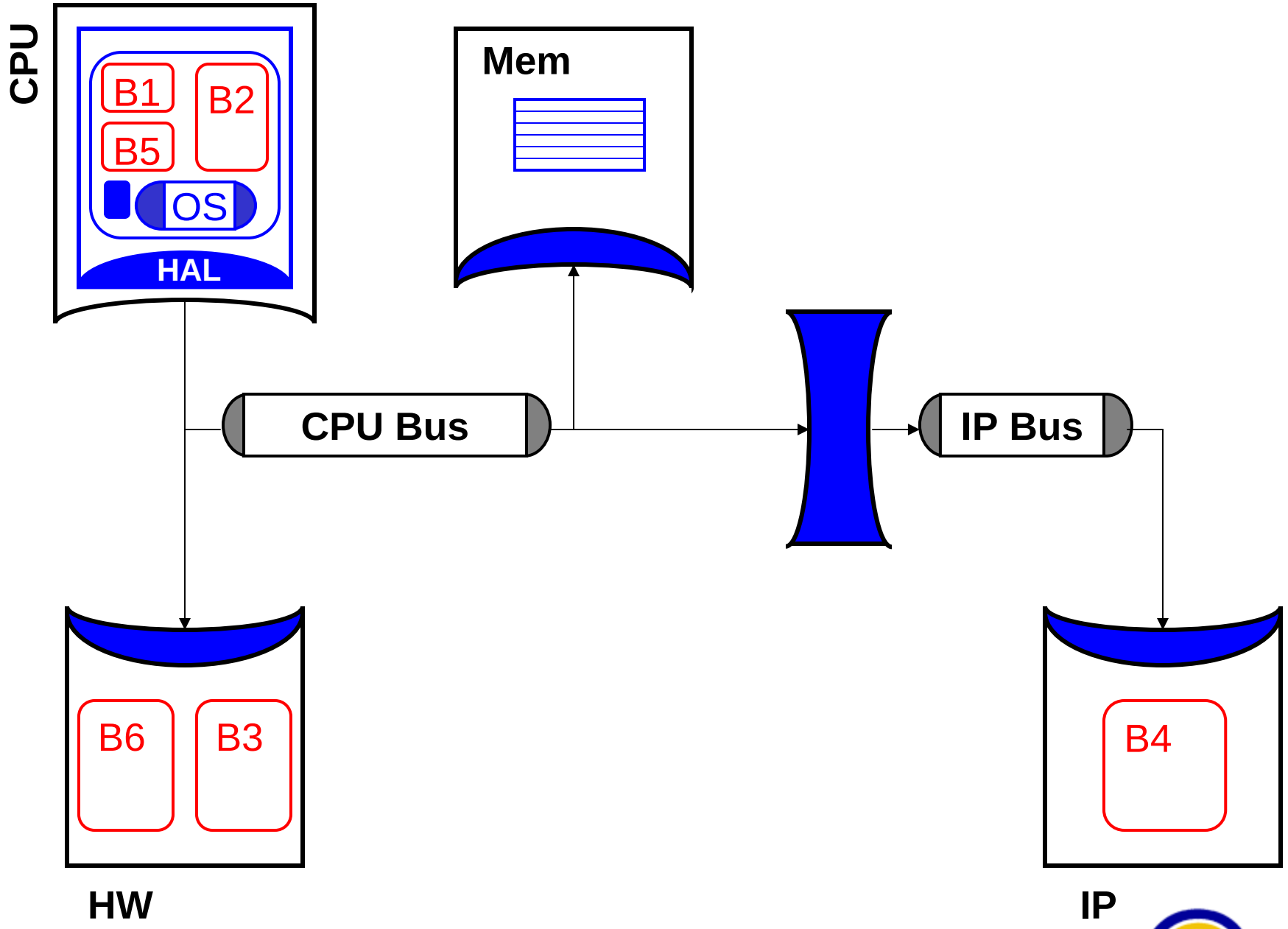
System Modifications



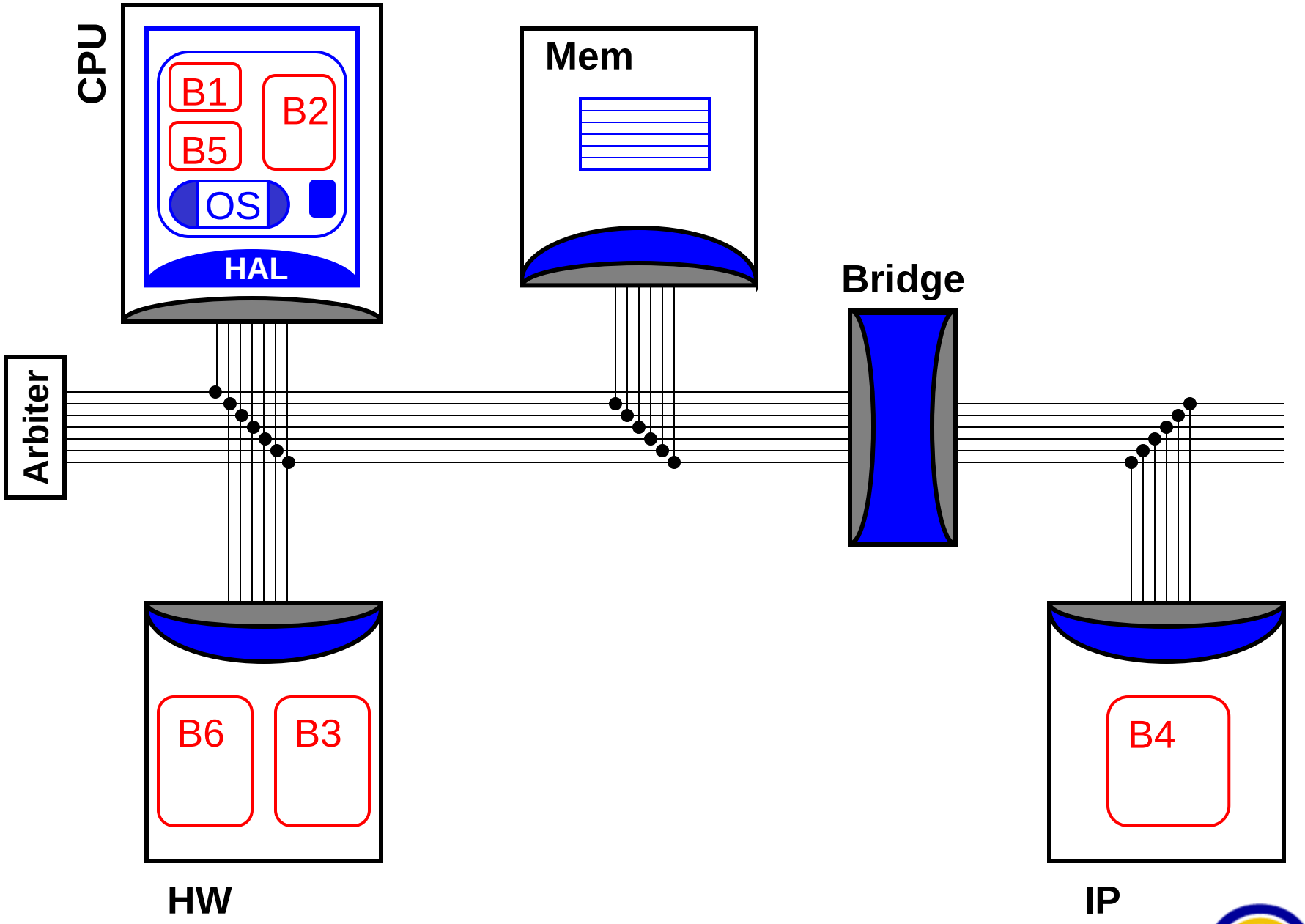
TLM is generated/upgraded automatically with changes in Spec or Platform, including:

- Software changes
- Hardware changes
- Communication changes

Output: Modified TLM

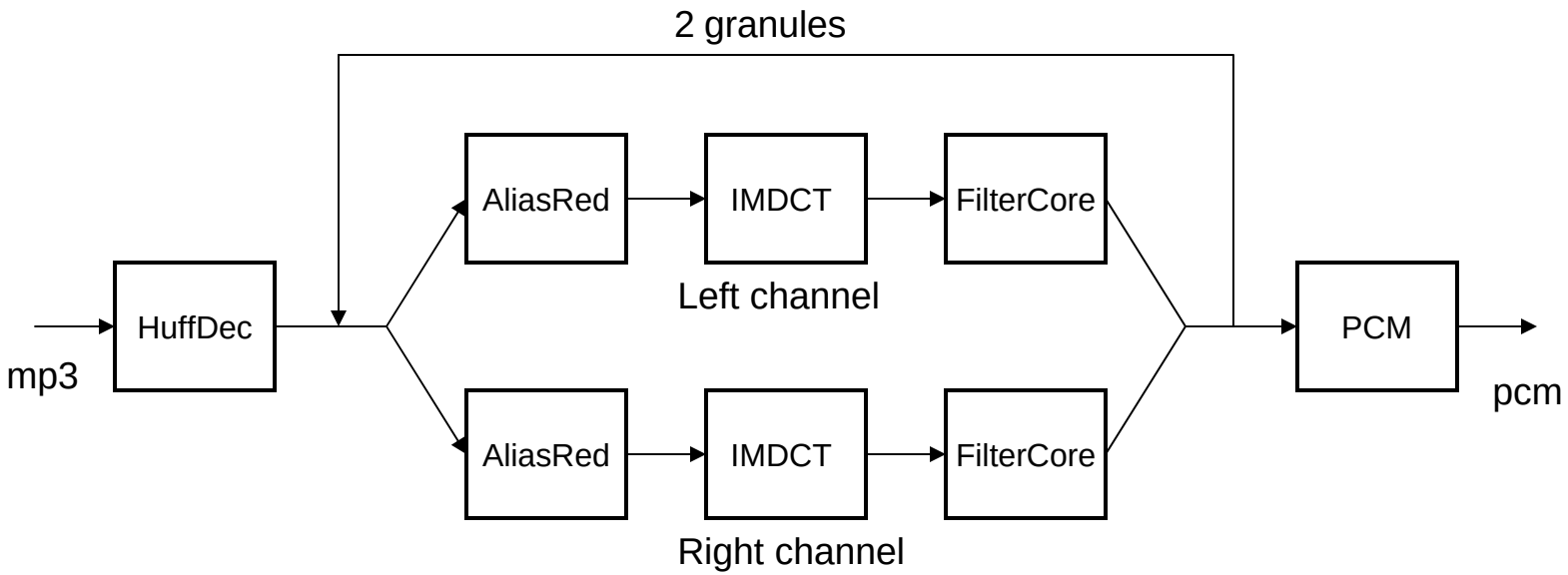


Output: Modified PAM



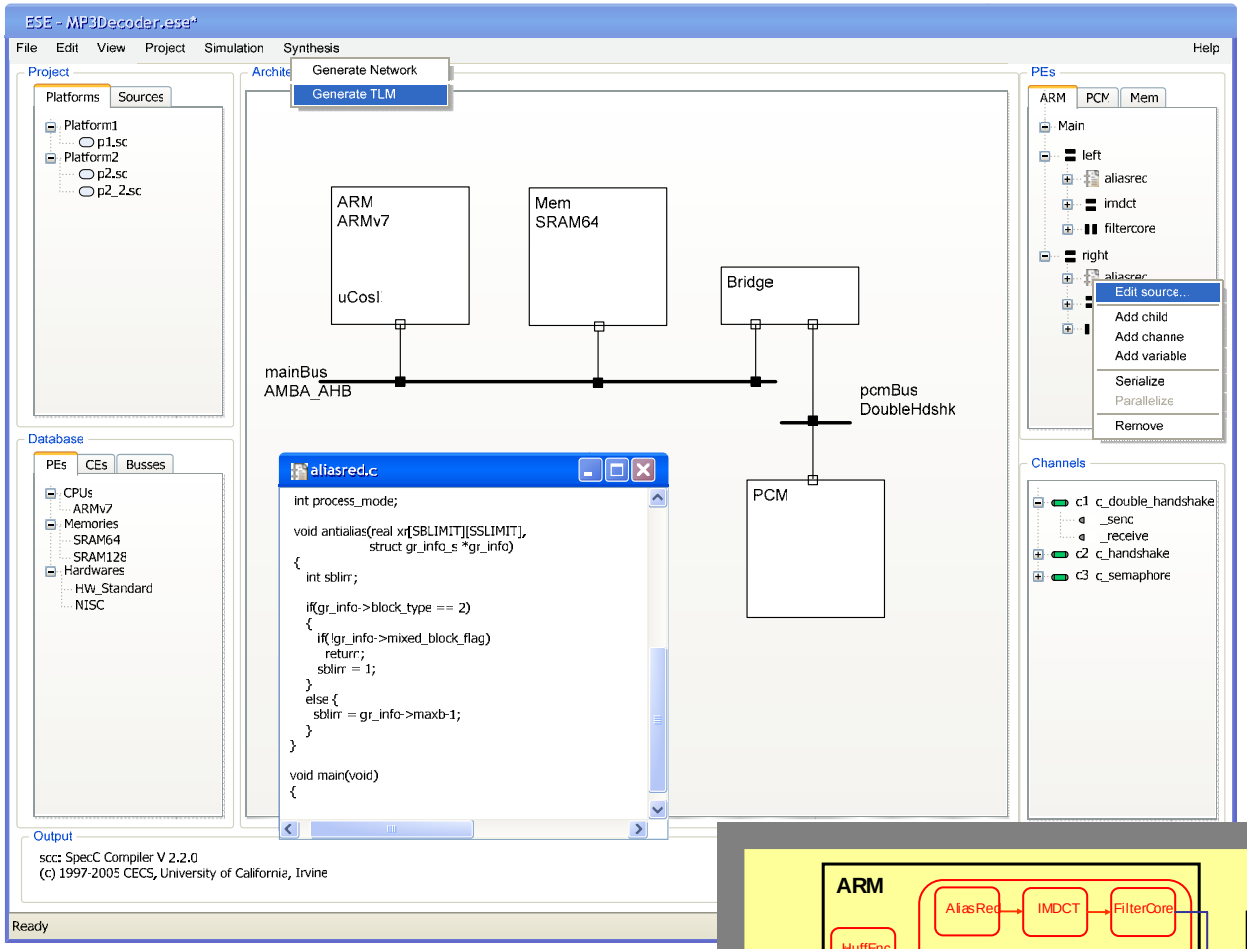
Example: MP3 Decoder

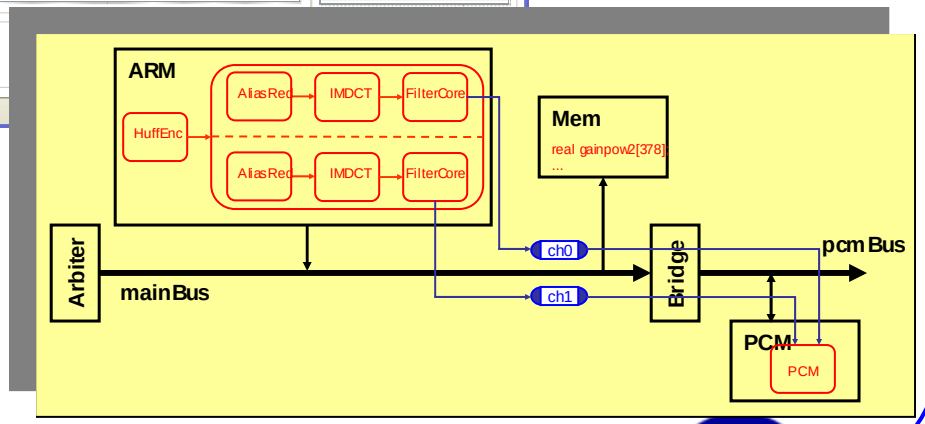
- **Functional block diagram (major blocks only)**



- **Timing constraints**
  - 38 frames per second
  - Frame delay < 26.12ms

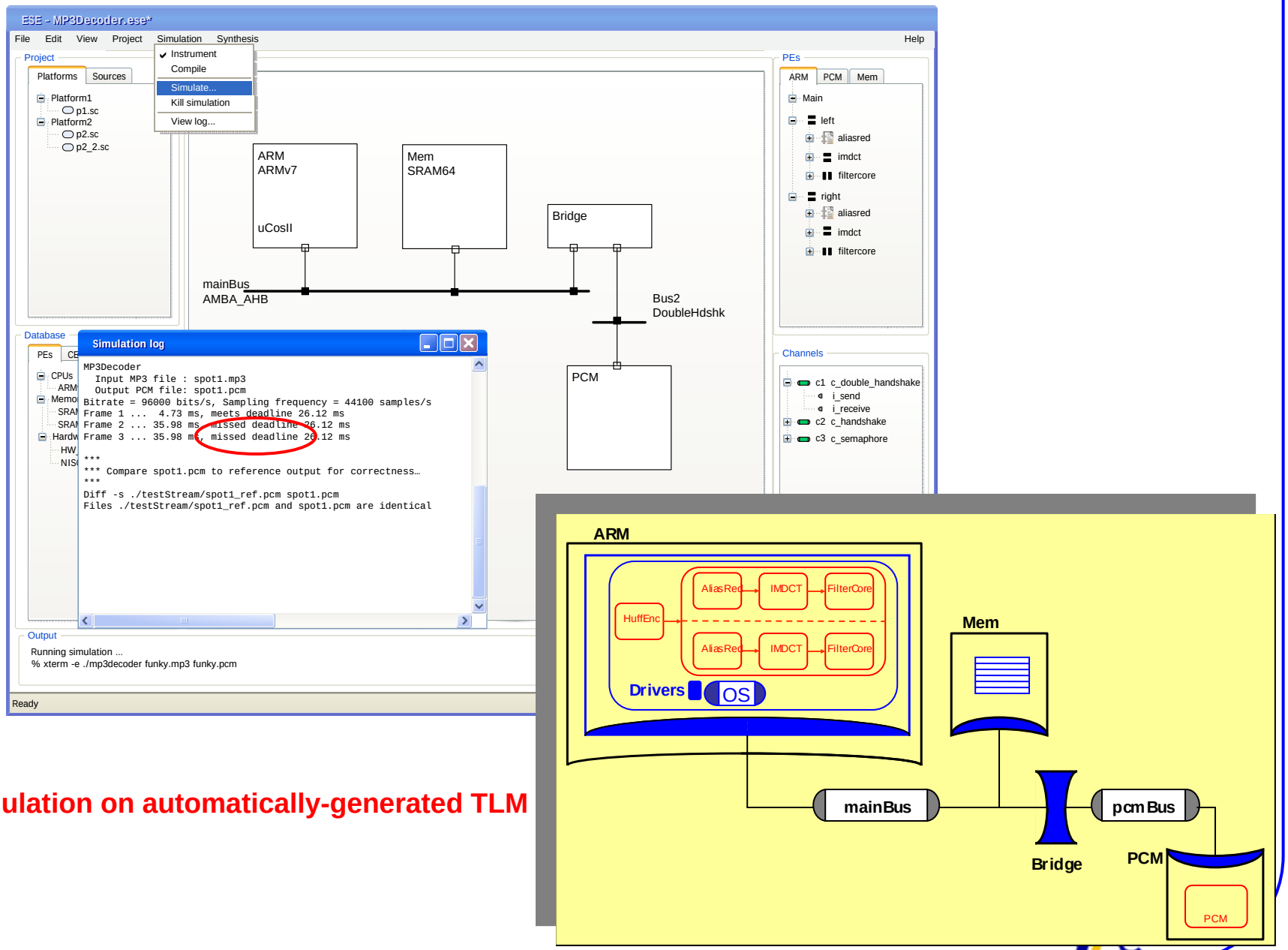
ESE: System Definition





- **Allocate and connect system components**
- **Edit processes (C code) inside components**
- **Insert communication channels and variables**
- **Run transaction-level model generator**

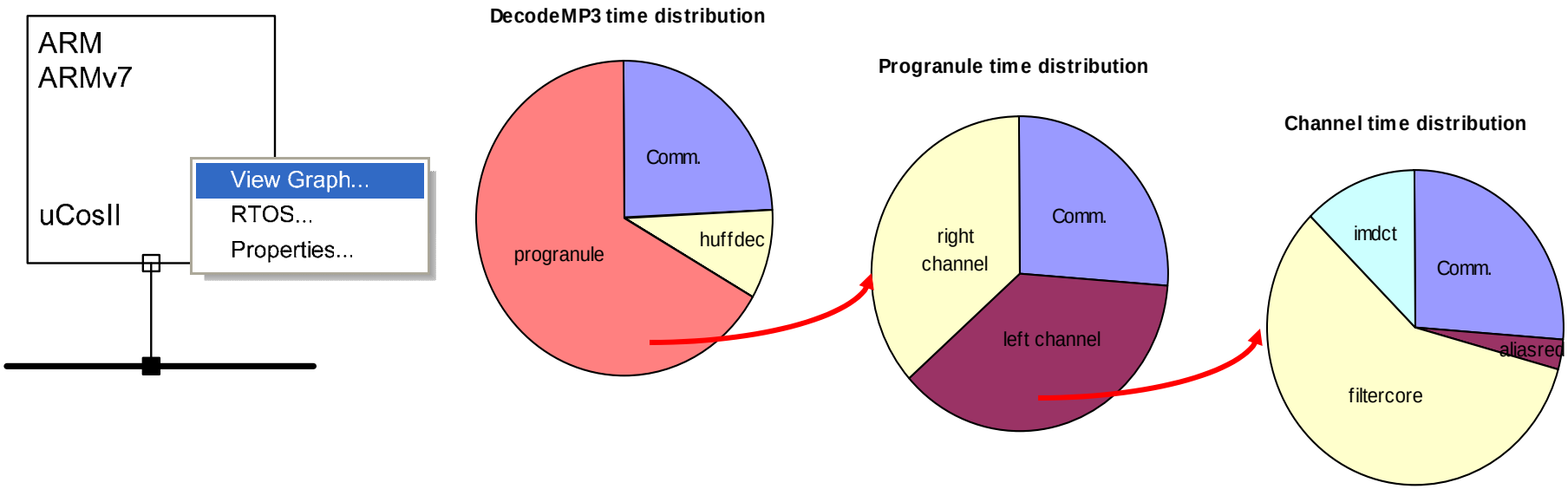
ESE: TLM Simulation



- **Run simulation on automatically-generated TLM**

Computation Analysis

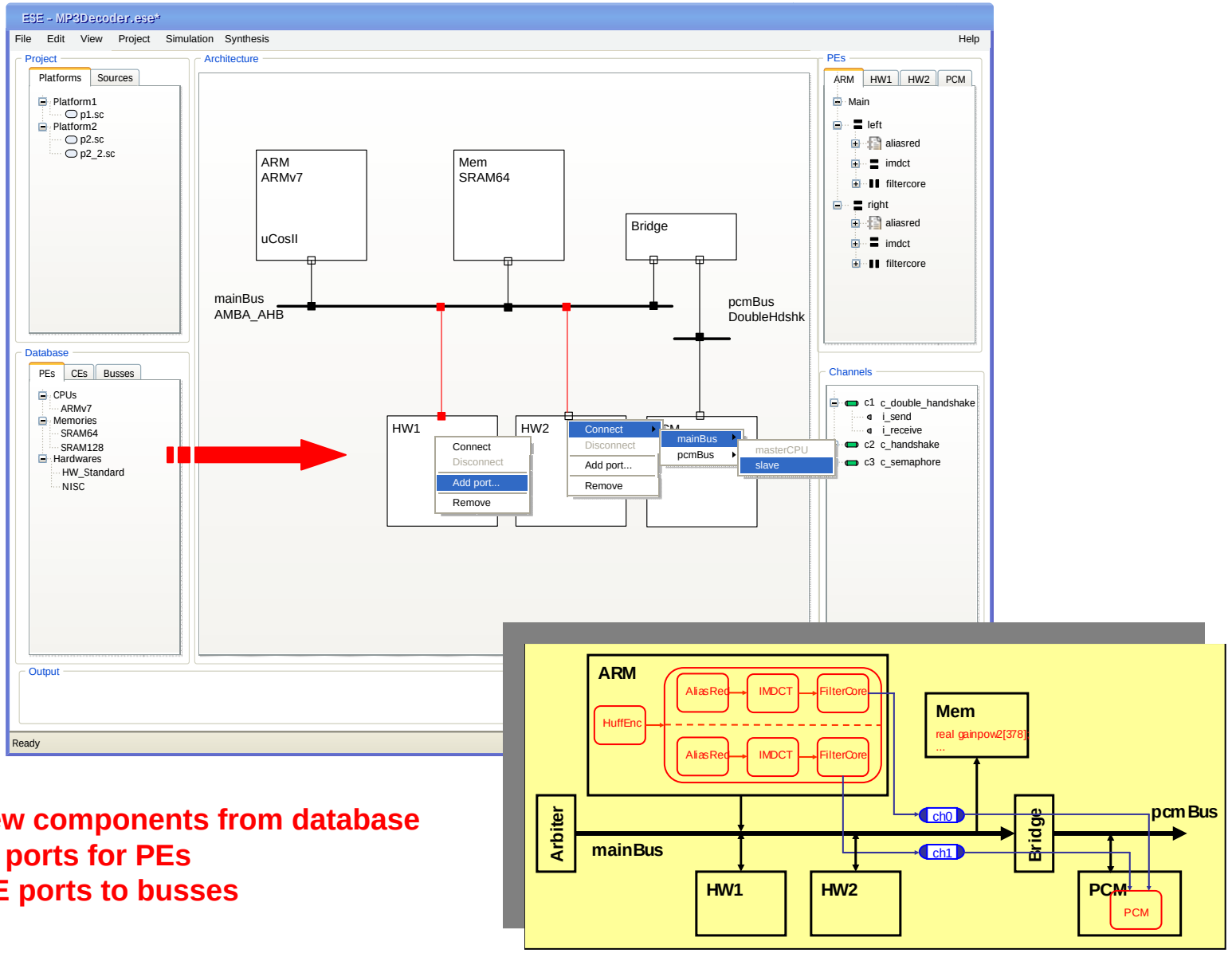
- **View computation time of processes**
  - *filtercore* is the most computation-intensive



- **Look for parallelism in process hierarchy**
  - Left and right *filtercore* processes can run in parallel

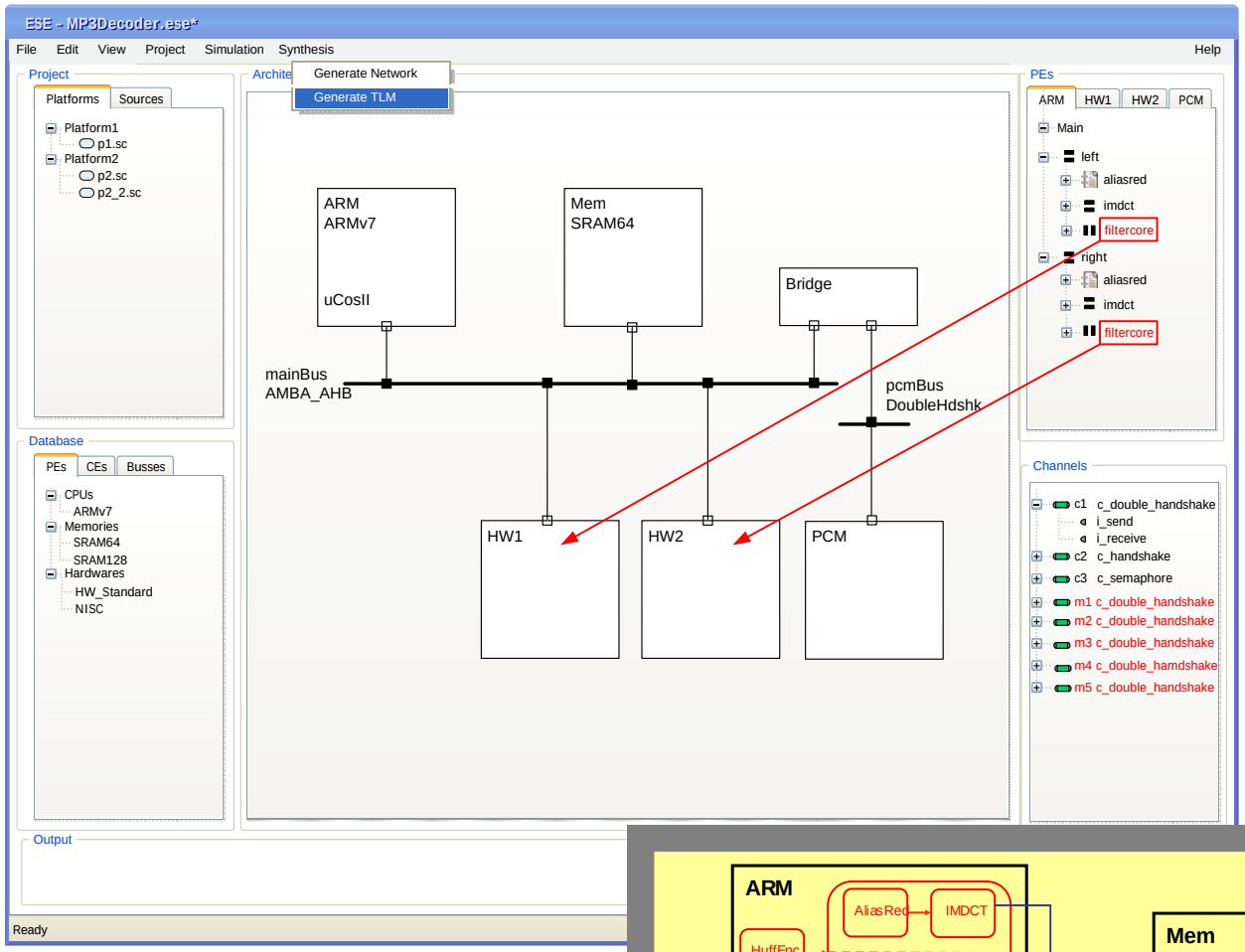
    → Use two identical custom HWs

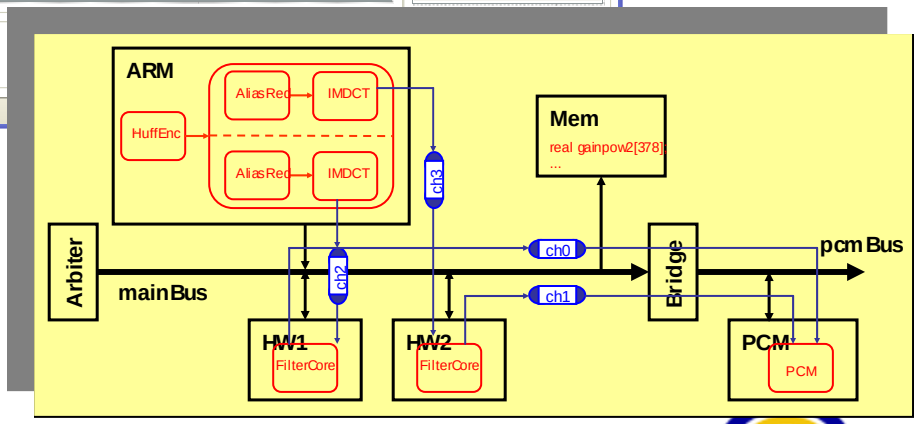
ESE: System Modification (1)



- **Allocate new components from database**
- **Create bus ports for PEs**
- **Connect PE ports to busses**

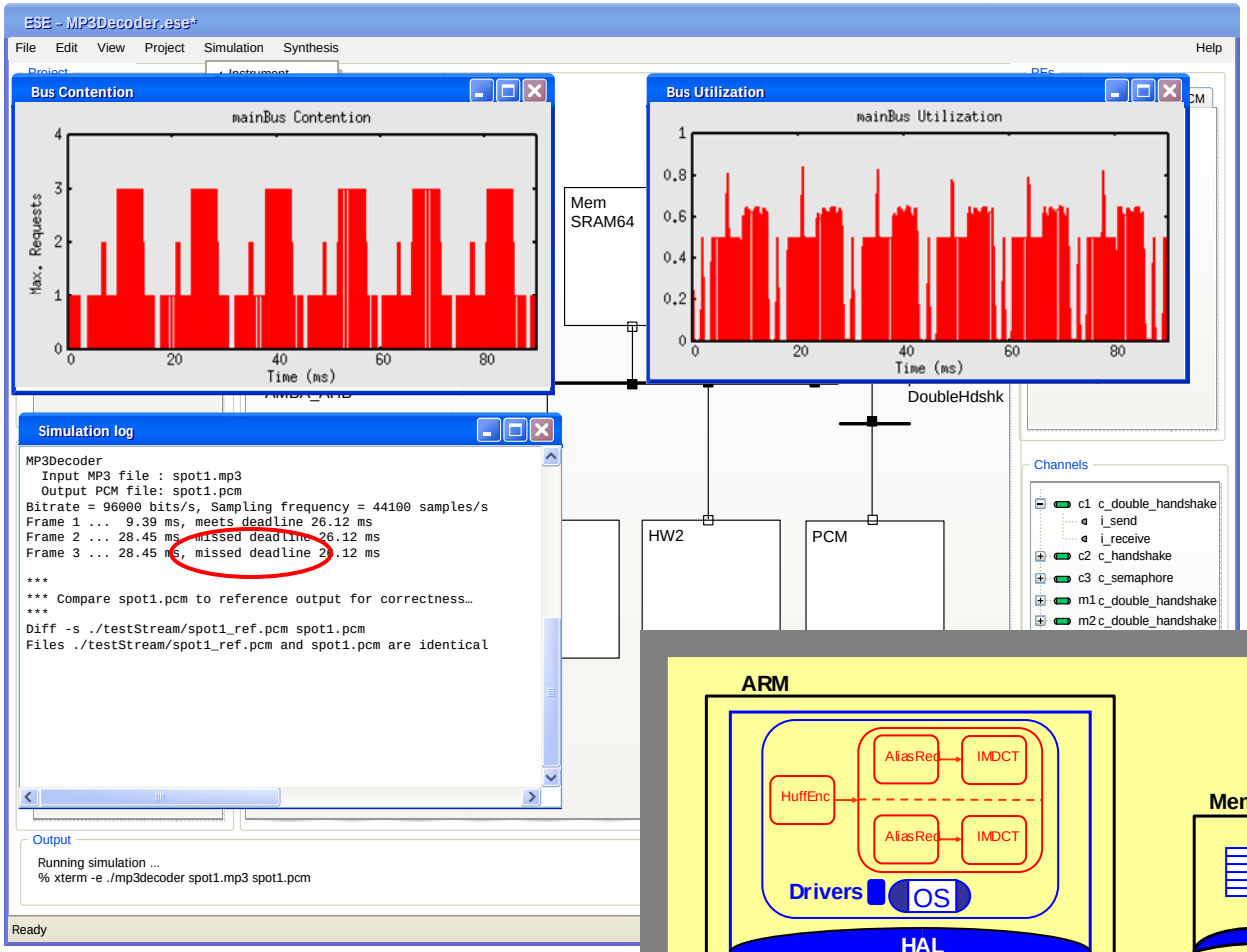
ESE: System Modification (2)

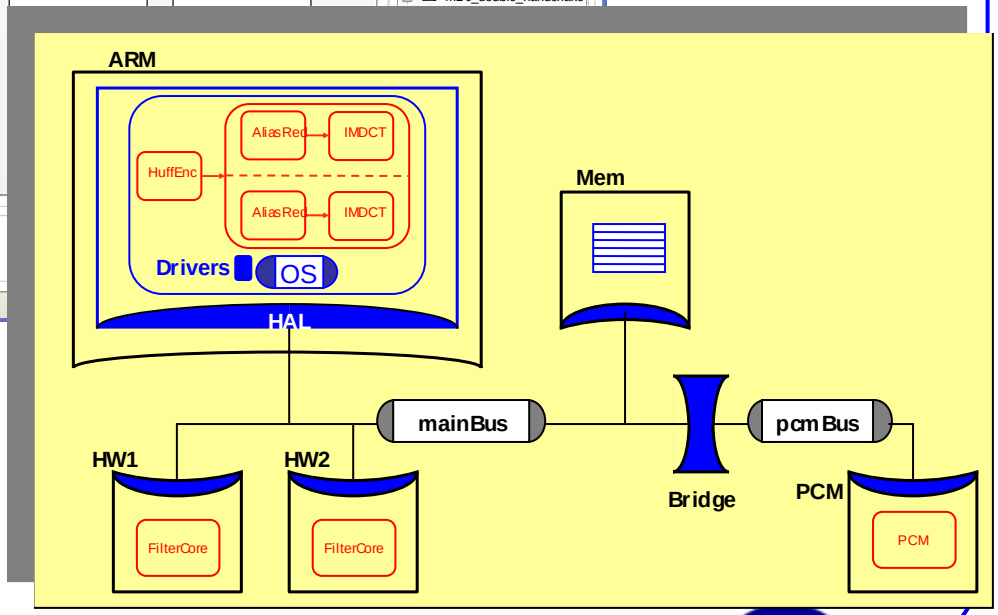




- **Move processes to newly allocated PEs**
- **Inter-PE channels are inserted automatically**
- **Run transaction-level model generator**

ESE: TLM Simulation

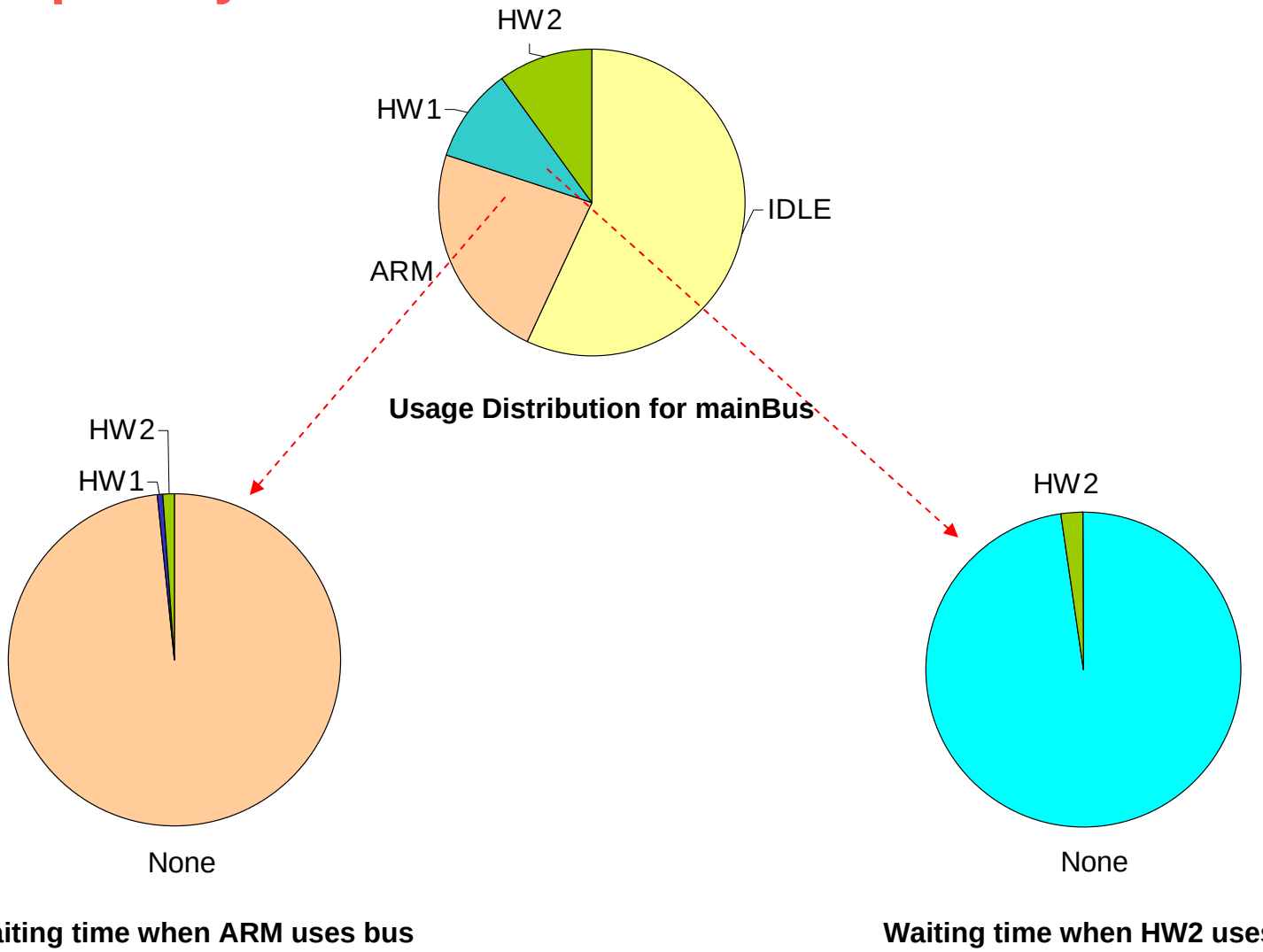




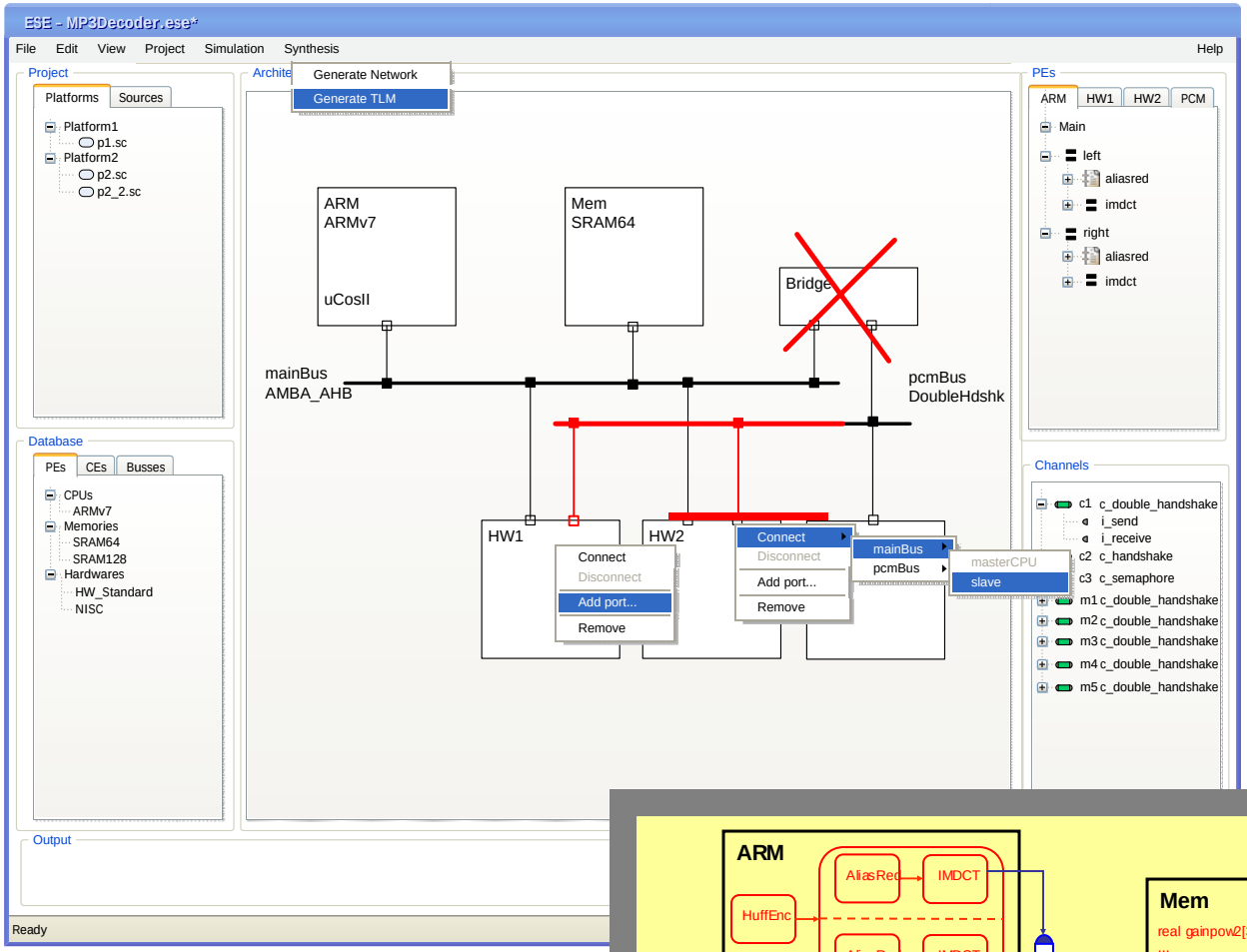
- **Run simulation on automatically-generated TLM**
- **Display over-the-time bus activity**

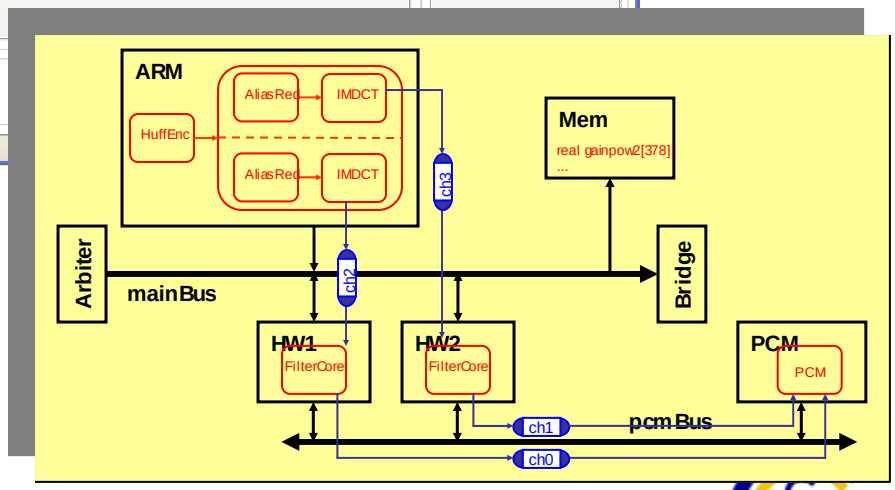
Bus Contention Analysis

- **Bus priority: ARM > HW1 > HW2**



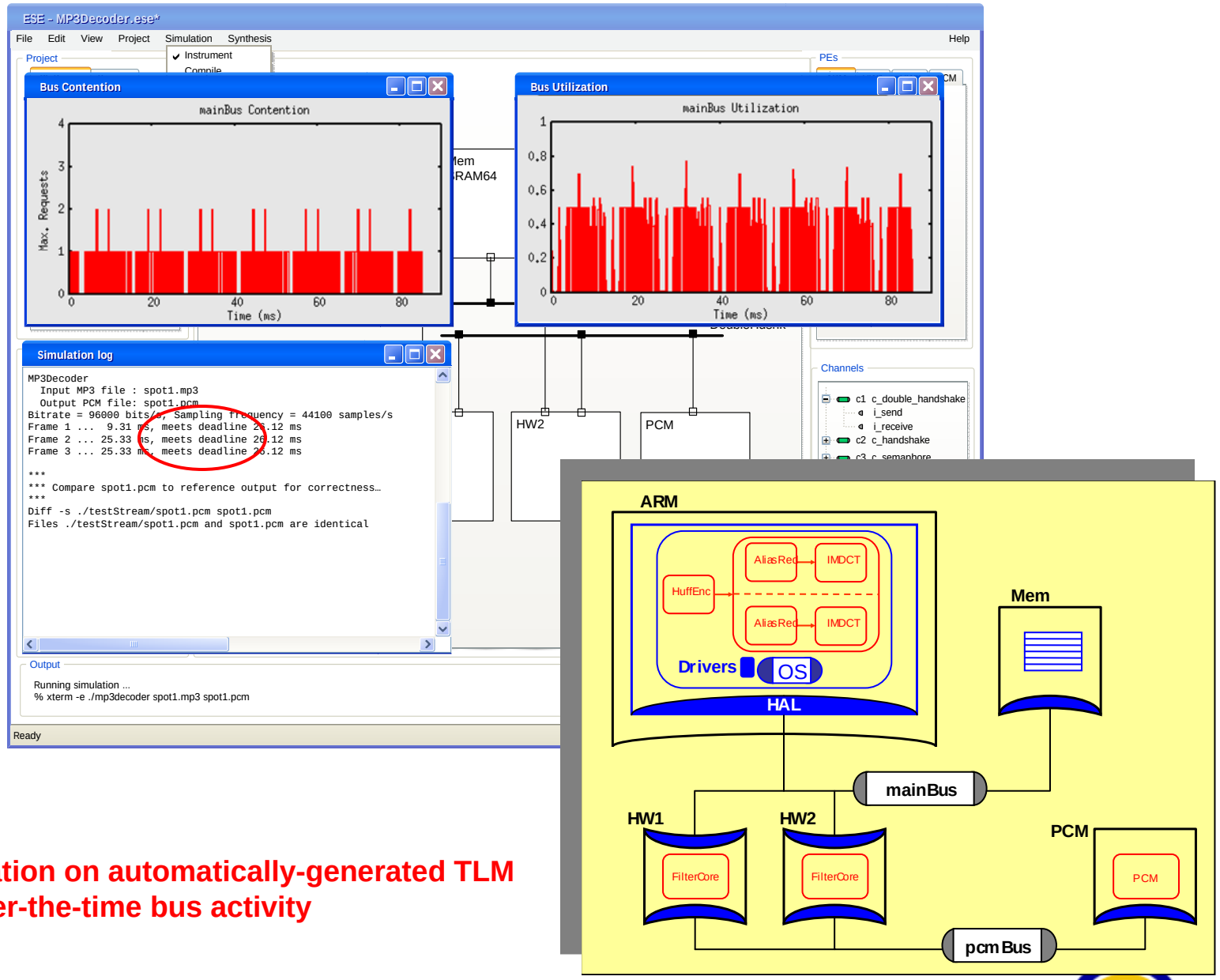
ESE: System Modification (3)





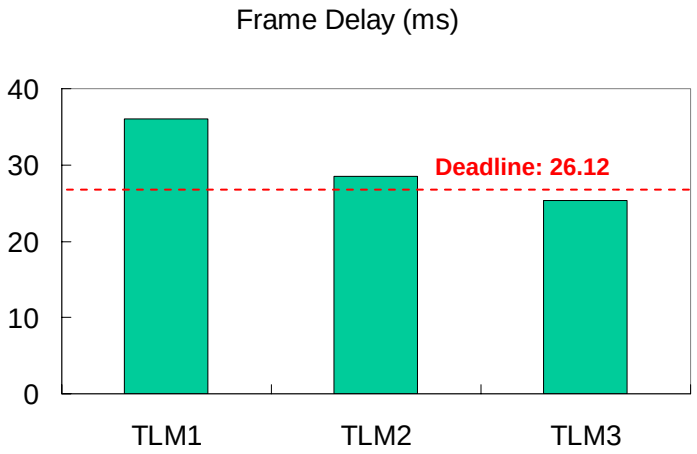
- **Remove components and connections**
- **Change connectivity**
- **Run transaction-level model generator**

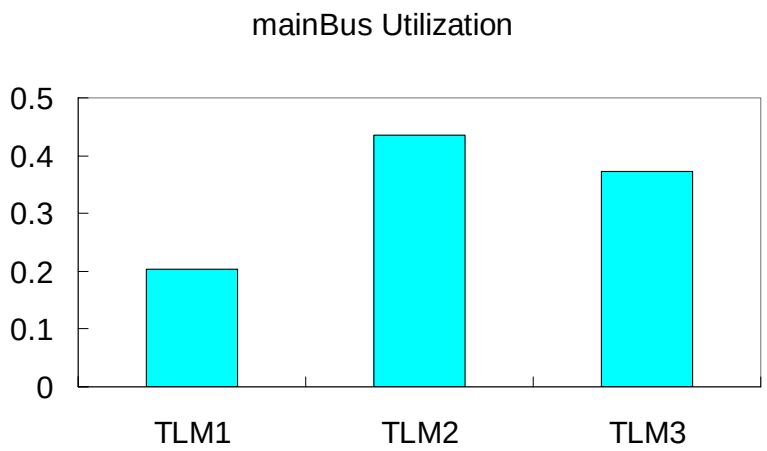
ESE: TLM Simulation

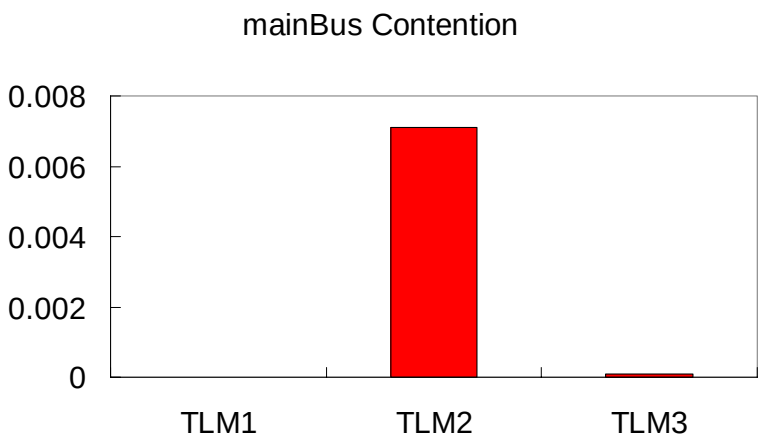


- **Run simulation on automatically-generated TLM**
- **Display over-the-time bus activity**

Design Summary







ESE Advantages

- Platform and application can be easily captured using GUI
- TL models are automatically generated
- ESE allows concurrent development of platform SW, HW and application code
- ESE allows easy upgrade of platform
- ESE simplifies reuse of legacy application SW and RTL HW code