# CECS eNEWS

Volume 9, Issue 2
Spring '09

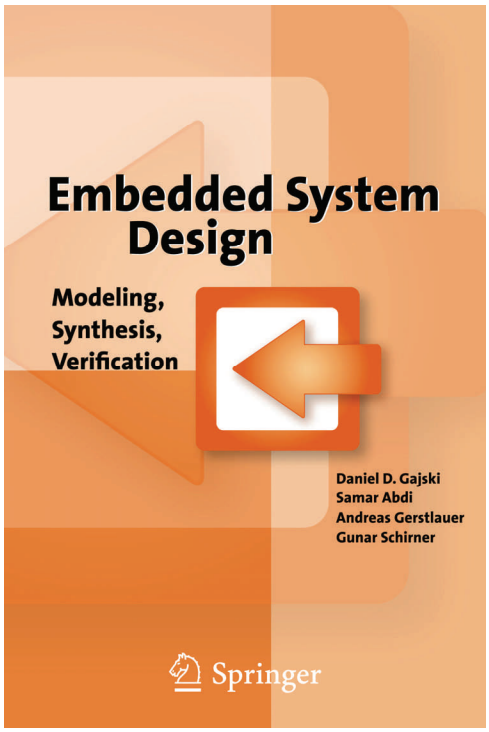
*Center for Embedded Computer Systems, University of California, Irvine*


## *Embedded System Design: Modeling, Synthesis and Verification* Released!

**- CECS Staff**

CECS members introduce a seminal new book on Embedded System Design. This book, *Embedded System Design: Modeling, Synthesis and Verification*, is scheduled to be published and released at the end of July 2009 by Springer.

The new book presents information on how to design a future multiprocessor system consisting of several processors and other components. Design methodology, modeling techniques, software and hardware synthesis methods and techniques for verification of such multi-processor systems are also discussed. The authors provide model based system synthesis techniques, including algorithms for platform design and application to platform design and application to platform mapping in addition to introducing methodology, design and tool concepts and delving into modeling practice and requirements all the way from application specification to system prototyping.




Daniel D. Gajski, University of California, Irvine, CA, USA; Samar Abdi, University of California, Irvine, CA, USA; Andreas Gerstlauer, University of Texas at Austin, TX, USA; Gunar Schirner, University of California, Irvine, CA, USA;

*Embedded System Design*, authored by Daniel Gajski, Samar Abdi, Andreas Gerstlauer, and Gunar Schirner, is written for embedded system designers, instructors, and graduate students.

CECS continues to be the leader in Embedded System innovations, following the tradition of such famous books as

- **Specification and Design of Embedded Systems**, by Daniel D. Gajski, Frank Vahid, Sanjiv Narayan, and Jie Gong
- **System Design - A Practical Guide with SpecC**, by Andreas Gerstlauer, Rainer Doemer, Junyu Peng, and Daniel D. Gajski
- **Embedded System Design: A Unified Hardware/Software Introduction**, by Frank Vahid and Tony D. Givargis
- **Memory Architecture Exploration for Programmable Embedded Systems**, by Peter Grun, Nikil D. Dutt, and Alexandru Nicolau

## CECS presents High-Level Synthesis and Design Tutorial @ DAC 09

**- CECS Staff**

CECS continues its presence in the hot topic area of High-Level Synthesis by presenting a tutorial on HLS at the 46th Design Automation Conference, to be held July 26-31, 2009, in San Francisco. This tutorial is part of a comprehensive introduction to using High-Level Synthesis with 3 speakers from academia and 3 speakers from industry.

**Continued on page 4**

**Highlights**


- **Embedded System Design: Modeling, Synthesis and Verification** Released
- CECS represents High-Level Synthesis and Design @ DAC 09
- Congratulations to the CECS Class of '09
- **Project Profile:** ConcurrenC
- **Visitor Profile:** Dr. Takashi Takenaka
- **Student Profile:** Rosario Cammarota
- **Student Profile:** Weiwei Chen

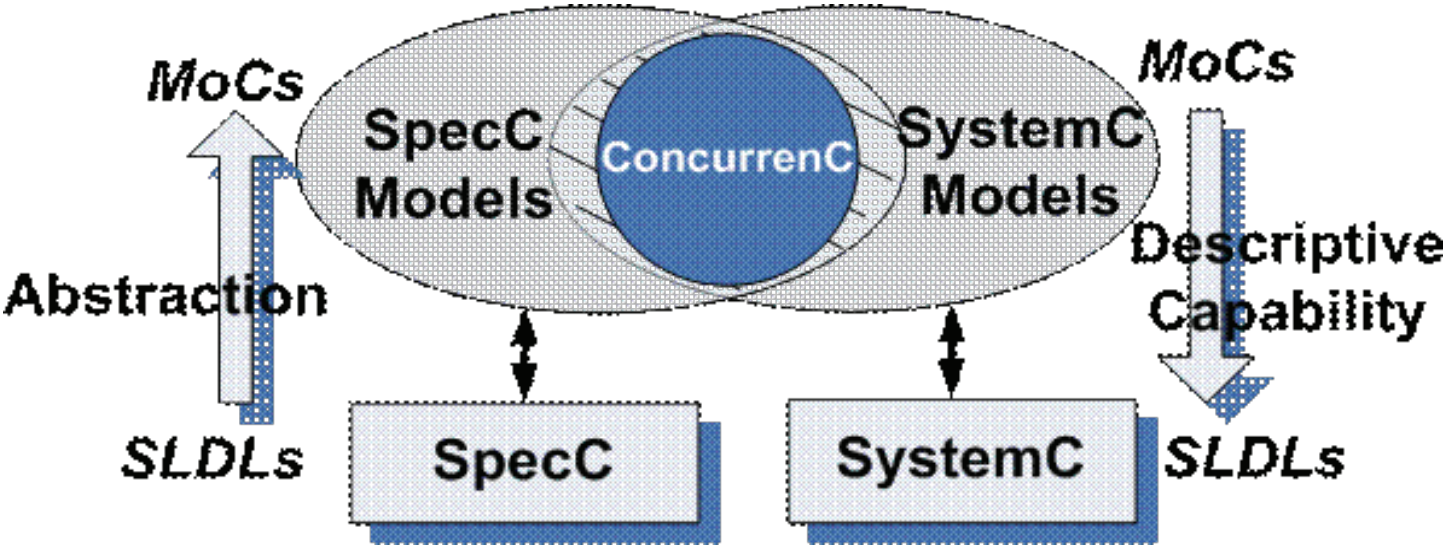

**Inside this Issue:**


| | |
|---|---|
| Project Profile | 2 |
| Visitor Profile | 3 |
| HDS Session | 4 |
| Congrats Grads | 5 |
| Publications | 6 |

# PROJECT & STUDENT PROFILES

## Project Profile: *ConcurrenC: A Novel Model of Computation for Effective System-level Abstraction of C-based SLDLs*

**- Weiwei Chen**



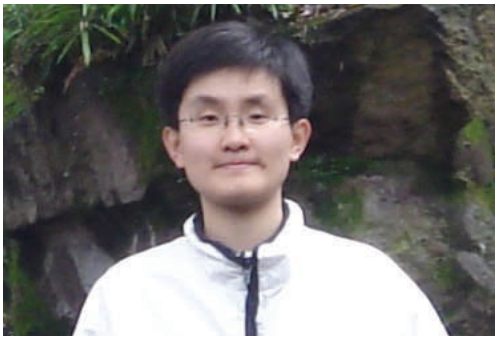

System design in general can only be successful if it is based on a suitable formal Model of Computation (MoC) that can be well represented in an executable System-level Description Language (SLDL), like SpecC and SystemC, and is supported by a matching set of design tools. While C-based SLDLs are popular in system-level modeling and validation, current tool flows impose almost arbitrary restrictions on the synthesizable subset of the supported SLDL. A properly aligned and consistent system-level MoC is often neglected or even ignored.

In this project, we motivate the need for a well-defined MoC in system design. We discuss the close relationship between SLDLs and the abstract models they can represent, in contrast to the smaller set of models the tools can support. Based on these findings, we then propose a novel MoC, called ConcurrenC, that defines a clear system level of abstraction, aptly fits system modeling requirements, and can be expressed precisely in both SystemC and SpecC SLDLs. Features like communication & computation separation, hierarchy, concurrency, abstract communications (channels), timing, and execution semantics are explicitly supported for the ConcurrenC MoC. We also discuss the relationship between the existing formal MoCs, like Kahn Process Network (KPN) and Synchronous Dataflow (SDF), and ConcurrenC which is essentially a superset of KPN and SDF. It is a versatile and convenient vehicle to express KPN and SDF models in C-based SLDLs.

Our research work will focus on defining the formal execution semantics of ConcurrenC, providing advanced scheduling and distributed simulation capabilities, as well as developing a suitable system design flow based on this MoC.

## Student Profile: Weiwei Chen

**- Weiwei Chen**



My name is Weiwei Chen. I am a Ph.D. candidate in the Department of Electrical Engineering and Computer Science at UCI. I received my master's degree in computer engineering from Shanghai Jiao Tong University in 2007, and my bachelor's degree in computer science and engineering from the same university in 2004. I was born in Shanghai, China, and lived there until coming to the U.S.

In September 2007, I joined CECS as a Ph.D. student and currently work with Professor Rainer Doemer in the Laboratory for Embedded Computer Systems (LECS). My research work focuses on methodologies of system level modeling of embedded computer systems.

# STUDENT PROFILES

## Student Profile: Rosario Cammarota

**- Rosario Cammarota**

I'm from Italy where I achieved my Master of Science degree in telecommunication engineering. After having worked in the Research Lab CNR and in industry, for some years, in the area of distributed systems, I decided to move to the US to advance my education and to continue my career in academia.

I started a Masters program and began working as a Research Specialist in the Center for Embedded Computer Systems, under the mentoring of Professor Veidenbaum. The main topic of my research is "Cache-Aware Synchronization and Scheduling of Data-Parallel Programs for Multi-Core Processors."

This year, I completed my Master of Science degree in Information and Computer Science with a concentration in Embedded Systems, from UC Irvine. The title of my thesis was: “A metrology based approach to performance analysis using hardware counters."

**Abstract:**
The dimensions that can be explored by doing performance analysis of computer systems are limited in number, however each dimension is composed by a large number of elements, such that the complexity of exploring all the possibilities grows exponentially. The basic elements that are usually investigated are micro architectural and/or compiler utilization and improvements, programming methodologies and practices.

Once the appropriate methodology to make performance analysis is selected, the accurate definition of the setup and the quantitative evaluation of the measurements still remain challenging.

This thesis defines, describes and implements a general methodology to obtain a fast, reproducible and accurate set of measurements of application behavior on a computer system. This is accomplished by accessing hardware performance counters through a sampling data collector. The methodology applies on modern microprocessors with out-of-order and speculative execution. It addresses the problem of how to deal with measurement errors in systems that can collect only a very small number of counters per run.

The methodology is based on a metrological approach to hardware counters harvesting, which is needed when an application is executed multiple times in order to make all the required measurements and for which the value of the counters changes for each execution of a given binary, although the execution produces correct output.

The methodology is used to evaluate performance of a System Under Test (SUT). Using SPEC CPU 2006 benchmarks, we give a basic analysis of the benchmark performance on Intel Core 2 Duo processor. The methodology is shown to produce accurate and reproducible measurements.

Finally, I have been admitted to the PhD program in Computer Science at UC Irvine, under the mentoring of Professor Veidenbaum, and my intention is to continue my academic career in the USA.

## Visitor Profile: Takashi Takenaka

**- CECS**

Dr. Takashi Takenaka is a visiting scholar at UC Irvine, hosted by Professor Nikil Dutt, from April 2009 through March 2010.

He received his Ph.D. degree in computer engineering from Osaka University, Japan in 2000. He joined NEC Corporation in 2000 and is currently in System IP Core Laboratories. His research interests include system level design, behavioral synthesis, formal verification and embedded systems. He has been engaged in the research and development of the C-based Synthesis and Verification suite “CyberWorkBench”.

Dr. Takenaka is very excited to visit Irvine. He says, “I am very pleased to have a great opportunity to collaborate with Professor Dutt and many outstanding researchers.” He adds, “Irvine is a very beautiful city. My family and I are enjoying the California atmosphere, the nearby coasts, and wide parks”.

# CECS HLS TUTORIAL

## CECS represents High-Level Synthesis and Design @ DAC 09 (cont'd from page 1)

Actual digital systems need new ESL tools in order to raise the specification abstraction level. High-Level Synthesis (HLS) starts from algorithmic specifications that focus on functionality rather than on the cycle accurate implementation that is used in Register Transfer Level (RTL) specifications. HLS tools thus allow designers to rapidly generate complex RTL hardware architectures that are optimized to various performance, area and power requirements. HLS offers the prospect of improving the productivity and quality of digital systems development. Designing at higher levels of abstraction allows one to better cope with the system design complexity, to verify earlier in the design process, and to increase code reuse.

This tutorial will provide a comprehensive introduction to the use of High-Level Synthesis. Basic definitions, key concepts, typical design flows, and design constraints will be described first. Next, case studies using High-Level Synthesis will be presented. The tutorial will examine the use and impact of High-Level Synthesis on the design process, from conception through implementation. It will provide guidance and insight on how this can be achieved in practice. The aim is for attendees to learn about High-Level Synthesis techniques they can use immediately and to give a view of the direction the industry is taking for the longer term.

Daniel Gajski directs the UCI Center for Embedded Computer Systems, with a research mission to incorporate embedded systems into automotive, communications, and medical applications. He has authored over 300 papers and numerous textbooks, including Principles of Digital Design, which has been translated into several languages. After ten years as a Professor at the University of Illinois he joined UCI, where he presently holds The Henry Samueli Endowed Chair in Computer System Design.

Jason Cong is currently a Chancellor's Professor at the Computer Science Department of University of California, Los Angeles, and a co-director of the VLSI CAD Laboratory. He also served as the department chair from 2005 to 2008. Dr. Cong's research interests include computer-aided design of VLSI circuits and systems, design and synthesis of system-on-a-chip, programmable systems, novel computer architectures, nano-systems, and highly scalable algorithms. He has published over 280 research papers and led over 30 research projects in these areas.

Nitin Chawla is a Senior Member of Technical Staff at STMicroelectronics and is currently responsible for design and methodology definition in the area of ESL Design. He is involved in the design of high performance and low power signal processing and communication systems. He graduated in electronics and telecommunication from Pune University, India. He has worked on various design domains related to audio and video processing, wireless communication and high speed serial links. He has several IEEE and IEC publications in the domain of signal processing and ESL design.

Sumio Morioka is a Senior Researcher at System IP Core Research Labs, NEC Corp. After receiving his Ph.D. degree in computer science from Osaka University in 1997, he joined NTT. He then moved to IBM Research Labs and subsequently to Sony and NEC Corp. During his entire career he has been working on the design of high performance IP cores and commercial SOCs in various application areas such as security, image/video processing and error correction. In 2004 he received the Sony MVP award for the development of a security hardware sub-system for PlayStation Portable and PLAYSTATION3.

Rodric Rabbah is an IBM researcher. He co-leads the Liquid Metal project, which aims to create a high-level language for programming software and hardware. Before joining IBM Corp., he was a member of CSAIL at MIT as a leading contributor to StreamIt, a new language and compiler for stream programming.

Scott Mahlke is an Associate Professor in the EECS Department at the University of Michigan where he directs the Compilers Creating Custom Processors research group. His group delivers technologies in application-specific processors, high-level synthesis, and compilers. Mahlke received the PhD in Electrical Engineering from the University of Illinois in 1997.

Earn Continuing Education Credit towards Professional Certification while attending the 46th DAC Tutorials! Click here to learn more.

**Speakers:**
Daniel Gajski - Univ. of California, Irvine, CA
Jason Cong - Univ. of California, Los Angeles, CA
Nitin Chawla - STMicroelectronics, Greater Noida, India
Sumio Morioka - NEC Corp., Kawasaki, Japan
Rodric Rabbah - IBM Corp., Hawthorne, NY
Scott Mahlke - Univ. of Michigan, Ann Arbor, MI

# CONGRATS GRADS



## Congrats '09 CECS Grads!

Several CECS PhD candidates presented their PhD Final Defenses this year. We would like to congratulate them, and wish them the best of luck in their Post Doctorate endeavors:

**Transducer Synthesis for Heterogeneous Multi-processor Systems**
by Hansu Cho, University of California, Irvine
July 9, 2009
view details

**Automatic Generation and Verification of Transaction Level Models**
by Lochi Yu, University of California, Irvine
June 18, 2009
view details

**TransMutations: A framework for dynamic customization of retargetable compilers for embedded processors**
by Ashok Halambi, University of California, Irvine
June 3, 2009
view details

**Temperature Aware VLSI Design for Reduced Power and Reliability Enhancement**
by Aseem Gupta, University of California, Irvine
May 29, 2009
view details

**Model-based Analysis of Event-driven Distributed Real-time Embedded Systems**
by Gabor Madl, University of California, Irvine
May 27, 2009
view details

**Automatic Design and Optimization of Application Specific Processors**
by Jelena Trajkovic, University of California, Irvine
February 27, 2009
view details



**Professor Nikil Dutt Hosts a Celebration Lunch**

# PUBLICATIONS

The following papers were published by CECS affiliates between April 2009 to June 2009.

| Focus | Title, Author, Publication |
|---|---|
| ***MPSoC Platforms*** | R. Leupers, A. Vajda, M. Bekooij, S. Ha, R. Doemer, and A. Nohl, "Programming MPSoC Platforms: Road Works Ahead!" Proceedings of Design Automation and Test in Europe, Nice, France, April 2009. |
| ***SEU-Aware Resource Binding*** | S. Golshan, and E. Bozorgzadeh, "SEU-Aware Resource Binding for Modular Redundancy Based Designs on FPGAs", to appear in ACM/IEEE International Conference on Design, Automation, and Test in Europe (DATE), April, 2009. |
| ***Scalable Channel Emulator for MIMO*** | Hamid Eslami, Sang V. Tran, and Ahmed M. Eltawil, "Design and Implementation of a Scalable Channel Emulator for Wideband MIMO Systems," Accepted to IEEE Transactions on Vehicular Technologies, April. 2009. |
| ***MicroBlaze-based Warp Processor*** | R. Lysecky and F. Vahid. "Design and Implementation of a MicroBlaze-based Warp Processor," ACM Transactions on Embedded Computing Systems (TECS), April, 2009. |
| ***Rich Sensor Networks*** | Arijit Ghosh and Tony Givargis, "Sytoplasm: A Middleware for Rich Sensor Networks," TR 09-01, April 14, 2009. |
| ***Fair Queueing*** | Arijit Ghosh and Tony Givargis, "Approximate Fair Queueing: A Low Complexity Packet Scheduler for Embedded Networks," TR 09-02, April 14, 2009. |
| ***Combined Routing + Queueing*** | Arijit Ghosh and Tony Givargis, "A Combined Routing+Queueing Approach to Improving Packet Latency of Video Sensor Networks," TR 09-03, April 14, 2009. |
| ***ESE Data Structure*** | Lochi Yu, Samar Abdi, and Daniel Gajski, "System Definition and ESE Data Structure," TR 09-04, March 25, 2009. Posted May 1, 2009. |
| ***SystemC TLM's*** | Lochi Yu, Samar Abdi, and Daniel Gajski, "Estimation of Communication in SystemC Transaction Level Models," TR 09-05, May 2009. |
| ***Garbage Collection for Parallel Systems*** | Shaoshan Liu, Ligang Wang, Xiao-Feng Li, and Jean-Luc Gaudiot, "Space-and-Time Efficient Garbage Collectors for Parallel Systems," Proceedings of the ACM International Conference on Computing Frontiers (CF 2009), Ischia, Italy, May 18-20, 2009. |
| ***Many-Core Systems*** | Shaoshan Liu (Ph.D. Student) and Jean-Luc Gaudiot (Advisor), "Value Prediction in Modern Many-Core Systems," Proceedings of the 23rd IEEE International Parallel & Distributed Processing Symposium (IPDPS 2009), TCPP-Ph.D. Forum, Rome, Italy, May 25-29, 2009. |
| ***Garbage Collection on Virtual Spaces*** | Shaoshan Liu, Ligang Wang, Xiao-Feng Li, and Jean-Luc Gaudiot, "Packer: an Innovative Space-Time-Efficient Parallel Garbage Collection Algorithm Based on Virtual Spaces," Proceedings of the 23rd IEEE International Parallel & Distributed Processing Symposium (IPDPS 2009), Rome, Italy, May 25-29, 2009. |
| ***ARM Instruction Set Simulators*** | K. P. Kim and R. Doemer, "Design Exploration using Multiple ARM Instruction Set Simulators - A Case Study on a JPEG Encoder," Center for Embedded Computer Systems, Technical Report 09-08, May 2009. |
| ***ConcurrenC C-based SLDL*** | W. Chen and R. Doemer, "ConcurrenC: A Novel Model of Computation for Effective Abstraction of C-based SLDLs," Center for Embedded Computer Systems, Technical Report 09-07, May 2009. |
| ***Recording Integrated Development Environment*** | B. Zhang and R. Doemer, "An Eclipse-based Software Platform for the Recoding Integrated Development Environment (RIDE)," Center for Embedded Computer Systems, Technical Report 09-06, May 2009. |
| ***Loop-Level Parallelism*** | Arun Kejariwal, Alexander V. Veidenbaum, Alexandru Nicolau, Milind Girkar, Xinmin Tian, and Hideki Saito, "On the exploitation of loop-level parallelism in embedded applications," ACM Trans. Embedded Computer Syst. 8(2) 2009. |

**Continued on page 7**

CECS—*promoting creativity and pursuing discovery!*

*Center for Embedded Computer Systems, University of California, Irvine*

***CECS** Mission Statement:*

*To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.*

**CECS eNews**
Center for Embedded Computer Systems
2010 Anteater Instruction & Research Building
University of California, Irvine
Email: enews@cecs.uci.edu

**CECS Research Advisory Board**
Dr. Gilbert F. Amelio, Senior Partner, Sienna Ventures, Sausalito, CA
Dr. Mutsuhiro Arinobu, Vice President, Toshiba Corporation, Tokyo, Japan
Dr. Jai K. Hakhu, Vice President Intel Corp., Santa Clara, CA

## The following papers were published by CECS affiliates between April 2009 to June 2009. (cont'd from page 6)

| | |
|---|---|
| ***Practical Design Verification*** | Dhiraj Pradhan and Ian G. Harris Eds., **Practical Design Verification**, Cambridge University Publishers, May 2009. |
| ***Code-Modulated Path-Sharing*** | Amin Jahanian, Fred Tzeng, Payam Heydari, "Code-Modulated Path-Sharing Multi-Antenna Receivers: Theory and Analysis," IEEE Trans. on Wireless Communications, May 2009. |
| ***Code-Modulated Path-Sharing*** | Fred Tzeng, Amin Jahanian, Deyi Pi, Payam Heydari, "A CMOS Code-Modulated Path-Sharing Multi-Antenna Receiver Front-End," IEEE J. Solid-State Circuits, May 2009. |
| ***Multi-core Processors*** | Chen Liu and Jean-Luc Gaudiot, "The Impact of Resource Sharing Control on the Design of Multicore Processors," The 9th International Conference on Algorithms and Architectures for Parallel Processing (ICA3PP'09), Taipei, Taiwan, June 8-11, 2009. |
| ***CUDA Graphics Processors*** | J. Moorkanikara Nageswaran, N. Dutt, J.L. Krichmar, A. Nicolau, and A. Veidenbaum, "Efficient Simulation of Large-Scale Spiking Neural Networks Using CUDA Graphics Processors," Paper presented at: IJCNN, Atlanta, GA, June 2009. |
| ***K-Best Sphere Decoder*** | Sudip Mondal, Ahmed M. Eltawil, Chung-An Shen, Khaled Salama, "Design and Implementation of a Sort Free K-Best Sphere Decoder," Accepted to IEEE Transactions on Very Large Scale Integration Systems, June 2009. |
| ***LazySync for Distributed Simulation of Sensor Networks*** | Z. Jin and R. Gupta, "LazySync: A New Synchronization Scheme for Distributed Simulation of Sensor Networks", In 5th IEEE International Conference on Distributed Computing in Sensor Systems (DCOSS), June 2009. |