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CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

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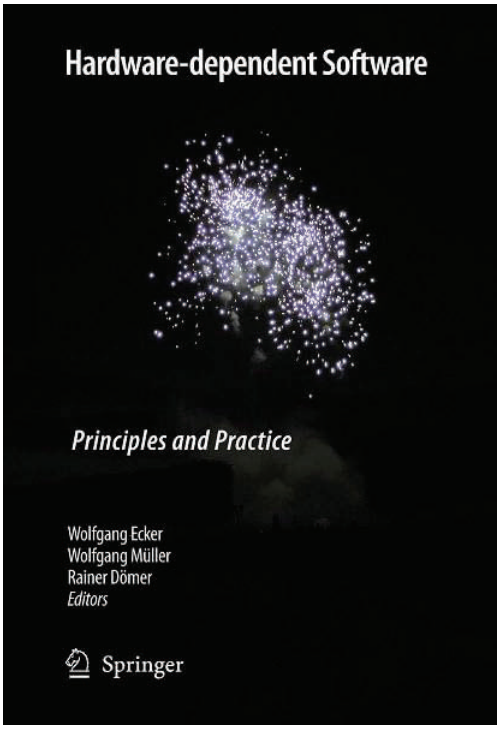
Hardware-dependent Software: Principles and Practice Released!

- CECS Staff

Hardware-dependent Software (HdS) plays a key role in desktop computers and servers for many years. Mainly due to its flexibility, the possibility of late change, and the quick adaptability, the relevance of HdS in the domains of embedded systems and in Systems-on-Chip (SoCs) has significantly increased.

HdS has become a crucial factor in embedded system design since it allows accommodating and adapting late changes in the hardware platform as well as in the application software. Thus, even last minute changes can be quickly performed. On the other hand, changes in the HdS are often hard to track and can have a complex impact on the system with a potential for total system failure. HdS also critically influences the system performance and power management. Consequently, HdS must be carefully designed and maintained.

Despite its importance, the role of HdS is most often underestimated and the topic is not well represented in literature and education. Considering today's literature, we can only find very few introductory and application-oriented text books. To overcome this gap, we have brought together



W. Ecker, Infineon Technologies AG, München, Germany; W. Müller, Paderborn University C-LAB, Germany; R. Dömer, University of California, Irvine, USA (Eds.)

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edaForum08: Dr. Daniel Gajski featured as Keynote Speaker

- CECS Staff

edaForum08 invited experts from the USA, Asia, and Europe to share the newest design methods for designing increasingly complex products in a short time with high efficiency and the highest quality. The edaForum08 also discusses today's burning economical questions of microelectronics in addition to its technical talks.

edaForum08 was held on December 11-12, 2008 in Dresden, Germany. This year's topics included the following:

- "How to use EDA to solve the challenges in microelectronics"
- "How to save energy and reduce CO2 emission by clever chips"
- "How to design robust chips for no failures during lifetime"
- "How to exploit future technologies to commercial success" and
- "How to get the right people to solve the above problems!"

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Project Profile: Cross-Layer Fault-Tolerant Adaptation Targeting Wireless Multimedia Systems

- Amin Khajeh

After I got my B.S. degree, I worked for Siemens Corp. After one year of working in the R&D section, I realized that I just know a little in the world of engineering. Then, I decided to continue my education. In the course of my Ph.D. studies, I realized that not only I learned how to solve my research problems, but also I have learned a systematic method of doing research in any field. I do believe that all the modeling and simulations have the same nature. At this point, I feel that it is not important what is the topic of the research, but how it can help people in our society, how it can promise a better life for our future. My goal has been and is to be an effective person, researcher, scientist, and an engineer.

I started my Ph.D. in winter of 2005 under the supervision of Prof. Eltawil and Prof. Kurdahi. I am working on fault tolerant adaptation for wireless multimedia systems. The embedded systems that support mobile applications are resource and power hungry. However in reality, the mobile resources are limited for ultra efficient compact systems. To support these apparent conflicting requirements under a wide range of operation condition, embedded systems for mobile applications have to be adaptive. Furthermore, the current adaptation techniques are not designed to be fault tolerant, while it is true that there exists a broad family of applications that are inherently fault tolerant such as wireless and multimedia applications. The idea here is to add an extra degree of freedom to the design space (which traditionally is based on error and performance) by extending it in the hardware error dimension.

The limitations of resources in mobile multimedia systems require good strategies for energy/QoS provisioning. This necessitates resource management policies at different layers including: a) a specific video encoding/decoding algorithm at the application layer; b) data transfer protocol and network monitoring at the middleware layer; c) Fault Tolerant techniques (FT) at the physical layer. Traditionally, each layer is self-contained and optimized independently from the other layers. By the very nature of independence, it is assumed that each layer operates correctly, and does not contribute errors that propagate through the system. This assumption inevitably limits the design space. For example, consider the case of voltage scaling at the physical layer, which is performed with the underlying assumption that the hardware has to maintain 100% correctness, 100% of the time. While this may be true for some classes of applications such as processor code, it is clearly not true when dealing with applications such as multimedia, which is inherently error resilient. In fact, multimedia applications are particularly interesting, since the error resilience is distributed across multiple layers, namely; error resilience at the application layer, error tolerance at the network level, and error tolerance a the communication layer. Clearly, by exchanging error tolerance statistics and behaviors between layers, optimum operating points can be achieved which were previously unattainable.

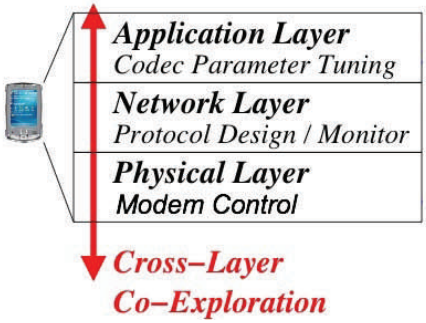

Figure 1. Cross-Layer Co-Exploration

One case that we have explored is where aggressive voltage scaling is allowed to occur at the physical level resulting in higher power savings, albeit associated with intermittent faulty operation of the underlying hardware. This scenario provides the best opportunity for innovation by relaxing the specifications of portions of the hardware and allowing the system to handle these errors at the system level. The ability of the system to handle errors is highly dependent on the statistics of the errors, and also on the algorithm running on the hardware, which implies that this has to be a dynamic process, *optimized at design time and managed during run-time*. To be

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Project Profile: Cross-Layer Fault-Tolerant Adaptation Targeting wireless Multimedia Systems (continued from pg 2)

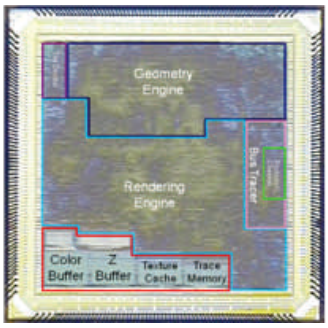
able to extract the most benefit out of this error aware approach, it is important to examine the relationship between (a) the constituent components of an architecture and their vulnerability in terms of power consumption and reliability as a function of the operating conditions, and (b) the needs, assumptions and requirements of the application layers depending on this architecture.

The key idea underlying the co-exploration is that we manipulate the parameters of the reconfigurable video coding to provide awareness of architectural characteristics at the physical layer. Typically, the main challenge in such an approach is to accurately and rapidly abstract the statistics of the physical layer (circuits) in a useful manner such that higher layers can easily utilize this information. Clearly, the expanded design space will require a multitude of design points to be evaluated. Running simulations on the physical layer at each design point parameters leads to a cumbersome approach, with limited applicability. It is therefore imperative to devise accurate analytical models that abstract the underlying fault mechanisms of the physical layer. For that reason, we have also developed a comprehensive analytical model that abstracts physical error statistics in embedded memories.

Visitor Profile: Ing-Jer Huang

Professor Ing-Jer Huang is a visiting scholar at UCI, hosted by Professor Nikil Dutt, from August 2008 through July 2009. He received his PhD degree in computer en¬gineering from the University of Southern California in 1994. He is currently a professor in the Department of Computer Science and En¬gineering at National Sun Yat-Sen University in Taiwan.

His research interests include computer architecture, SoC design, design automation, system software, embedded systems, and hardware/software co-design/verification. He has established a long term solid relationship with IC related industries. Many of his techniques have been licensed to or as the result of collaboration with companies, such as ACard, ADMtek, ATChip, Faraday, GlobalUniChip, Himax, Holtek, Microtime, RDC, STC/ITRI, S&Q, Temento, Via, etc.



During recent years, he has been working on the development of SoC infrastructure and related IP's to support real time on-chip tracing, debugging, verification and monitoring for advanced on-chip connection. In addition, he is currently leading a large scale joint project consisting of eight professors in the development of the hardware/software of a 3D graphics SoC for consumer electronics, in which multidisciplinary research issues are explored, including computer graphics algorithms, application interface, middleware, compiler, device drivers, operating system, development environment, low power design, system modeling/ exploration, hardware architecture, SoC integration/ monitoring/debugging/ testing, FPGA/chip implementation and verification, etc.

He has won many awards, including Excellent Professor in Engineering, Chinese Institute of Engineers, 2007, Invention Awards, National Sun Yat-Sen University, 2005, 2007, and Excellent Advisor, National Sun Yat-Sen University, 1999.

To further enhance the collaboration with UCI research community, three of his PhD students are also visiting UCI for the same period: Fu-Ching (Alan) Yang, with interests in SoC infrastructure, microprocessor verification and photography, Liang-Bi Chen, with interests in low power design and Chinese music playing and conducting, and Chun-Hung (James) Lai with interests in memory system organization and optimization. Their visits are supported by National Science Council (Taiwan) and National Sun Yat-Sen University.

STUDENT PROFILE

Student Profile: Vahid Salmani

Vahid Salmani is a first year student of the Department of Electrical Engineering and Computer Science at UCI. He received his Master's and Bachelor's degrees in Computer Engineering under the supervision of Prof. Mahmoud Naghibzadeh in 2007 and 2004 from Ferdowsi University of Mashhad, Iran. His previous research was mainly focused on real-time scheduling on multiprocessors and intelligent decision making in multi-agent environments.

In April 2008, Vahid joined CECS program and currently works with Prof. Pai H. Chou in the Embedded Systems & Design Integration Laboratory. He has been working on the ECO project, an ultra-compact wireless sensing system. "We are trying to achieve the maximum practical throughput using communication scheduling" says Vahid. He adds "I have been working on optimization of the MAC protocol to hide the idle times and maximize the system performance".

Vahid is excited to come to Irvine. "It is a very safe and beautiful city and the weather is so nice here" he says. He has also met many knowledgeable professors and made some good friends. Vahid adds "I am very pleased to work with Professor Chou and it is a great opportunity to collaborate with many outstanding researchers here at UC Irvine."

Hardware-dependent Software: Principles and Practice Released (cont'd from page 1)

experts from different HdS areas in this book. By providing a comprehensive overview of general HdS principles, tools, and applications, we feel that this book provides adequate insight into the current technology and upcoming developments in the domain of HdS.

The reader will find an interesting text book with self-contained introductions to the principles of Real-Time Operating Systems (RTOS), the emerging BIOS successor UEFI, and the Hardware Abstraction Layer (HAL). Other chapters cover industrial applications, verification, and tool environments. Tool introductions cover the application of tools in the ASIP software tool chain and the generation of drivers and OS components from C-based languages. Applications focus on telecommunication and automotive systems. For automotive systems, two approaches for SystemC-based verification are presented.
more on *http://springer.com/978-1-4020-9435-4*

▶To our knowledge, this is the first complete book on hardware-dependent software, a critical topic in embedded system design

▶Comprehensive introductions

▶HdS coverage with many applications

▶Examples from industrial automotive and communication designs

ASP-DAC 2009 Features Special HDS Session

- Ikutaro Kojima
(Nikkei Electronics Asia - March 2009)
article from:
http://techon.nikkeibp.co.jp/article/HONSHI/20090225/166328/

The 14th Asia and South Pacific Design Automation Conference (ASP-DAC 2009) was held from January 19 to 22 at Pacifico Yokohama, Japan. This time there were multiple special sessions, one of which was on the theme of hardware-dependent software (HDS) in the multi-core/many-core era. Entitled "Special Session: Hardware Dependent Software for Multi- and Many-Core Embedded Systems," the session featured four speakers.

HDS Defined

The first speaker was Assistant Professor Dr Rainer Doemer of the University of California (UC) at Irvine, who was also one of the organizers of the session. In his talk, "Introduction to Hardware-dependent Software Design," presented jointly by UC Irvine, University of Texas, Austin, and University of Paderborn, Germany, Doemer provided a definition of HDS and touched on various related issues.

According to Doemer, HDS refers to software that is exceedingly close to hardware, such as the operating system (OS) and real-time OS (RTOS), device drivers, boot firmware and communication protocol stacks. The role of HDS is becoming increasingly important in the effective utiliza-

ASP-DAC 2009 Features Special HDS Session (con't from page 4)

tion of a rich array of hardware resources for diverse tasks. In particular, it has become commonplace for integrated circuits (IC) to integrate multiple processor cores (multi-core, many-core, etc), further raising expectations of HDS. At the same time, though, HDS development has become quite complex.

TLM Takes Too Long

The second person at the podium was Michael Velten of Infineon Technologies AG of Germany. His talk, titled "Using a Dataflow Abstracted Virtual Prototype for HDS-Design," dealt with hardware models (virtual prototypes) applicable in HDS development.

In the electronic design automation (EDA) industry, virtual prototyping using transaction-level modeling (TLM) is attracting considerable attention, but Velten argued that TLM processing takes too long when it comes to tasks such as HDS development or verification. He proposed a new, higher level of abstraction, which he calls TLM+, and which makes it possible to reduce processing time to one-tenth, or better.

The third speaker, Yasutaka Tsunakawa of Sony Corp of Japan, discussed "Needs and Trends in Embedded Software Development for Consumer Electronics." He talked about the present state of multi- and many-core designs, and related issues, from the viewpoint of asynchronous multi-processor (AMP) and synchronous multi-processor (SMP) technology.

He said that practical application of HDS is progressing in AMP and mixed AMP/SMP (what he calls "simple SMP") multi-core implementations, as evidenced by, for example, a commercial OS. In many-core, however, with about 100 cores, no clear direction is evident in HDS.

Multi-core does not suddenly jump to many-core, but instead passes through a stage called "complex SMP." In complex SMP multiple SMPs are linked to operate like an AMP. A paradigm shift from simple SMP to complex SMP is necessary, and he believes that is the path to many-core.

The final speaker was Dr Samar Abdi, again of UC Irvine, who announced an automatic HDS generating system under the title "Hardware-Dependent Software Synthesis for Many-Core Embedded Systems." Until now, HDS has been developed manually, using tools such as prototyping boards and virtual platforms as bases, but he described how programs and hardware design information would be used to automatically generate HDS in the future, introducing the Embedded System Environment (ESE) now under development at UC Irvine.

ASP-DAC 2009, Pacifico Yokohama

edaForum08 (cont'd from page 1)

Dr. Daniel Gajski was the December 12th Keynote speaker. His talk, "New Strategies for System Design," was as follows (from abstract):

With complexities of Systems-on-Chip (SOCs) rising almost daily, the design community has been searching for a new methodology that can handle given complexities with increased productivity and decreased time-to-market. The obvious solution that comes to mind is increasing levels of abstraction, or in other words, increasing the size of the basic building blocks. However, it is not clear what these basic blocks should be and what should be the strategy for creating a SOC out of these basic blocks. To make things more difficult, the difference between software and hardware is becoming indistinguishable, which in turn, requires sizable change in the industrial and academic infrastructure.

In order to find the solution, we will look first at the system gap between SW and HW designs and derive requirements for the system design flow that includes software, as well as hardware. In order to enable new tools for model generation, simulation, synthesis and verification, the design flow has to be well defined with unique abstraction levels, model semantics and model transformations that correspond to design decision made by designers…

The complete abstract, as well as more information on the forum, can be found on edaForum's web site at: http://www.edacentrum.de/edaforum/

PUBLICATIONS

The following papers were published by CECS affiliates between January 2009 to March 2009.

Focus	Title, Author, Publication
Hardware-dependent Software	W. Ecker, W. Müller, R. Dömer, "Hardware-dependent Software - Principles and Practice," Springer, Boston, January 2009. (ISBN 978-1-4020-9435-4)
Hardware-dependent Software	W. Ecker, W. Müller, R. Dömer, "Hardware-dependent Software - Introduction and Overview," Chapter 1 in **Hardware-dependent Software: Principles and Practice** (ed. W. Ecker, W. Müller, R. Dömer), Springer, Boston, January 2009. (ISBN 978-1-4020-9435-4)
Hardware-dependent Software	G. Schirner, R. Dömer, A. Gerstlauer, "High-Level Development, Modeling and Automatic Generation of Hardware-dependent Software," Chapter 8 in **Hardware-dependent Software: Principles and Practice** (ed. W. Ecker, W. Müller, R. Dömer), Springer, Boston, January 2009. (ISBN 978-1-4020-9435-4)
Hardware-dependent Software	R. Dömer, A. Gerstlauer, W. Müller, "Introduction to Hardware-dependent Software Design," Proceedings of the Asia and South Pacific Design Automation Conference 2009, Yokohama, Japan, January 2009.
Many-Core Embedded Systems	Samar Abdi, Gunar Schirner, Ines Viskic, Hansu Cho, Yonghyun Hwang, Lochi Yu, and Daniel Gajski, "Hardware-dependent Software Synthesis for Many-Core Embedded Systems," Proceedings of the Asia and South Pacific Design Automation Conference 2009, Yokohama, Japan, January 2009.
Frequency Divider	Chun-Cheng Wang, Zhiming Chen, Vipul Jain, and Payam Heydari, "Design and Analysis of a Silicon-Based Millimeter-Wave Divide-by-3 Injection-Locked Frequency Divider," IEEE Silicon Monolithic Integrated Circuits in RF Systems, Jan. 2009.
Virtual Microcontrollers	S. Sirowy, D. Sheldon, T. Givargis, F. Vahid, "Virtual Microcontrollers," ACM SIGBED Review, vol. 6, no. 1, January 2009. (PDF)
Loop-level Parallelism	Arun Kejariwal, Alexander V. Veidenbaum, Alexandru Nicolau, Milind Girkar, Xinmin Tian, and Hideki Saito, "On the exploitation of loop-level parallelism in embedded applications," ACM Trans. Embedded Computer Syst. 8(2) 2009
Many-Core Architectures	Shaoshan Liu, Jean-Luc Gaudiot, "Potential Impact of Value Prediction on Communication in Many-Core Architectures," IEEE Transactions on Computers, 03 Feb. 2009. IEEE computer Society Digital Library.
BiCMOS Transceiver	Vipul Jain, Fred Tzeng, Lei Zhou, and Payam Heydari, "A Single-Chip Dual-Band 22-to-29GHz/77-to-81GHz BiCMOS Transceiver for Automotive Radars," IEEE Int'l Solid-State Circuits Conference (ISSCC), Feb. 2009.
Power-Aware Network-on-Chip	Seung Eun LEE and Nader Bagherzadeh, "A Variable Frequency Link for a Power-Aware Network-on-Chip (NoC)," Integration, the VLSI Journal, Elsevier. 2009 (PDF)
Network-on-Chip Router	Seung Eun LEE and Nader Bagherzadeh, "A High-level Power Model for Network-on-Chip (NoC) Router," Computer & Electrical Engineering, Elsevier. 2009 (PDF)
Multi-Antenna Receivers	Amin Jahanian, Fred Tzeng, Payam Heydari, "Code-Modulated Path-Sharing Multi-Antenna Receivers: Theory and Analysis," IEEE Trans. on Wireless Communications, 2009.
Processor Speed Control	"Processor Speed Control with Thermal Constraints," Almir Mutapcic, Stephen Boyd, Srinivasan Murali, David Atienza, Giovanni De Micheli, Rajesh Gupta, IEEE Transactions on Circuits and Systems, Part I, 2009.

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