Volume 8, Issue 4
Fall '08

CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights

- Embedded System Environment (ESE) 2.0 Released
- Fadi Kurdahi receives Distinguished Alumni Award from AUB
- CECS hosts Annual CECS Potluck '08
- Mohammad Ali Ghodrat, Tony Givargis, and Alex Nicolau win Best Paper Award at CASES 2008
- Special Session at ASPDAC 2009
- Student Profile: Sehwan Kim

Inside this Issue:

CECS Potluck	2
Best Paper Award	3
Student Profile	4
ASPDAC 2009	5
Recent Publications	7

Embedded System Environment (ESE) 2.0 Released

- ESE Design Team

We are happy to announce that the Embedded System Environment (ESE) in version 2.0 has been released for public use on 11/07/2008. ESE is a toolset for efficient modeling, synthesis and validation of multi-processor embedded system designs. It implements a design methodology that raises abstraction level by separating functional and platform concerns. With the raised abstraction level, it allows the developer to focus on the essential algorithmic functionality without the burden of low-level implementation detail.

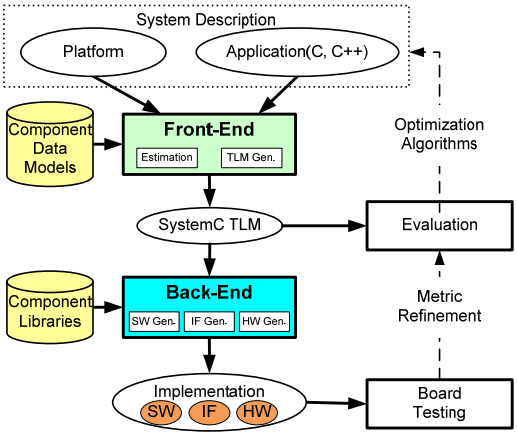


Figure 1: ESE design flow.

Figure 1 shows the ESE design flow, which consists of a front-end and a back-end. The front-end provides a graphical user interface for capturing the platform definition and application code. The application is expressed as parallel communicating processes, independent of their later implementation in hardware or software. The TLM generator in front-end then generates a TLM implementing a given application mapping onto the selected multi-core platform. For detailed timing information ESE uses a component database containing SW processor cores, HW cores, RTOSes, buses, links and routers. The generated system TLM serves as a

Continued on page 4

Fadi Kurdahi receives Distinguished Alumni Award from American University of Beirut.

- orig. article: http://www.aub.edu.lb/news/archive/preview.php?id=88980

Congratulations to Professor Fadi Kurdahi for his award from his alma mater, American University of Beirut. Professor Kurdahi was recognized for his contributions to design automation of digital systems.

Fadi Kurdahi receives his award from Dean Hajj. Picture from http://www.aub.edu.lb/

The Faculty of Engineering and Architecture at the American University of Beirut recognized six of its alumni with awards during the Seventh FEA Student Conference, which was held on October 16 and 17, 2008.

The conference is an annual event during which engineering, architecture and graphic design students present their final-year projects, many of which showcase innovative ideas. Additionally, the faculty also recognizes distinguished alumni who have achieved success in their careers.

CECS POTLUCK

CECS Hosts Annual Potluck '08

- CECS Events Staff

The Center for Embedded Computer Systems welcomed back both faculty and staff on Friday, November 21, 2008 with the Annual CECS Potluck. This year, we had everything from turkey, ribs, and gigantic shrimp to ginseng chicken, friend rice, and vegetarian turkey.

The turnout totaled roughly 30 to 40 attendees over the lunch period in the BBQ and Volleyball area at the University Hills Lower Pool area.

In addition to eating great food and finally having some time to catch up with colleagues, we were treated with some live entertainment from one of our attendees playing a duxianqin (literal translation: single string zither).

We would like to thank all the faculty, students, and other guests who attended to make a great potluck party!









Continued on page 3

Mohammad Ali Ghodrat, Tony Givargis, and Alex Nicolau win Best Paper Award for CASES 2008

Mohammad Ali Ghodrat, Tony Givargis, and Alex Nicolau recently received the Best Paper Award for CASES 2008 for their “Control Flow Optimization in Loops Using Interval Analysis.” Congratulations!

Abstract of Paper:

The work presents a novel loop transformation technique, particularly well suited for optimizing embedded compilers, where an increase in compilation time is acceptable in exchange for significant performance increase. The transformation technique optimizes loops containing nested conditional blocks. Specifically, the transformation takes advantage of the fact that the Boolean value of the conditional expression, determining the true/false paths, can be statically analyzed using a novel interval analysis technique that can evaluate conditional expressions in the general polynomial form. Results from interval analysis combined

Continued on page 5

CECS Annual Potluck ‘08

(cont’d from pg. 2)










Continued on page 6

STUDENT PROFILE

Student Profile: Sehwan Kim

It has been said that "everyone who is prosperous or successful must have dreamed of something. It is not because he is a good worker that he is prosperous, but because he dreamed." When I decided to go abroad to study further, it was a dream. Now, I am living the dream. Actually, it is no longer a dream, it is real. I joined CECS, at UC Irvine, in September 2008 and have been studying under Professor Pai H. Chou.

My specific research interest is in embedded systems and also covers various areas of advanced communication systems, which are extensions of my academic and professional work so far. I would like to design and analyze communication algorithms for wireless ad hoc and RF sensor networks. In particular, I am fascinated by the fields of robust resource allocation, low power system design and energy harvesting systems. Such systems can have a broad range of applications including real-time structure health monitoring and biomedical engineering and telematics.

I dreamed for nine years until I made my dreams to come true. These include my masters degree and extensive work experience. I received my masters from Hanyang University in Korea, majoring in optical communication systems. In addition, I built up my work experience not only in the optical field of Ethernet switching systems but also in the CDMA field of wireless technology at Samsung Electronics. I believe this new opportunity to collaborate with the most talented engineers to explore the possibilities and challenges of new technology, at CECS at UC Irvine, will surely become the greatest chapter of my life.

Embedded System Environment (ESE) 2.0 Released (cont'd from page 1)

convenient platform for design space exploration, analysis and development.

The back-end automatically generates an implementation model consisting of software, interfaces and hardware. For SW, the tool generates drivers and the RTOS configuration necessary to run communication and application SW on the platform. The HW synthesis generates RTL description of the HW cores. The interface synthesis generates and/or configures interfaces, interrupt controllers, bridges and routers to facilitate communication. The generated implementation model, containing all software, interfaces and hardware, can be exported traditional design tools for low level synthesis.

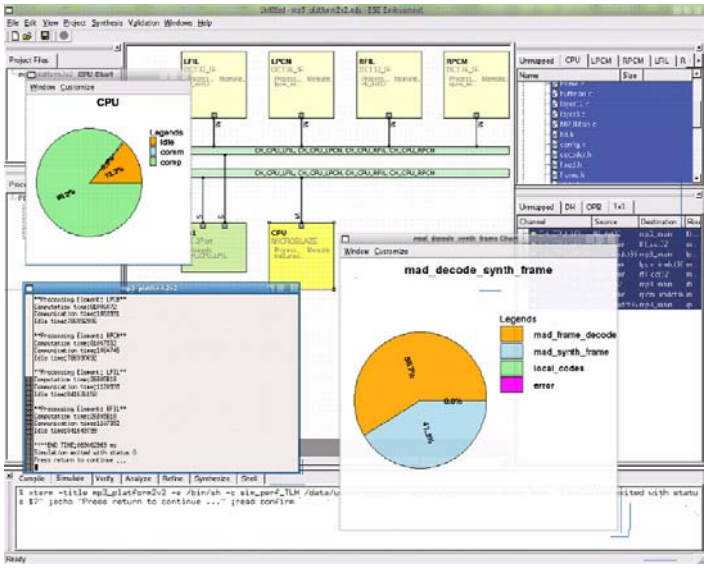


Figure 2: ESE Graphical User Interface.

ESE guides developers through the complex process of designing a Multi-Processor System-on-Chip (MPSoC) using an intuitive GUI as shown in Figure 2. It facilitates graphically capturing the platform definition (as shown in the main canvas) and guides the user through mapping the application to the platform. The ESE TLM generator implements these decisions when generating the system TLM. It serves as a comprehensive platform for system analysis and development. The user receives immediate feedback about the quality of the design decisions through various metrics, such as processor and bus utilization, distribution of computation load and memory consumption. These metrics enable an informed decision making for improving platform and/or mapping decisions.

By automating the implementation of system-level design decisions and by graphically guiding the user through the design process, ESE dramatically reduces the development effort in prototyping complex MPSoCs. As a result application designers, platform architects and system designers can significantly benefit from the efficient design flow made possible by ESE.

Please visit our web site at: http://www.cecs.uci.edu/~ese to download ESE 2.0 and try it with your own application and platform. At the same site we also have a video tutorial available demonstrating step-by-step a many-core MP3 player design.

Special Session at ASPDAC 2009: Hardware-dependent Software for Multi- and Many-Core Embedded Systems

Abstract:

With the relentless increase in embedded system complexity and the shrinking time to market, great challenges have emerged in the development of embedded software. The focus of this special session is Hardware-dependent Software (HdS), which interacts directly with the underlying hardware platform. Special consideration is paid to the increasing complexity of HdS due to the transition from multi-core systems to many-core platforms.

This session discusses the challenges involved in HdS design, covers different perspectives from both industry and academia, and outlines potential solutions to overcome the embedded software challenges in system design. Various multimedia applications are used as design drivers.
After a brief introduction and overview about HdS by the session organizers, the first talk outlines the challenges for HdS development from a semiconductor perspective using the case study of a design of a wireless communication chip for use in mobile phones. The second talk, from the viewpoint of a large consumer electronics manufacturer, discusses the needs and trends in embedded software design as well as tool support requirements. The final talk presents emerging techniques and tools towards the automatic generation of embedded software applications and platform-specific HdS code from system level models.

Organizers:

Rainer Doemer, University of California at Irvine, USA (doemer@uci.edu)
Andreas Gerstlauer, University of Texas at Austin, USA (gerstl@ece.utexas.edu)
Wolfgang Müller, University of Paderborn, Germany (wolfgang@acm.org)

Session Schedule:

Tuesday, January 20, 2009, 15:50 – 17:55

Detailed Presentation Schedule:

15:50 – 16:05
“Introduction to Hardware-dependent Software Design”
Rainer Dömer, University of California at Irvine, USA,
Andreas Gerstlauer, University of Texas at Austin, USA,
Wolfgang Müller, University of Paderborn, Germany

16:05 – 16:45
“Using a Dataflow abstracted Virtual Prototype for Hardware-dependent Software Design”
Wolfgang Ecker, Stefan Heinen, Michael Velten,
Infineon Technologies AG, Germany

16:45 – 17:15
“Needs and Trends in Embedded Software Development for Consumer Electronics”
Yasutaka Tsunakawa,
Sony Corp., Japan

17:15 – 17:55
“Hardware-dependent Software Synthesis for Many-Core Embedded Systems”
Samar Abdi, Gunar Schirner, Ines Viskic, Hansu Cho,
Yonghyun Hwang, Lochi Yu, and Daniel Gajski,
Center for Embedded Computer Systems, UC Irvine, USA

ASIA SOUTH PACIFIC DESIGN AUTOMATION CONFERENCE DAC

Mohammad Ali Ghodrat, Tony Givargis, and Alex Nicolau win Best Paper Award

(cont’d from pg. 3)

with loop dependency information is used to partition the iteration space of the nested loop. In such cases, the loop nest is decomposed such as to eliminate the conditional test, thus substantially reducing the execution time. Our technique completely eliminates the conditional from the loops (unlike previous techniques) thus further facilitating the application of other optimizations and improving the overall speedup. Applying the proposed transformation technique on loop kernels taken from Mediabench, SPEC-2000, mpeg4, qsdpcm and gimp, on average we measured a 175% (1.75X) improvement of execution time when running on a SPARC processor, a 336% (4.36X) improvement of execution time when running on an Intel Core Duo processor and a 198.9% (2.98X) improvement of execution time when running on a PowerPC G5 processor.
The CASES conference provides a forum for emerging technology in embedded computing systems, with an emphasis on compilers and architectures for embedded systems. CASES is a common forum for researchers with an interest in embedded systems to reach across vertically integrated communities and to promote synergies. As evident from the past CASES meetings, several emerging applications are critically dependent on these interactions for their sustained growth and evolution (from http://thedude.cc.gt.atl.ga.us/conferences/cases/).

CECS Annual Potluck '08

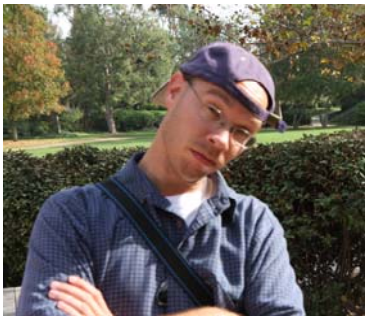
(cont'd from pg. 3)










PUBLICATIONS

The following papers were published by CECS affiliates between September 2008 to December 2008.

Focus	Title, Author, Publication
Network-on-a-Chip	Wolfgang Trumler, Sebastian Schlingmann, Theo Ungerer, Jun Ho Bahn and Nader Bagherzadeh, "Self-optimized Routing in a Network-on-a-Chip," 20th IFIP World Computer Congress, Milano, Italy 7-10 September 2008.
Supercapacitor-based Power Supply	Chulsung Park and Pai H. Chou, "TurboCap: Batteryless, Supercapacitor-based Power Supply for Mini-FDPM," to appear, in Proc. 3rd European Symposium on Supercapacitors and Applications (ESSCAP'08), Rome, Italy, November 6-7, 2008.
Video Stream Converter	T. Bohr, R. Doemer, "A Flexible Video Stream Converter", Center for Embedded Computer Systems, Technical Report 08-13, October 2008.
Hardware-dependent Software	W. Ecker, W. Müller, and R. Doemer, "Hardware-dependent Software - Principles and Practice," Springer, Boston, in print September 2008.
Hardware-dependent Software	W. Ecker, W. Müller, and R. Doemer, "Hardware-dependent Software - Introduction and Overview," Chapter 1 in "Hardware-dependent Software: Principles and Practice" (ed. W. Ecker, W. Müller, R. Doemer), Springer, Boston, in print September 2008.
Automatic Generation of Hardware-dependent Software	G. Schirner, R. Doemer, and A. Gerstlauer, "High-Level Development, Modeling and Automatic Generation of Hardware-dependent Software," Chapter 8 in "Hardware-dependent Software: Principles and Practice" (ed. W. Ecker, W. Müller, R. Doemer), Springer, Boston, in print September 2008.
On-Chip Interconnect	S. Pasricha and N.D. Dutt, "Trends in Emerging On-Chip Interconnect Technologies," IPSJ Transactions on System LSI Design Methodology, September 2008 (Invited Paper).
Mobile Embedded Systems	K. Lee, M. Kim, N. Dutt, N. Venkatasubramanian, "Error-Exploiting Video Encoder to Extend Energy/QoS Tradeoffs for Mobile Embedded Systems," Proceedings of the IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES2008), Milano, Italy, September 2008.
Protected Caches	K. Lee, A. Shrivastava, N. Dutt, N. Venkatasubramanian, "Data Partitioning Techniques for Partially Protected Caches to Reduce Soft Error Induced Failures," Proceedings of the IFIP Working Conference on Distributed and Parallel Embedded Systems (DIPES2008), Milano, Italy, September 2008.
Managing Power and Reliability in Hot Chips	A. Gupta, A. Djahromi, F. Kurdahi, A. Eltawil, and N. Dutt, "Managing Leakage Power and Reliability in Hot Chips Using System Floorplanning and SRAM Design," Proceedings of the 14th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC-2008), Rome, Italy, September 2008.
Multi-Granularity Embedded Processor	Y. Park, S. Pasricha, F. Kurdahi, N. Dutt, "Methodology for Multi-Granularity Embedded Processor Power Model Generation for an ESL Design Flow," Proceedings of the International Symposium on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2008), October 2008.
Multimedia Applications	K. Lee, A. Shrivastava, M. Kim, N. Dutt, N. Venkatasubramanian, "Mitigating the Impact of Hardware Failures on Multimedia Applications -- A Cross-Layer Approach," Proceedings of ACM Multimedia (Mutimedia2008), Vancouver, Canada, October 2008.
Video over Wireless Applications	A. Khajeh, M. Kim, N. Dutt, A. Eltawil and F. Kurdahi, "Cross-Layer Co-Exploration of Exploiting Error Resilience for Video over Wireless Applications," Proceedings of the 6th IEEE Workshop on Embedded Systems for Real Time Multimedia (ESTIMEDIA 2008), Atlanta, GA, October 2008.
Application Mapping on Chip-Multiprocessors	L. Bathen, S. Pasricha, and N. Dutt, "A Framework for Memory-aware Multimedia Application Mapping on Chip-Multiprocessors," Proceedings of the 6th IEEE Workshop on Embedded Systems for Real Time Multimedia (ESTIMEDIA 2008), Atlanta, GA, October 2008.

Continued on page 8

PUBLICATIONS (cont'd from pg 7)

The following papers were published by CECS affiliates during Winter 2008 quarter

Focus	Title, Author, Publication
MIMO Relay Network	Alireza S. Behbahani, Ricardo Merched and Ahmed Eltawil, "Optimizations of a MIMO Relay Network," IEEE Transactions on Signal Processing, vol.56, no.10, pp.5062-5073, October 2008.
L2 Cache Peripheral Circuits	H. Homayoun, A. Veidenbaum, and J-L. Gaudiot, "Adaptive Techniques for Leakage Power Management in L2 Cache Peripheral Circuits," Proceedings of the XXVI IEEE International Conference on Computer Design (ICCD 2008), Lake Tahoe, California, October 12-15, 2008.
Control Flow Optimization	M. Ghodrat, T. Givargis, A. Nicolau, "Control Flow Optimization in Loops using Interval Analysis," International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), pp. 157-166, Atlanta, October 2008.
System Codesign and Synthesis	F. Vahid, T. Givargis, "Highly-Cited Ideas in System Codesign and Synthesis," International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 191-196, Atlanta, October 2008.
Deterministic Service Guarantees	S. Choudhuri, T. Givargis, "Deterministic Service Guarantees for NAND Flash using Partial Block Cleaning," International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS), pp. 19-24, Atlanta, October 2008.
Partial Block Cleaning	S. Choudhuri, T. Givargis, "Real-Time Access Guarantees for NAND Flash using Partial Block Cleaning," Workshop on Software Technologies for Future Embedded & Ubiquitous Systems (SEUS), pp. 139-150, Italy, September 2008.
Multi-Client Multi-Radio Environment	Y. Agarwal, T. Pering, R. Want, R. Gupta, "SwitchR: Reducing System Power Consumption in a Multi-Client Multi-Radio Environment," 12th IEEE International Symposium on Wearable Computers (ISWC), October 2008.
Structured Time-Oriented Programming	F. Vahid and T. Givargis. Timing is Everything, "Embedded Systems Demand Teaching of Structured Time-Oriented Programming," IEEE/ACM Int. Conf. on Hardware/Software Codesign and System Synthesis, (CODES/ISSS), October 2008.
Dynamic Tuning of Configurable Architectures	C. Huang, D. Sheldon, and F. Vahid, "Dynamic Tuning of Configurable Architectures: The AWW Online Algorithm," IEEE/ACM Int. Conf. on Hardware/Software Codesign and System Synthesis, (CODES/ISSS), October 2008.
Pattern Counting ASIC Circuit for FPGAs	D. Sheldon and F. Vahid, "Don't Forget Memories: A Case Study Redesigning a Pattern Counting ASIC Circuit for FPGAs," IEEE/ACM Int. Conf. on Hardware/Software Codesign and System Synthesis, (CODES/ISSS), October 2008.
System Codesign and Synthesis	F. Vahid and T. Givargis, "Highly-Cited Ideas in System Codesign and Synthesis," IEEE/ACM Int. Conf. on Hardware/Software Codesign and System Synthesis, (CODES/ISSS), October 2008.
FPGA-Enhanced Compute Platforms	C. Huang and F. Vahid, "Dynamic Coprocessor Management for FPGA-Enhanced Compute Platforms," IEEE/ACM Int. Conf. on Compilers, Architectures, and Synthesis for Embedded Systems (CASES), Oct ober 2008.
Fault Tolerant Error Concealment	Mohammad A Makhzan (Avesta Sasan), Amin Khajeh, Ahmed Eltawil, and Fadi J. Kurdahi, "A Low Power JPEG2000 Encoder with Iterative and Fault Tolerant Error Concealment," Accepted to IEEE Transactions on Very Large Scale Integration Systems, 2008.

CECS—*promoting creativity and pursuing discovery!*

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

CECS eNews
Center for Embedded Computer Systems
2010 Anteater Instruction & Research Building
University of California, Irvine
Email: enews@cecs.uci.edu