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CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights

- **DAC 2011**
- **Student Profile: Ahmed Nassar**
- **Project Profile: Multichannel Clock and Data Recovery: A Synchronous Approach**
- **Project Profile: Pruning Hardware Evaluation Space via Correlation Driven Application Similarity Analysis**

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CECS @ DAC 2011 - San Diego

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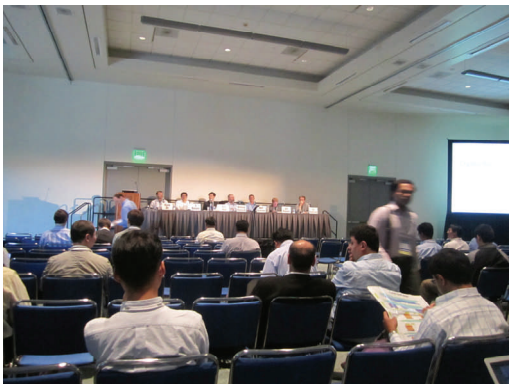
The 48th DAC conference was held at the San Diego Convention Center between June 5, 2011 to June 9, 2011. CECS faculty and students presented several papers and technical sessions.

Prof. Daniel Gajski chaired the System-Level Power Management technical session, which focused on power management techniques for creating power-efficient designs. CECS alumni Dongwan Shin and Youngyun Kim presented "Dynamic Voltage of OLED Displays" in this session along with Prof. Naehyuck Chang and Prof. Massoud Pedram.



The Special Session on Embedded Multiprocessor Software Synthesis was chaired by Prof. Peter Marwedel and Prof. Daniel Gajski. Organizers included Professors Andreas Gerstlauer, Christian Haubelt, and Erlangen-Nurnberg. This session presented state-of-the-art approaches for embedded multi-processor software development.

Prof. Nikil Dutt co-organized the Work-in-Progress Poster session along with Prof. Soha Hassoun. This WIP poster session is new to the DAC program and is designed to allow authors a chance to present their ideas to industry peers in hopes of initiating discussion and getting feedback in the earlier stages of the projects.

CECS students also participated in the Sigda PhD Forum:

- Luis Bathen, *SeReVraL: Secure, Reliable and Dynamic Virtualization Layer for On-Chip Distributed Memories* 38
- Hessam Kooti, *Real-Time Scheduling for Embedded Systems* 12

For more information, including papers, proceedings, and photos, visit the DAC website at:
http://www.dac.com/dac+2011.aspx

STUDENT & PROJECT PROFILES

Student Profile: Ahmed Nassar

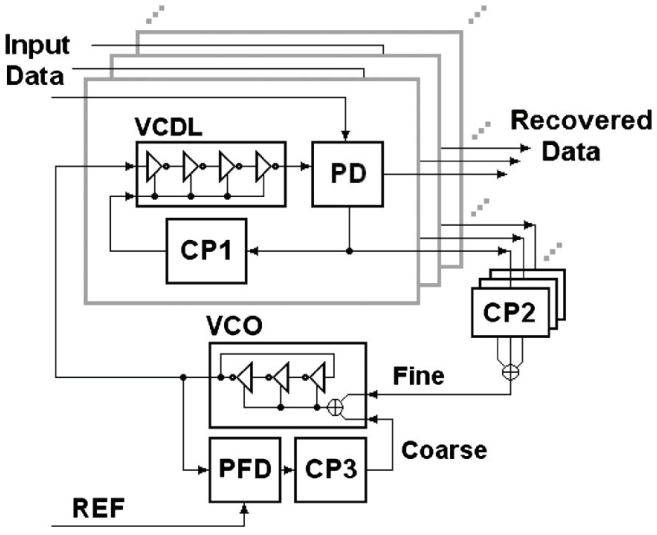
- Staff

Ahmed Nassar received his B.Sc. degree in electrical and communications engineering from Alexandria University, Alexandria, Egypt in 2002. Immediately afterwards, he worked for five years on signal integrity of high-speed digital designs at military and civilian telecom equipment manufacturers. He later joined Newport Media, a world leader in mobile TV technology, as a digital VLSI designer. Meanwhile, in his M.Sc. thesis (obtained from Cairo University, Cairo, Egypt in 2010), he did work on multichannel multi-Gbps clock and data recovery circuits published in IEEE TCAS. During the Spring of 2010, he did brief research on model-order reduction of nonlinear analog circuits at the University of Paris-6, Paris, France. Since Fall quarter, 2010, he has been working toward his PhD. degree at the University of California, Irvine.

His current research interests include digital VLSI design and verification methodologies and EDA, and architectural support for debugging of multithreaded programs on many-core multiprocessors. He is a student member of the Institute of Electrical and Electronics Engineers (IEEE).

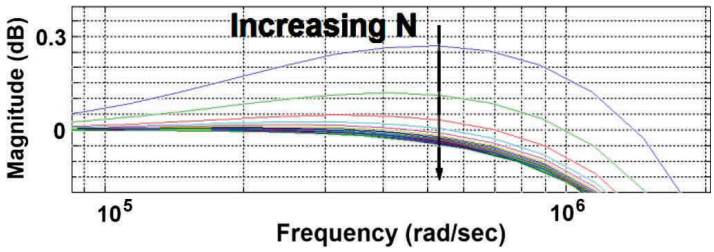
Project Profile:
Multichannel Clock and Data Recovery: A Synchronous Approach

- By Ahmed Nassar, Ahmed Emira, Ahmed Nader Mohieldin, and Ahmed Hussien



Conceptual multichannel CDR architecture proposed in this brief.

This brief proposes a scalable multichannel clock and data recovery architecture that exploits the synchrony of multiple point-to-point serial links and uses a single voltage-controlled oscillator (VCO) to drive multiple phase detection loops. The proposed architecture can be naturally reduced by design to an ensemble of weakly interacting delay-locked loops. As a result, the jitter peaking problem is asymptotically eliminated, which makes this architecture well suited for use in long-haul repeater chains. Moreover, it allows controlling VCO jitter transfer to the recovered clock without affecting data jitter transfer. The architecture is demonstrated both by a Verilog-A behavioral model along with a rigorous system and statistical analysis.



Peaking of the closed-loop transfer function of every channel as a function of the number of channels.

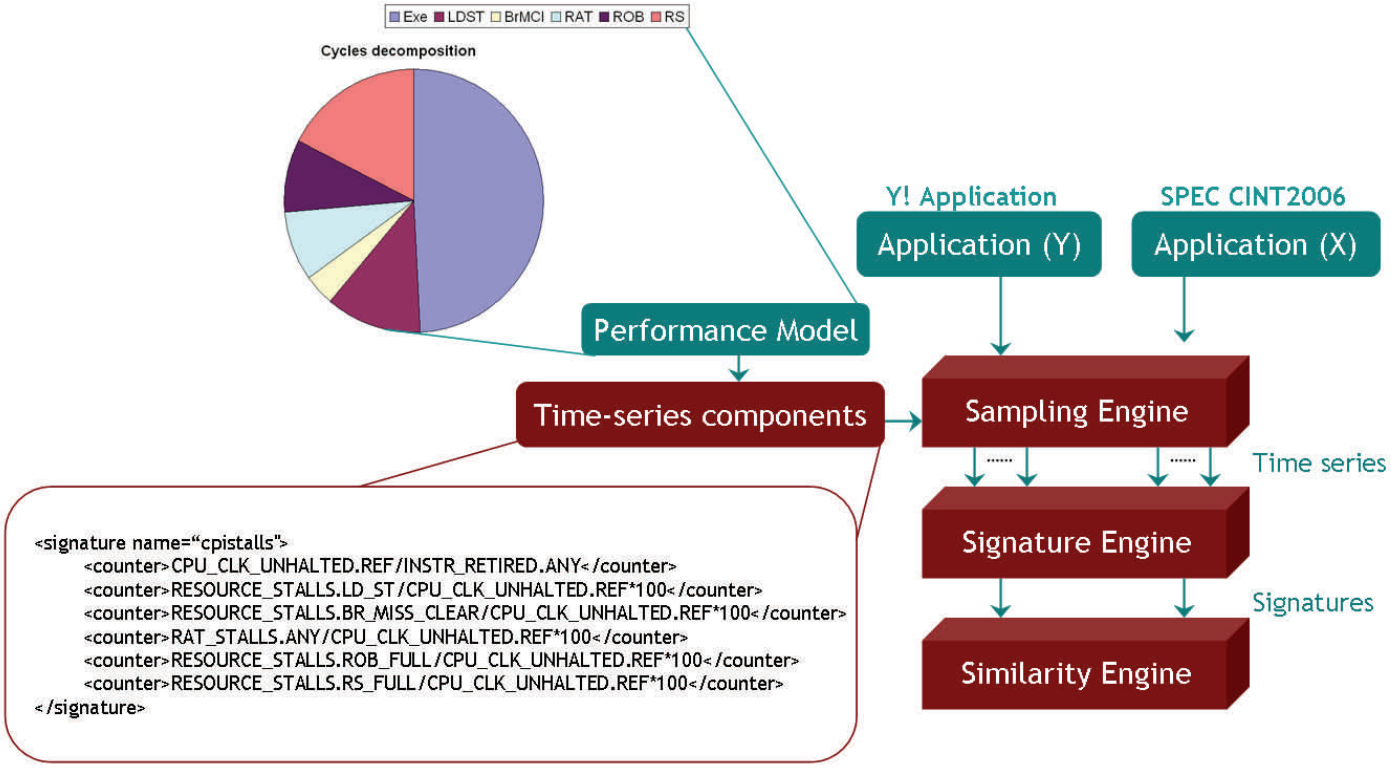
Project Profile: Pruning Hardware Evaluation Space via Correlation Driven Application Similarity Analysis

- Rosario Cammarota, Arun Kejariwal, Paolo D'Alberto, Sapan Panigrahi, Alexander V. Veidenbaum, and Alexandru Nicolau

System evaluation is routinely performed in industry to select one amongst a set of different systems to improve performance of proprietary applications. However, a wide range of system configurations is available every year on the market. This makes an exhaustive system evaluation progressively challenging and expensive.

In this paper we propose a novel similarity-based methodology for system selection. Our methodology prunes the set of candidate systems by eliminating those systems that are likely to reduce performance of a given proprietary application. The pruning process relies on applications that are similar to a given application of interest whose performance on the candidate systems is known. This obviates the need to install and run the given application on each and every candidate system.

The concept of similarity we introduce is performance centric. For a given application, we compute the Pearson's correlation between di♂erent types of resource stall and cycles per instruction. We refer to the vector of Pearson's correlation coefficients as an application signature. Next, we assess similarity between two applications as Spearman's correlation between their respective signature. We use the former type of correlation to quantify the association between pipeline stalls and cycles per instruction, whereas we use the latter type of correlation to quantify the association of two signatures, hence to assess similarity, based on the difference in terms of rank ordering of their components.



Overview of the methodology

We evaluate the proposed methodology on three different micro-architectures, viz., Intel's Harpertown, Nehalem and Westmere, using industry-standard SPEC CINT2006. We assess performance centric similarity among applications in SPEC CINT2006. We show how our methodology clusters applications with common performance issues. Finally, we show how to use the notion of similarity among applications to compare the three architectures with respect to a given Yahoo! property.

PUBLICATIONS

The following papers were published by CECS affiliates between April 2011 to July 2011 (and unreported papers from previous eNews).

Focus	Title, Author, Publication
Energy Harvesting Sensor Networks	Nga Dang, Elaheh Bozorgzadeh, Nalini Venkatasubramanian, **"QuARES: Quality-aware Data Collection in Energy Harvesting Sensor Networks",** in International Green Computing Conference (IGCC'11), Orlando, Florida, 25-28th July 2011
Frequency Synthesis	Zhiming Chen, Chun-Cheng Wang, Payam Heydari, **"W-Band Frequency Synthesis Using a Ka-Band PLL and Two Different Frequency Triplers,"** IEEE RFIC Symposium, June 2011.
System Level Modeling	C. Chang, R. Doemer, **"System Level Modeling of a H.264 Video Encoder",** Center for Embedded Computer Systems, Technical Report 11-04, June 2011.
Transaction-Level Modeling	X. Han, W. Chen, R. Doemer, **"A Parallel Transaction-Level Model of H.264 Video Decoder",** Center for Embedded Computer Systems, Technical Report 11-03, June 2011.
Distributed Amplifier	Amin Jahanian, Payam Heydari**, "A CMOS 818-GHz GBW Differential Distributed Amplifier with Distributed Active Input Balun,"** IEEE RFIC Symposium, June 2011. (Nominated for the Best Paper Award)
MIMO Decoder	C.-A. Shen, A. M. Eltawil, K. N. Salama, and S. Mondal, **"A best-first soft/hard decision tree searching MIMO decoder for a 4×4 64-QAM system,"** IEEE Transactions on Very Large Scale Integration (VLSI) Systems Accepted for Publication, June 2011.
On-Chip Antenna	Chun-Cheng Wang, Zhiming Chen, Payam Heydari, **"A Fully Integrated 96GHz 2×2 Focal-Plane Array with On-Chip Antenna,"** IEEE RFIC Symposium, June 2011. (Nominated for the Best Paper Award)
Thread Warping	G. Stitt and F. Vahid, **"Thread Warping: Dynamic and Transparent Synthesis of Thread Accelerators,"** ACM Trans. on Design Automation of Electronic Systems (TODAES), Vol 16, Issue 3, June 2011, 21 pages.
Just-in-Time Compilation	A. Becker, S. Sirowy, F. Vahid, **"Just-in-Time Compilation for FPGA Processor Cores,"** IEEE Electronic System Level Synthesis Conf. (ESLsyn), June 2011.
Cyber-Physical Systems	B. Miller, T. Givargis, F. Vahid, **"Application-Specific Codesign Platform Generation for Digital Mockups in Cyber-Physical Systems,"** IEEE Electronic System Level Synthesis Conf. (ESLsyn), June 2011.
Scalable Object Detection	C. Huang, F. Vahid, **"Scalable Object Detection Accelerators on FPGAs Using Custom Design Space Exploration,"** IEEE Symposium on Application Specific Processors (SASP), June 2011
Model-Based Power Characterization	John McCullough, Yuvraj Agarwal, Jaideep Chandrashekhar, Sathyanarayanan Kuppuswamy, Alex Snoeren, Rajesh K. Gupta, **"Evaluating the Effectiveness of Model-Based Power Characterization,"** In Proceedings of the USENIX Annual Technical Conference (USENIX ATC '11), Portland, June 2011.
SoC Environment	W. Chen, X. Han, R. Doemer, **"Multicore Simulation of Transaction-Level Models Using the SoC Environment",** IEEE Design & Test of Computers, vol. 28, no. 3, pp. 20-31, May-June 2011.
Causality-Driven Application Analysis	R. Cammarota, A. Kejariwal, P. D'Alberto, S. Panigrahi, A. Veidenbaum, and A. Nicolau, **"Pruning Hardware Evaluation Space via Causality-Driven Application Similarity Analysis,"** ACM International Conference on Computing Frontiers (CF'11) May 2011.
Distributed Parallel Simulator	W. Chen, R. Doemer, **"A Distributed Parallel Simulator for Transaction Level Models with Relaxed Timing",** Center for Embedded Computer Systems, Technical Report 11-02, May 2011.

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PUBLICATIONS

The following papers were published by CECS affiliates between April 2011 to July 2011 (and unreported papers from previous eNews) - continued from page 4...

Focus	Title, Author, Publication
Distributed Delay Circuits	Amin Jahanian, Payam Heydari, **"Analysis and Optimization of Distributed Delay Circuits,"** IEEE Int'l Symp. on Circuits and Systems (ISCAS), May 2011.
EcoCast Macroprogramming	Yi-Hsuan Tu, Yen-Chiu Lee, Ting-Chou Chien, and Pai H. Chou, **"EcoCast: Interactive, Object-Oriented Macroprogramming for Networks of Ultra-Compact Wireless Sensor Nodes,"** in Proc. the 10th International Conference on Information Processing in Sensor Networks (IPSN 2011), Chicago, IL, USA, April 12-14, 2011. pp. 366--377. (27/122 = 22% acceptance rate).
HVAC Control	Yuvraj Agarwal, Bharathan Balaji, Seemanta Dutta, Rajesh K Gupta, Thomas Weng, **"Duty-Cycling Buildings Aggressively: The Next Frontier in HVAC Control,"** International Conference on Information Processing in Sensor Networks: Sensor Platforms, Tools and Design Methods (IPSN/SPOTS), April 2011.
Sensor Localization	Ryo Sugihara, Rajesh K. Gupta, **"Sensor Localization with Deterministic Accuracy Guarantee,"** IEEE International Conference on Computer Communications (IEEE INFOCOM), April 2011.
RF-Correlation-Based Impulse-Radio	Lei Zhou, Zhiming Chen, Chun-Cheng Wang, Fred Tzeng, Vipul Jain, and Payam Heydari, **"A 2Gbps RF-Correlation-Based Impulse-Radio UWB Transceiver Front-End in 130nm CMOS,"** IEEE Trans. on Microwave Theory and Techniques - Special Issue on UWB Technologies, vol. 59, April 2011.
Cryptography Algorithms	Jed Kao-Tung Chang, Chen Liu, Shaoshan Liu, and Jean-Luc Gaudiot, **"Workload Characterization of Cryptography Algorithms for Hardware Acceleration,"** Proceedings of the 2nd ACM International Conference on Performance Engineering (ICPE 2011), Karlsruhe, Germany, March 14-16, 2011
System-Level Models	Lan S. Bai, Robert P. Dick, Pai H. Chou, Peter A. Dinda, **"Automated Construction of Fast and Accurate System-Level Models For Wireless Sensor Networks",** in Proc. Design, Automation & Test in Europe (DATE), March 2011.
Faulty Sensor Networks	Lan S. Bai, Robert P. Dick, Peter A. Dinda, and Pai H. Chou, **"Simplified Programming of Faulty Sensor Networks via Code Transformation and Run-Time Interval Computation",** in Proc. Design, Automation & Test in Europe (DATE), March 2011.
Smart Wireless Sensor System	Sehwan Kim, Eunbae Yoon, Hadil Mustafa, Pai H. Chou, and Masanobu Shinozuka, **"Smart Wireless Sensor System for Lifeline Health Monitoring under a Disaster Event",** in Nondestructive Characterization for Composite Materials, Aerospace Engineering, Civil Infrastructure, and Homeland Security IV, March 2011. San Diego, CA USA
CMOS Amplifiers	Deyi Pi, Byung-Kwan Chun, and Payam Heydari, **"A Synthesis-Based Bandwidth Enhancement Technique for CMOS Amplifiers: Theory and Design,"** IEEE J. Solid-State Circuits, vol. 45, Feb. 2011.
Energy Efficiency	Jie Tang, Shaoshan Liu, Zhimin Gu, Chen Liu, and Jean-Luc Gaudiot, **"Prefetching in Embedded Mobile Systems Can Be Energy-Efficient,"** Computer Architecture Letters, DOI: http://doi.ieeecomputersociety.org/10.1109/L-CA.2011.2, February, 2011
Radiometer Systems	Lei Zhou, Chun-Cheng Wang, Zhiming Chen, and Payam Heydari, **"A W-band CMOS Receiver Chipset for Millimeter-Wave Radiometer Systems,"** IEEE J. Solid-State Circuits, vol. 45, Feb. 2011.
Network-on-Chip Design	Chifeng Wang, Wen-Hsiang Hu, Bagherzadeh, N., **"A Wireless Network-on-Chip Design for Multicore Platforms,"** Parallel, Distributed and Network-Based Processing (PDP), 2011 19th Euromicro International Conference on , pp.409-416, 9-11 Feb. 2011.

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CECS—*promoting creativity and pursuing discovery!*

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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The following papers were published by CECS affiliates between April 2011 to July 2011 (and unreported papers from previous eNews) - continued from page 5...

Network-on-Chip Architecture	Chifeng Wang, Wen-Hsiang Hu, Seung Eun Lee, Nader Bagherzadeh, **"Area and Power-efficient Innovative Congestion-aware Network-on-Chip Architecture,"** Journal of Systems Architecture, Volume 57, Issue 1, Special Issue On-Chip Parallel And Network-Based Systems, January 2011, Pages 24-38.
Matrix Multiplications on GPUs	Matthew Badin, Lubomir Bic, Michael B. Dillencourt, Alexandru Nicolau, **"Improving accuracy for matrix multiplications on GPUs,"** Scientific Programming 19(1): 3-11 (2011)
Reconfigurable Architectures	Ganghee Lee, Kiyoung Choi, Nikil D. Dutt, **"Mapping Multi-Domain Applications Onto Coarse-Grained Reconfigurable Architectures,"** IEEE Trans. on CAD of Integrated Circuits and Systems 30(5): 637-650 (2011)
Embedded Processors	Young-Hwan Park, Sudeep Pasricha, Fadi J. Kurdahi, Nikil D. Dutt, **"A Multi-Granularity Power Modeling Methodology for Embedded Processors,"** IEEE Trans. VLSI Syst. 19(4): 668-681 (2011)
Voltage Scaling	A. Sasan, K. Amiri, H. Homayoun, A. Eltawil, and F. J. Kurdahi., **"Variation trained drowsy cache (VTD-cache): A history trained variation aware drowsy cache for fine grain voltage scaling,"** IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011.
Scalable Network-on-Chip	P. M Yaghini, H. Pedram, A. Eghbal, and H.R. Zarandi, **"An scalable GALS Network-on-Chip asynchronous Router,"** Elsevier Computer and Electrical Engineering Journal -- Submitted.