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Center for Embedded Computer Systems, University of California, Irvine

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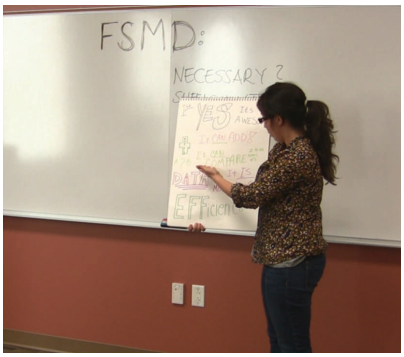
Online Course Videos 2.0: *Digital Design Idol* series

- Staff

CECS Professor Daniel Gajski has renewed students' interests in the EECS 31L Digital Logic Design Lab course with online videos and interactive activities.

In addition to the online course videos already on the 31L web site, two additional *Digital Design Idol* videos were filmed Winter '11 Quarter where a select number of students compete for extra points in the course by answering a question related to Digital Design.

The contestants are graded by CECS faculty members and guest judges based on presentation, thoroughness, and other factors. For the latest installments of *Digital Design Idol*, the judges included Prof. Rainer Doemer, Prof. Fadi Kurdahi, Prof. Brian Demsky, and Prof. Athina Markopoulou.



Digital Design Idol

VISITOR & PROJECT PROFILES

Visitor Profile: Junsoo Hwang

- Staff

Junsoo Hwang joined the Center for Embedded Computer Systems at UCI in December, 2010 as a short-term visiting scholar hosted by Professor Pai Chou. He is the Deputy Director in the Better Business Climate Division of the Ministry of Knowledge and Economy (MKE) in South Korea. He was selected for the Korean Government Overseas Fellowship last year and he got an opportunity to study in the United States.

His research topic is as follows: The policy in USA for Improving the productivity using information technology; a good example is using IT for improving productivity in major industry sector such as automobile, heavy chemical industry, etc. "It is getting difficult to improve industry's productivity by using labor power. Now lots of countries focus on new policy to improve in efficiency by using IT system. I think United States is the best country for the subject because IT system is not only well used but also makes very high efficiency in many fields," Junsoo Hwang says.

Project Profile: Reliability Enhancement against Soft Errors in SRAM-based Programmable Systems

- By Shahin Golshan

Trends are shifting towards FPGA-based designs due to their shorter time-to-market, ability to re-program in the field to fix errors and lower non-recurring engineering costs. However, in spite of their advantages over ASIC designs, FPGA designs are becoming more sensitive to soft errors. Soft errors are defined as faults causing errors in functionality while no physical damage is incurred to the circuitry. Soft error in FPGA designs manifests itself as a permanent fault when it upsets memory bit. Functionality and connectivity of circuits implemented on FPGAs can be damaged if a single event upsets (SEU) caused by soft error flips a configuration bit.

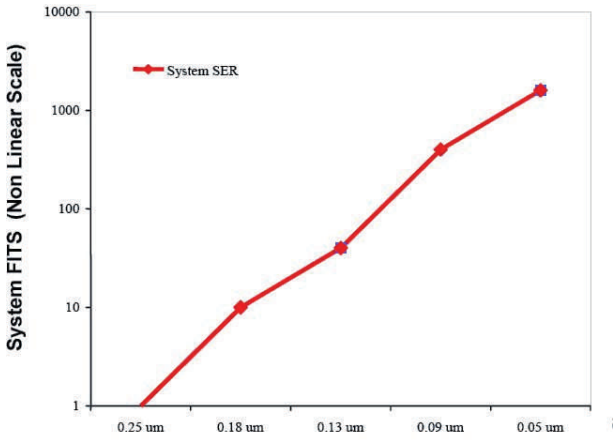


Figure 1: Failure-in-time for different technologies

Soft error is one of the main challenges against wide use of FPGAs in critical operations due to shrinking feature size, high density, increase in operation temperature and lower operating voltages. As depicted in Figure 1, the failure-in-time (FIT) rate of FPGA systems are expected to grow exponentially as the technology scaled down. Recent studies show that SRAM-based FPGAs are rather more vulnerable to SEUs than their ASIC counterparts. In order to mitigate the impact of SEUs on FPGAs, several orthogonal strategies are employed in different stages of FPGA CAD flow. These strategies in general either try to filter out the propagation of faults to the outputs of the designs through redundancy (TMR), or try to control and constrain the operating conditions (e.g. temperature) to enhance the immunity of the SRAMs against SEUs. In our work, we study both strategies in details.

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STUDENT & PROJECT PROFILES

Student Profile: Shahin Golshan

- Staff

Shahin Golshan received the B.S. degree in Computer Engineering from Sharif University of Technology, Tehran, Iran in 2005, and the M.S. degree in Systems from the University of California, Irvine (UCI) in 2009, where he is currently working toward the PhD. Degree.

His research interests include VLSI/FPGA computer aided design, design automation for embedded systems (high level synthesis and physical design algorithms) with emphasis on low power and reliability, and reconfigurable computing. He is a member of the Association for Computing Machinery (ACM) and the Institute of Electrical and Electronics Engineers (IEEE).

Project Profile: Reliability Enhancement against Soft Errors in SRAM-based Programmable Systems (continued from page 2)...

Although Triple Modular Redundancy (TMR) has been widely used to mitigate Single Event Upsets (SEUs) in SRAM-based FPGAs, SEU-caused bridging faults between the TMR modules do not guarantee the correctness of TMR design under SEU. It has been observed that 10% of SEUs in routing configurations produce multiple errors that TMR is not able to filter out. When replicas of TMR are placed too close to each other (**Figure 2**), SEU-caused bridging faults between TMR replicas does not guarantee correctness of TMR design. Once an SEU-induced flip in the routing configuration bit connects the two nets in Figure 2-b, the bridging fault causes interference of the signals carried by the nets of the two replicas.

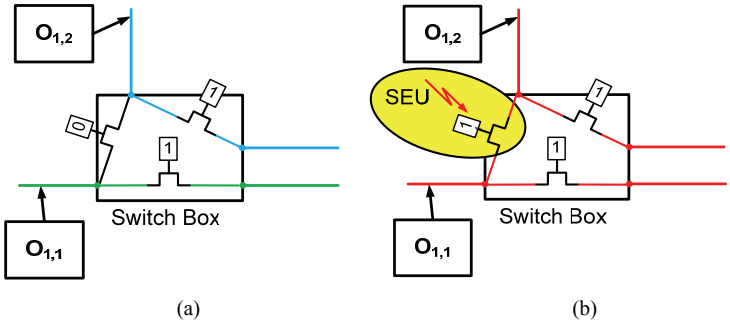

Figure 2: Bridging fault affect in TMR-based FPGA ($O_{1,1}$ and $O_{1,2}$ are two replicas of operation O_1)

While several related works focus on removal of such TMR breaches in FPGAs in physical design stages, we focus on SEU mitigation for redundancy-based designs inside all the stages of the CAD flow for SRAM-based FPGAs. we also extend the concept of containment of SEUs within a single TMR replica to each stage of the CAD flow (**Figure 3**).

In my thesis, we present a novel CAD flow for redundancy-based applications on FPGAs in order to mitigate the impact of SEUs in the configuration bit streams. Based on our previous works, we have introduced the notions of *modular redundancy conflicts* and *vulnerability-gap conflicts* which maintain the fundamental assumption underlying the integrity of redundancy-based designs (i.e. self-containment of SEU-induced faults within a single replica of redundant resources). We consider SEU-awareness for redundancy-based designs during all the stages of design flow: high-level synthesis, floorplanning and placement, and routing. By applying our design flow technique, on average, we can achieve 41.5%, 44.7% and 50.1% improvements in terms of the number of SEU-induced faults for TMR ratios of 10%, 20% and 50% respectively, in comparison to the case where bridging faults are not considered in high-level synthesis.

Figure 3: SEU-aware design flow stages

PUBLICATIONS

The following papers were published by CECS affiliates between January 2011 to March 2011 (and unreported papers from previous eNews).

Focus	Title, Author, Publication
Hardware Evaluation Space Pruning	Cammarota R., Kejariwal A., D'Alberto P., Panigrahi S., Nicolau A., Veidenbaum A., **"Pruning Hardware Evaluation Space via Correlation-Driven Application Similarity Analysis,"** to appear in ACM International Conference on Computing Frontiers (CF'11).
Resource Management	Houman Homayoun, Avesta Sasan, Jean-Luc Gaudiot, and Alex Veidenbaum, "**Reducing Power in All Major CAM and SRAM-Based Processor Units via Centralized, Dynamic Resource Size Management,"** *IEEE Transactions on Very Large Scale Integration Systems, in press*
Hardware Acceleration	Jed Kao-Tung Chang, Chen Liu, Shaoshan Liu, and Jean-Luc Gaudiot, "**Workload Characterization of Cryptography Algorithms for Hardware Acceleration,"** *Proceedings of the 2nd ACM International Conference on Performance Engineering (ICPE 2011), Karlsruhe, Germany, March 14-16, 2011*
Wireless Sensor Networks	Lan S. Bai, Robert P. Dick, Pai H. Chou, Peter A. Dinda, **"Automated Construction of Fast and Accurate System-Level Models For Wireless Sensor Networks,"** to appear, in *Proc. Design, Automation & Test in Europe* (DATE), March 2011.
Faulty Sensor Networks	Lan S. Bai, Robert P. Dick, Peter A. Dinda, and Pai H. Chou, **"Simplified Programming of Faulty Sensor Networks via Code Transformation and Run-Time Interval Computation,"** to appear, in *Proc. Design, Automation & Test in Europe* (DATE), March 2011.
RAIDs-on-Chip	L. Bathen and N. Dutt, **"E-RoC: Embedded RAIDs-on-Chip for Low Power Distributed Dynamically Managed Reliable Memories,"** Proceedings of the 2011 Conference on Design, Automation and Test in Europe (DATE 2011), March 2011.
Reconfigurable Arrays	G. Ansaloni, K. Tanimura, L. Pozzi, and N. Dutt, **"Slack-aware Scheduling on Coarse Grained Reconfigurable Arrays,"** Proceedings of the 2011 Conference on Design, Automation and Test in Europe (DATE 2011), March 2011.
Smart Wireless Sensor Systems	Sehwan Kim, Eunbae Yoon, Hadil Mustafa, and Pai H. Chou, **"Smart Wireless Sensor System for Lifeline Health Monitoring under a Disaster Event,"** in *Nondestructive Characterization for Composite Materials, Aerospace Engineering, Civil Infrastructure, and Homeland Security IV*," March 2011. San Diego, CA USA
Next-Generation Non-Volatile Memories	J. Coburn, A.M. Caulfield, A. Akel, L.M. Grupp, R.K. Gupta, R. Jhala, S. Swanson, **"NV-Heaps: Making Persistent Objects Fast and Safe with Next-Generation, Non-Volatile Memories,"** *The Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2011.
Smart Microgrid	Yuvraj Agarwal, Thomas Weng, And Rajesh Gupta, **"Understanding the Role of Buildings in a Smart Microgrid,"** *Design and Test Europe (DATE)*, March 2011.
Cyber-Physical Systems	Rahul Balani, Kaisen Lin, Lucas Wanner, Jonathan Friedman, Mani Srivastava and Rajesh Gupta, **"Programming Support for Distributed Optimization and Control in Cyber-Physical Systems,"** *ACM/IEEE Second International Conference on Cyber-Physical Systems (ICCPS)*, March 2011.
Embedded Mobile Systems	Jie Tang, Shaoshan Liu, Zhimin Gu, Chen Liu, and Jean-Luc Gaudiot, **"Prefetching in Embedded Mobile Systems Can Be Energy-Efficient,"** *Computer Architecture Letters, DOI: http://doi.ieeecomputersociety.org/10.1109/L-CA.2011.2, February, 2011*
Deterministic Accuracy	Ryo Sugihara, Rajesh K. Gupta, **"Clock Synchronization with Deterministic Accuracy Guarantee,"***European Conference on Wireless Sensor Networks (EWSN)*, February 2011.
Multi-Core Parallel Simulation	R. Doemer, W. Chen, X. Han, A. Gerstlauer, **"*Multi-Core Parallel Simulation of System-Level Description Languages*,"** Proceedings of the Asia and South Pacific Design Automation Conference 2011, Yokohama, Japan, January 2011.

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Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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