Volume 10, Issue 2
Spring '10

CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights

- **CECS Ranks 6th in the World for Hardware and Architecture.**
- **CECS Members chair Technical Sessions at DAC 2010**
- **Visitor Profile: Dr. Hyungkeun Lee**
- **Project Profile: Hybrid Instruction Set Simulator by Yitao Guo**

Inside this Issue:

Microsoft Ranking Places CECS 6th in the World!

- CECS Staff

The recently published Academic Research Ranking by Microsoft Corp (http://academic.research.microsoft.com/) ranks 20 Computer Science topics from Algorithms and Theory to the World Wide Web including 2.4 million publications. In the specific topic titled Hardware and Architecture, which is particularly pertinent to the UCI Center for Embedded Computer Systems (CECS), it ranks over one-hundred thousand researchers world wide. CECS is very highly ranked by sharing 6th place with MIT, UCLA, Princeton and UIUC with 4 faculty in the top 100. First on the list is UCB with 10 in 100, followed by Stanford with 9, Michigan with 7 and UCSD and CMU with 5 faculty members in the top 100.

This faculty ranking affirms CECS reputation as one of the leading centers for embedded systems research and technology.

"I heartily extend my congratulations to the Center for Embedded Computer Systems faculty, students and staff. It is an honor for the Samueli School faculty to be listed among the world's top faculty in the field of computer hardware and architecture," said Rafael L. Bras, distinguished professor and dean of The Henry Samueli School of Engineering.

Prof. Gajski, the CECS Director, said that he is very happy that the research of CECS faculty has been recognized and appreciated around the world. He is also hoping that such recognition will help improve the ranking of our schools, the School of ICS and the School of Engineering, as well as improving the standing of UCI in the ranking of world universities (http://www.arwu.org/#).

CECS Members Chair several Technical Sessions at Design Automation Conference 2010

- CECS Staff

CECS members continue their presence in hot topic areas such as High-Level Synthesis, Embedded Software, SRAMs, and Computing without Guarantees at the 47th Design Automation Conference, held June 13-18, 2010, at the Anaheim Convention Center.

Embedded Software

Prof. Eli Bozorgzadeh chaired the "Embedded Software Timing Matters!" session on Tuesday, June 15, 2010. The following is the excerpt from the Final Program at DAC:

Software execution time is one of the most important issues in embedded system design and takes different forms that depend on the application context. The first paper presents a method to optimize both latency and throughput of packet-processing systems in a soft real-time context. Focusing on hard real-time systems, the second paper discusses a scheduling approach to optimize energy efficiency. How

CECS Members Chair several Technical Sessions at Design Automation Conference 2010 (continued from front page)

to estimate the worst-case execution time of Esterel programs for multiprocessors is the subject of the third paper. The session is concluded by a paper that presents an efficient implementation of breadth-first search on Graphics Processing Unit (GPU).

SRAMs

Prof. Payam Heydari's session on "Variation-aware Methods for SRAMs and Clocks" was held on Thursday, June 17, 2010. The following excerpt is from the Final Program:

In this session, novel variation-aware methods for SRAMs and clocks are discussed. The first paper proposes a non-invasive method to measure threashold variations in SRAMs. The second paper discusses a method for doing statistical analysis during the design phase of SRAMs for the purpose of improving the parametric yield. The third paper proposes a mechanism for creating clock to enable pre-bond testability of dies in 3-D stacked ICs. The last paper proposes a method for clock-tree design to support on-chip skew detection and correction.

High-Level Synthesis

Prof. Daniel Gajski chaired the "Panel: What Input Language is the Best Choice for High-Level Synthesis" session on June 17, 2010. The excerpt from the Final Program is as follows:

As of 2010, over 30 of the world's top semiconductor/systems companies have adopted HLS. In 2009, tape-outs for SOCs containing IP developed with HLS exceeded 50 for the first time. Now that the practicality and value of HLS is established, engineers are asking the question of "what input-language works best?" The answer to this question is critical because it drives key decisions regarding the tool/methodology infrastructure companies will create around this new flow. ANSI-C/C++ advocates cite ease-of-learning and simulation speed. SystemC advocates make similar claims and point to SystemC's hardware-oriented features. Proponents of BSV (Bluespec SystemVerilog) claim that the language enhances architectural transparency and control. To realize the full benefits of HLS, companies must consider all of these factors and then make a choice that is right for their flow.

Computing without Guarantees

Finally, Prof. Fadi Kurdahi was the chair of "Special Session: Computing without Guarantees" on June 17, 2010. The following is the excerpt for this session from the Final Program:

The process of electronic system design has traditionally conformed to an axiom—that the specification and implementation need to be equivalent in a numerical or Boolean sense. However, a wide range of application domains, ranging from digital signal processing, multimedia processing, and wireless communications actually do not require such a strong notion of equivalence, due to the presence of noise in the input data and the limited perceptual ability of humans consuming their output. Emerging workloads of the future, such as Recognition, Mining, and Synthesis, take this "inherent resilience" to a different level due to the massive amounts of data they process, statistical nature of the algorithms, and built-in expectation of less than perfect results. Several recent research efforts attempt to exploit this inherent resilience of algorithms to obtain unprecedented levels of performance or energy-efficiency in hardware and software implementations.

For more information about these technical sessions, or DAC in general, please visit the official DAC site at http://www.dac.com/.

VISITOR & PROJECT PROFILES

Visitor Profile: Dr. Hyungkeun Lee

- CECS Staff

Professor Hyungkeun Lee joined the Center for Embedded Computer Systems at UCI in September, 2009 as a visiting scholar hosted by Professor Pai Chou. He received his BS degree in Electronic Engineering from Yonsei University, Korea in 1987 and his MS and PhD degrees in Computer Engineering from Syracuse University, NY in 1998 and 2002, respectively. He had been a research engineer with Samsung Electronics since 1987 and joined the Department of Computer Engineering at Kwangwoon University in Korea in 2003.

His research interests are in ad hoc networks, sensor networks, wireless mesh networks, cross-layer design/optimization for wireless networks, and WLAN. In recent years, he has participated in the development of MAC protocols for IEEE 802.11n and the design of a new MAC protocol for IEEE 802.15.4 in Korea. He is also working on tactical data links and their interoperability, which are standardized radio communication links used for defense systems.

Project Profile: A Hybrid Instruction Set Simulator for System Level Design

- By Yitao Guo

Validation is an essential step in System Level Design (SLD) for Multiprocessor System on Chip (MPSoC). Traditional Instruction Set Simulators (ISS) are often either slow (interpretive ISS) or unable to handle accurate multiprocessor simulation (static or dynamically compiled ISS).

We propose a hybrid simulation scheme which combines interpreted and static compiled ISS. The proposed ISS is free to execute a target function either natively or in interpreted mode. With the aid of System Level Description Languages (SLDL) like SpecC/SystemC, the designer using proposed ISS is able to di♂erentiate the computation portion and the communication portion of the target code. By executing the computation intensive code on the host natively and the communication portion in interpreted mode, the proposed ISS is able to speed up the simulation significantly while maintaining acceptable accuracy and support for multiprocessor simulation. The execution will jump back and forth between interpreted and compiled mode.

To achieve the specifications, the target code is processed by a code generation tool. The tool strips the computation code from the target source and generates the computation code for the host. Computation functions in the target source are then replaced by the system call stubs. The computation code and corresponding auxiliary functions are then complied on the host and linked with an interpreted ISS. The resulting host simulator loads the modified target binary to perform simulation.

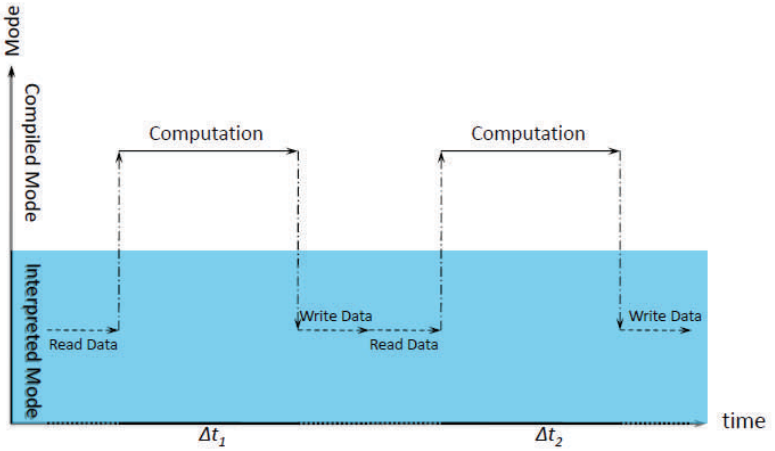

Figure 1: Execution Mode Switch with Proposed Hybrid Approach

Traditionally, in System Level Design context, the simulation is either cycle approximate (like in Transaction Level Model or Bus Function Model) or completely cycle-accurate and pin-accurate (like in Implementation Model). The former produces an inaccurate performance estimation, while the latter takes a substantial longer simulation time. In the proposed approach, by simulating the computation functions in cycle-

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Congrats Grads!

Project Profile: A Hybrid Instruction Set Simulator for System Level Design

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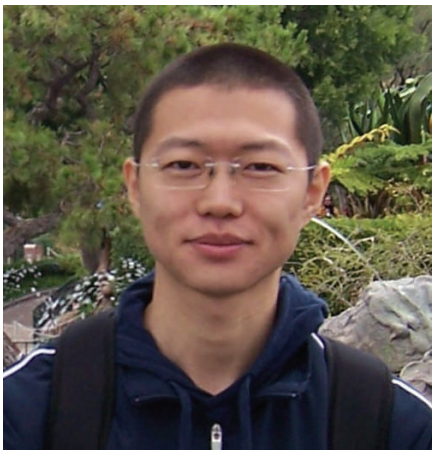
approximate mode and maintains cycle-accurate and pin-accurate simulation for communication between processors, we allow the user to explore the design space in between. In our proposed approach, the user is free to choose whether to run a function in interpreted mode or compiled mode. Thus, the user will have the freedom to make a trade off between simulation speed and simulation accuracy in their own design.



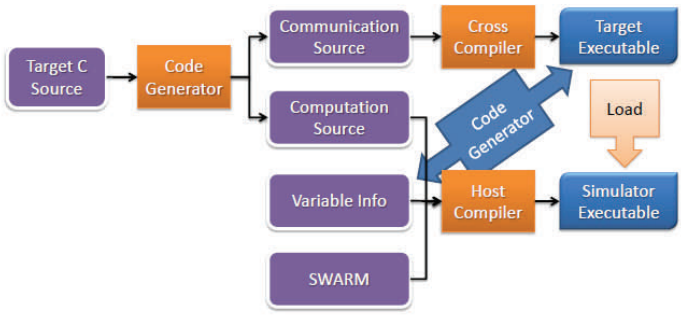


Figure 2: Work Flow Overview

Professors Eltawil and Kurdahi hosted a celebration for their graduating students: Amin Khajeh Djahromi, Hamid Eslami, Ali Reza Behbahani, Gaurav Patel, Avesta Sassan & Chitaranjan Sukumar
Congratulations to all 2010 CECS Graduates!

PUBLICATIONS

The following papers were published by CECS affiliates between April 2010 to June 2010 (and unreported papers from previous eNews).

Focus	Title, Author, Publication
Wireless Sensor Nodes	Chih-Hsiang Hsueh, Yi-Hsuan Tu, Yen-Chiu Li, and Pai H. Chou, **"EcoExec: An Interactive Execution Framework for Ultra Compact Wireless Sensor Nodes,"** (pending) in *Proceedings of the 7th IEEE Communications Society Conference on Sensor, Mesh and Ad Hoc Communications and Networks* (SECON 2010), Boston, MA, June 21-25, 2010. pp. 190-198.
Parallelizing Layout Engine of Firefox	Carmen Badea, Mohammad R. Haghighat, Alex Nicolau, and Alexander V. Veidenbaum, **"Towards Parallelizing the Layout Engine of Firefox,"** 2nd USENIX Workshop on Hot Topics in Parallelism 2010. Berkely, CA. June 14-15, 2010.
System Level Design	Yitao Guo and Rainer Doemer, **"A Hybrid Instruction Set Simulator for System Level Design,"** TR 10-06, June 11, 2010. Posted June 11, 2010.
Dual Triaxial-Accelerometer	Yi-Lung Tsai, Ting-Ting Tu, Hyeoungho Bae, and Pai H. Chou, **"A Dual Triaxial-Accelerometer Inertial Measurement Unit for Wearable Applications,"** in *Proc. International Conference on Body Sensor Networks* (BSN 2010), June 7-9, 2010, Singapore.
Wireless Embedded Sensing	Vahid Salmani and Pai H. Chou, **"Pushing the Throughput Limit of Low-Complexity Wireless Embedded Sensing Systems,"** to appear, in *Proc. 2010 IEEE International Conference on Sensor Networks, Ubiquitous, and Trustworthy Computing* (SUTC 2010), Newport Beach, CA USA, June 7-9, 2010.
Differential Power Analysis	K. Tanimura and N. Dutt, **"Exploration of Complementary Cells for Efficient Differential Power Analysis Attack Resistivity,"** in Proceedings of IEEE International Symposium on Hardware-Oriented Security and Trust, pp.117-120, Jun. 2010.
SleepServer - Reducing Energy Consumption	Yuvraj Agarwal, Stefan Savage and Rajesh Gupta, **"SleepServer: A Software-Only Approach for Reducing the Energy Consumption of PCs within Enterprise Environments,"** to appear in *Proceedings of the USENIX Annual Technical Conference (USENIX '10),* Boston, MA, June 2010.
Smart Buildings	Jan Kleissl and Yuvraj Agarwal, **"Cyber-Physical Energy Systems: Focus on Smart Buildings,"** to appear in *Proceedings of the ACM/EDAC/IEEE Design Automation Conference (DAC '10)*, June 2010.
SystemC	S. Sirowy, C. Huang, and F. Vahid. **"Online SystemC Emulation Acceleration,"** to appear in IEEE/ACM Design Automation Conference, June 2010. pdf
Leakage and Temperature Control	Houman Homayoun, Avesta Sasan, Aseem Gupta, Alex Veidenbaum, Fadi Kurdahi, and Nikil Dutt, **"Beyond Memory Cells for Leakage and Temperature Control in SRAM-based Units, the Peripheral Circuits Story,"** 2010 ACM International Conference on Computing Frontiers, CF-2010. Bertinoro, Italy. May 17-19, 2010.
Passive Imaging Receiver	Leland Gilreath, Vipul Jain, Hsin-Cheng Yao, Le Zheng, and Payam Heydari, **"A 94-GHz Passive Imaging Receiver using a Balanced LNA with Embedded Dicke Switch,"** *IEEE RFIC Symposium*, May 2010.
Frequency Tripler	Zhiming Chen and Payam Heydari, **"An 85-95.2 GHz Transformer-Based Injection-Locked Frequency Tripler in 65nm CMOS,"** *IEEE Int'l Microwave Symp.* (*IMS*), May 2010.
BiCMOS	Leland Gilreath, Vipul Jain, and Payam Heydari, **"A W-Band LNA 0.18-mm SiGe BiCMOS,"** *IEEE Int'l Symp. on Circuits and Systems* (*ISCAS*), May 2010.
Solar Energy Harvesting	Pai H. Chou and Sehwan Kim, **"Techniques for Maximizing Efficiency of Solar Energy Harvesting Systems (Invited Paper),"** to appear in *Proceedings of the Fifth Conference on Mobile Computing and Ubiquitous Networking* (ICMU 2010), Seattle, WA, April 26-28, 2010.

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CECS—*promoting creativity and pursuing discovery!*

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

CECS eNews
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Publications continued from page 5...

April 2010 to June 2010 (and unreported papers from previous eNews).

BiCMOS Leland Gilreath, Vipul Jain, Le Zheng, Hsin-Cheng Yao, and Payam Heydari, **"A Fully Integrated W-Band Passive Imaging Receiver IC in Silicon-Germanium BiCMOS Technology,"** *Proc. of SPIE Defense Security + Sensing*, April 2010.

Fault Tolerance Xiaobin Li and Jean-Luc Gaudiot, **"Tolerating Radiation-Induced Transient Faults in Modern Processors,"** International Journal of Parallel Programming (IJPP), Springer, Issue 2, pp. 85-116, April 2010

Sleep Transistor Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Fadi Kurdahi, and Alex Veidenbaum, **"Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks,"** 11th IEEE International Symposium on Quality Electronic Design, ISQED-2010. San Jose, CA. March 22-24, 2010.

Speed Control and Scheduling Ryo Sugihara and Rajesh K. Gupta, **"Speed Control and Scheduling of Data Mules in Sensor Networks,"** *ACM Transactions on Sensor Networks,* Accepted for publication.

3D Stacked Architectures A. Coskun, J. Ayala, D. Atienza, T. Simunic Rosing, **"Thermal Modeling and Management of Liquid Cooled 3D Stacked Architectures,"** invited for publication in a book; Editors: J. Becker, M. Johann and R. Reis; Springer Publishers, 2010.

Virtualized Environments G. Dhiman, G. Marchetti, T. Simunic Rosing, **"vGreen: A System for Energy Efficient Management of Virtualized Environments,"** under review in Special Issue of ACM TODAES, 2010.

Virtualized Environments G. Dhiman, G. Marchetti, T. Simunic Rosing, **"vGreen: A System for Energy Efficient Management of Virtualized Environments,"** under review in Special Issue of ACM TODAES, 2010.

Energy Management J. Recas, C. B, T. Simunic Rosing, D. Atienza, **"Energy management in SHM,"** to appear in JIMSS, 2010.