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CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

EDAA Lifetime Achievement Award 2010 goes to Daniel D. Gajski

- Adapted from EDAA Press Release

Highlights

Inside this Issue:

The Lifetime Achievement Award is given to individuals who made outstanding contributions to the state of the art in electronic design, automation and testing of electronic systems in their life. In order to be eligible, candidates must have made innovative contributions which had an impact on the way electronic systems are being designed.

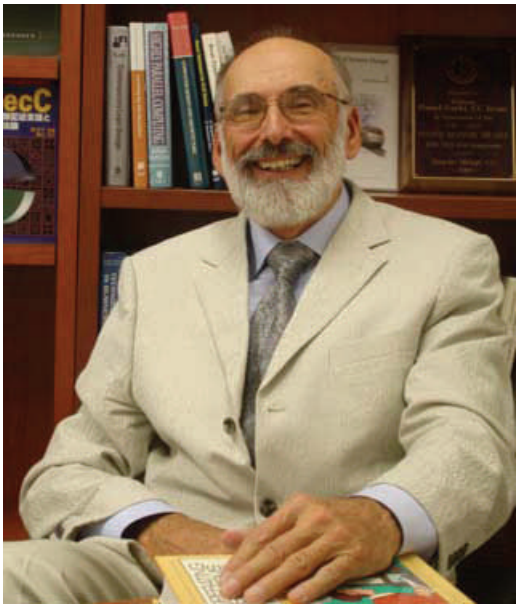
"We look forward to the continued success and world-wide recognition of Dr. Gajski and the Center for Embedded Computer Systems."

Susan Bryant
UCI Vice Chancellor for Research

UCI Vice Chancellor for Research Susan Bryant congratulates Professor Gajski for this outstanding achievement: "His establishment and leadership of the Center for Embedded Computer Systems as a campus Organized Research Unit reflects the world-class research being undertaken at UCI. We look forward to the continued success and world-wide recognition of Dr. Gajski and the Center for Embedded Computer Systems."

Past recipients have been Kurt Antreich (2003), Hugo De Man (2004), Jochen Jess (2005), Robert Brayton (2006), Tom W. Williams (2007), Ernest S. Kuh (2008) and Jan M. Rabaey (2009). The Award was presented at the plenary session of the 2010 DATE Conference, held 8-12 March in Dresden, Germany.

Daniel D. Gajski received the Dipl. Ing. and M.S. degrees in Electrical Engineering from the University of Zagreb, Croatia, and the Ph.D. degree in Computer and Information Sciences from the University of Pennsylvania, Philadelphia, in 1974. After 10 years of industrial experience in digital circuits, supercomputing, and VLSI design, he spent 10 years in academia with the Department of Computer Science at the University of Illinois, Urbana-Champaign. Presently, he is a Full Professor in the Department of Electrical Engineering and



Computer Science at the University of California, Irvine. He holds the Henry Samueli Endowed Chair in Computer System Design and is the Director of the Center for Embedded Computer Systems at UCI.

Daniel Gajski has made many fundamental contributions to areas spanning from electronic design automation to embedded systems. He is considered among the

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Book Review

Embedded System Design: Modeling, Synthesis and Verification Book Review

- excerpt by Grant Martin

March/April 2010 IEEE Design & Test of Computers

Embedded System Design: Modeling, Synthesis and Verification, by Daniel D. Gajski, Samar Abdi, Andreas Gerstlauer, and Gunar Schirner, has received many positive reviews since its release earlier last year. Recently, Grant Martin of Tensilica published a review in **IEEE Design & Test of Computers** on this book. The following is an excerpt from the article. The complete review can be found in the March/April 2010 release of IEEE Design & Test of Computers:

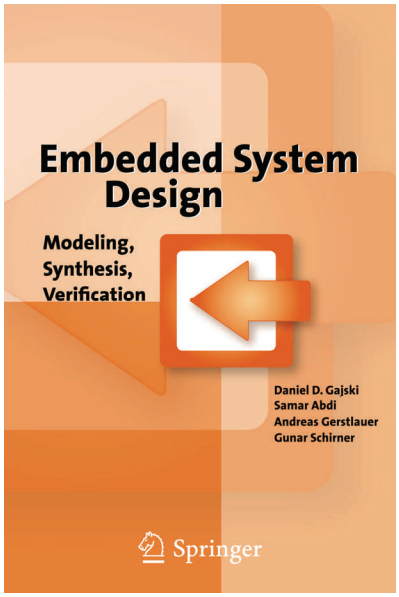
One of the most active researchers, teachers, and leaders in system-level design for many years is Daniel Gajski of the University of California, Irvine. Together with students (many who have become academic leaders and influential parts of the industry in their own right), colleagues, and partners, he has explored all parts of system-level design, both widely and deeply. Some of the concepts and tools developed during these efforts have formed an essential part of spinout companies, and others have been adopted by major users in the design community. Some of Dan Gajski's concepts, such as the Gajski Y-chart from 1983, have become standard tools with which to describe design methodologies.

So when it came time for Gajski and his colleagues to write about system-level design methodologies, in their new book Embedded System Design: Modeling, Synthesis and Verification, they had a wealth of material to work with. Indeed, figuring out what to say in a book on system design must have been a challenge, but one to which the authors have risen admirably.

This book deals with the need for both breadth and depth in describing system-level design by its structure. Two general chapters—an introductory one, and one on system design methodologies—and a concluding chapter on embedded-design practice bracket five more detailed chapters that cover the major topics of embedded-system design: modeling, system synthesis, software synthesis, hardware synthesis, and verification. These detailed chapters cover their topics in two ways: descriptions of the methods and technologies that address each topic, illustrated with examples drawn from the research of the authors and the authors' colleagues.

…

This book is a great introduction to embedded systems design methodologies and tools, both those in use and those yet to come. It is a good summary of the pioneering work of Gajski and his colleagues in system-level design, highlighting progress made and directions for future developments. It is also a good learning vehicle for those who wish to understand this area and apply it to their own work. Students in embedded design should find it a good introduction and survey. Even more important, it will be useful to those in industry wanting a better overview of what is possible. I heartily recommend it.



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continued from front page...

founding fathers of the push in electronic design methods towards higher levels of abstractions and their relationship to system architectures and has been a leader in establishing the fields of Silicon Compilation, High-Level Synthesis, and System-Level Design.

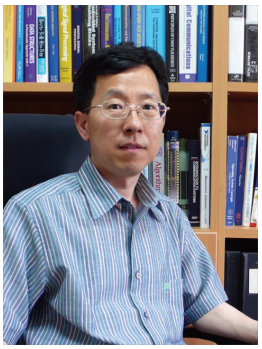
Daniel Gajski has published over 250 journal and conference papers, has edited, authored and co-authored a total of seven books and numerous book chapters, and has received several best-paper awards and nominations. He has been named an IEEE Fellow for contributions to VLSI design, system-level design methodologies and CAD tools and also has been presented with an honorary doctorate from the University of Oldenburg, Germany, in 2006 in recognition of his contributions in the areas of embedded systems and design science.

More information and electronic version of this Press Release available at: http://www.edaa.com/

VISITOR & STUDENT PROFILES

Visitor Profile: Dr. Jong Tae Kim

- CECS Staff



Professor Kim is taking his sabbatical year here at CECS as a visiting scholar, hosted by Professor Fadi Kurdahi. He is an alumnus of UCI. He received the MS and PhD degrees in electrical and computer engineering at the University of California, Irvine, in 1987 and 1992, respectively. He is a professor at the School of Information and Communication Engineering, Sungkyunkwan university, Korea, where he has been since 1995. He was with the Aerospace Corporation in Elsegundo, California, as a member of technical staff from 1991 to 1993.

His research expertise is in system-on-a-chip design, embedded systems, and computer architecture. Currently he is engaged in several research projects including a design of digital predistortion VLSI chip, an embedded system design for FDG synthesis microreactor, and a soft-error mitigation method for high speed memory.

Student Profile: Luis Bathen

- By Luis Bathen

I am a Ph.D. Candidate working under Professor Nikil Dutt. I am one of many UCI products, by that I mean, I started me college career at UCI and plan on finishing it here.
I started working on reconfigurable architectures back when I was a sophomore during a summer program funded by the UCI CAMP program. As an undergraduate I was funded by CAMP/McNair and UROP. As a graduate student I have been blessed with many other different opportunities (Intel/AGEP, UCI/Eugene Cota-Robles, UC-Mexus, UCI/Federal Cyber Service (SFS)). Of course, like all graduate students I continue my search for further funding.

I have worked for Intel and IBM during my summers dating back to 2004. I have gained plenty of industry exposure and worked under a series of different environments in industry, ranging from research oriented to pure application development. As an intern I have developed technologies that have made it to the front lines (actual GA products), as well as filed for IP disclosures and published several papers. These experiences have helped me widen my area of expertise.

The increasing demand for low power, high performance, reliable, and secure multimedia embedded systems has motivated the need for effective solutions to satisfy application bandwidth and latency requirements under a tight power budget. As technology scales and new techniques such as aggressive voltage scaling are utilized in the design of embedded systems it is imperative that applications are optimized to take full advantage of the underlying resources and meet power, performance, and reliability requirements. Moreover, as these devices become more complex and their connectivity to the world-wide-web is constantly increasing their vulnerabilities to malicious software increase.

In order to address these issues I am currently working on CAM, a framework for constraint-aware application mapping on multiprocessor embedded systems. Figure 1 shows CAM's block diagram. Given a series of constraints, a mixture of power, performance, security, reliability, and temperature, CAM will take an application and try to map it onto the desired embedded system. Currently CAM supports a wide spectrum of platforms, ranging from simple chip-multiprocessors, to dedicated hardware models. CAM consists of four main parts. The first is the front end which extracts all the necessary information from the application and generates the input models to our framework. The second part is the transformations, analysis and policy making engine which is responsible for applying different source code level optimizations to increase the application's parallelism and determine data reuse opportunities as well as generate an augmented task graph which was been annotated with different application information which will be used by our scheduler. Our policy making engine takes an application and generates policies to guarantee safe execution of software which are then enforced by the target platform. The next part is the mapping and scheduling heuristics which will take the augmented task graph and given the set of constraints and policies, it will optimize the scheduling and mapping for the given platform. Finally, the back end consists of a model generation which will take the application's code and generate performance models which are then plugged into CAM's SystemC modeling engine.

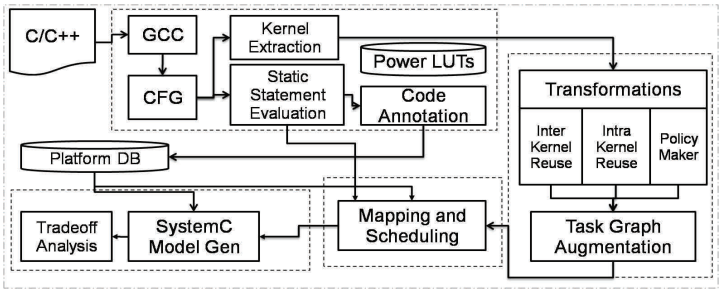


Figure 1. CAM Block Diagram

PUBLICATIONS

The following papers were published by CECS affiliates between January 2010 to March 2010.

Focus	Title, Author, Publication
Power Optimization	Houman Homayoun, Shahin Golshan, Eli Bozorgzadeh, Fadi Kurdahi, Alex Veidenbaum, "Post-Synthesis Sleep Transistor Insertion for Leakage Power Optimization in Clock Tree Networks," 11th IEEE International Symposium on Quality Electronic Design (ISQED), March 22-24, 2010.
Sensor Networks	Masanobu Shinozuka, Sehwan Kim, Pai H. Chou, Lu Fei, and Hong Rok Kim, "A Sensor Network for Real-Time Damage Location and Assessment," Nondestructive Characterization for Composite Materials, Aerospace Engineering, Civil Infrastructure, and Homeland Security IV, March 9, 2010. San Diego, CA USA.
Distributed Ultrasonic Sensors	Jiming Liu, Michael B. Dillencourt, Lubomir F. Bic, Daniel Gillen, and Arthur D. Lander, "Gas-Leak Localization Using Distributed Ultrasonic Sensors," Proc. SPIE, Vol. 7293, 72930Z, San Diego, March 2009 .
Aerospace Engineering	Masanobu Shinozuka, Sehwan Kim, Pai H. Chou, Lu Fei, and Hong Rok Kim, "A Sensor Network for Real-Time Damage Location and Assessment," to appear, in *Nondestructive Characterization for Composite Materials, Aerospace Engineering, Civil Infrastructure, and Homeland Security IV*, March 9, 2010. San Diego, CA USA
Server-side Coprocessor	C. Huang and F. Vahid. "Server-Side Coprocessor Updating for Mobile Devices with FPGAs ACM," International Symposium on FPGAs, February 2010.
Network-on-Chip Architecture	Chifeng Wang, Wen-Hsiang Hu, Seung Eun Lee and Nader Bagherzadeh, "Area and Power-efficient Innovative Network-on-Chip Architecture," at the 18th Euromicro International Conference on Parallel, Distributed and Network-Based Computing (PDP 2010), Pisa, Italy. February 2010.
Automated Power Control	Hyeoungho Bae, Yu-Chih Huang, Owen Yang, Pai H. Chou, and Bernard Choi, "Automated Power Control for Mobile Laser Speckle Imaging System,"' IEEE Embedded Systems Letters, Vol. 1, No. 3, October 2009, pages 65-68, (version published February 2010).
Wireless Sensing System	Chien-Ying Chen, Yu-Ting Chen, Yi-Hsuan Tu, Shun-Yao Yang, and Pai H. Chou, "EcoSpire: An Application Development Kit for an Ultra-Compact Wireless Sensing System," IEEE Embedded Systems Letters, Vol. 1, Nov. 3, October 2009, pages 73-76, (version published February 2010).
Power and Thermal Management	Houman Homayoun, Aseem Gupta, Alex Veidenbaum, Fadi J. Kurdahi, Nikil Dutt, "RELOCATE: Register File Local Access Pattern Redistribution Mechanism for Power and Thermal Management in Out-of-Order Embedded Processor," 5th International Conference of High Performance Embedded Architectures and Compilers, (HiPEAC), January 25-27, 2010.
W-Band Detector	Le Zheng, Leland Gilreath, Vipul Jain, and Payam Heydari, "Design and Analysis of a W-Band Detector in 0.18-mm SiGe BiCMOS," IEEE Silicon Monolithic Integrated Circuits in RF Systems, January 2010.
Periodic ConcurrenC Models	W. Chen, R. Doemer, "*A Fast Heuristic Scheduling Algorithm for Periodic ConcurrenC Models*," Proceedings of the Asia and South Pacific Design Automation Conference 2010, Taipei, Taiwan, January 2010.

CECS—*promoting creativity and pursuing discovery!*

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Center for Embedded Computer Systems
2010 Anteater Instruction & Research Building
University of California, Irvine
Email: enews@cecs.uci.edu