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CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights

- Tony Givargis's Best Paper Award
- CECS renews contract with JAXA
- Sudeep at E3
- SER Tool Communication and Nanomachines

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DAC Best Paper Award Goes to CECS' Tony Givargis

CECS affiliate, Tony Givargis, received The ACM Transactions on Design Automation of Electronic Systems 2006 Best Paper Award at this year's Design Automation Conference. His paper is titled "Zero Cost Indexing for Improved Processor Cache Performance." The increasing use of microprocessor cores in embedded systems as well as mobile and portable devices creates an opportunity for customizing the cache subsystem for improved performance. In traditional cache design,

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JAXA and CECS Renew Contract

On May 16 and May 17, 2006, CECS was visited by representatives from the Japanese Aerospace Exploration Agency (JAXA), InterDesign Technologies, Inc. (IDT) and HIREC to discuss successful completion and possible continuation of the SER project.

Two years ago, CECS teamed up with the Japanese Aerospace Exploration Agency and InterDesign Technologies to develop the Specify-Explore-Refine (SER) tool set as part of a JAXA project to establish an environment for automated and computer-assisted design of space electronic applications and equipment. CECS is pleased to announce the successful completion of this two-year project. The SER tools have been successfully delivered and are currently being evaluated by and introduced to users in Japan. In addition, during their visit representatives from CECS, JAXA, IDT and HIREC agreed to renew and extend the partnership for another year in order to develop additional database models of space electronic components to be used in SER.

SER is an electronic system-level (ESL) design tool that performs interactive architecture exploration and synthesis of bus communication networks. "SER facilitates rapid and early exploration of the system-level design space with easy interactive and application-driven design of the platform", Jerry Peng, Project Scientist in charge of architecture exploration said. Dongwan Shin, Project Scientist and developer of SER's communication synthesis engine adds, "With its automatic generation of bus interfaces and bus drivers, SER frees the designer from the tedious and error-prone process of implementing application communication mechanisms".

"Overall, the successful project completion and contract renewal proves that our approach is valid and viable in a real world, commercial setting," Andreas Gerstlauer, Assistant Researcher responsible for SER project coordi-

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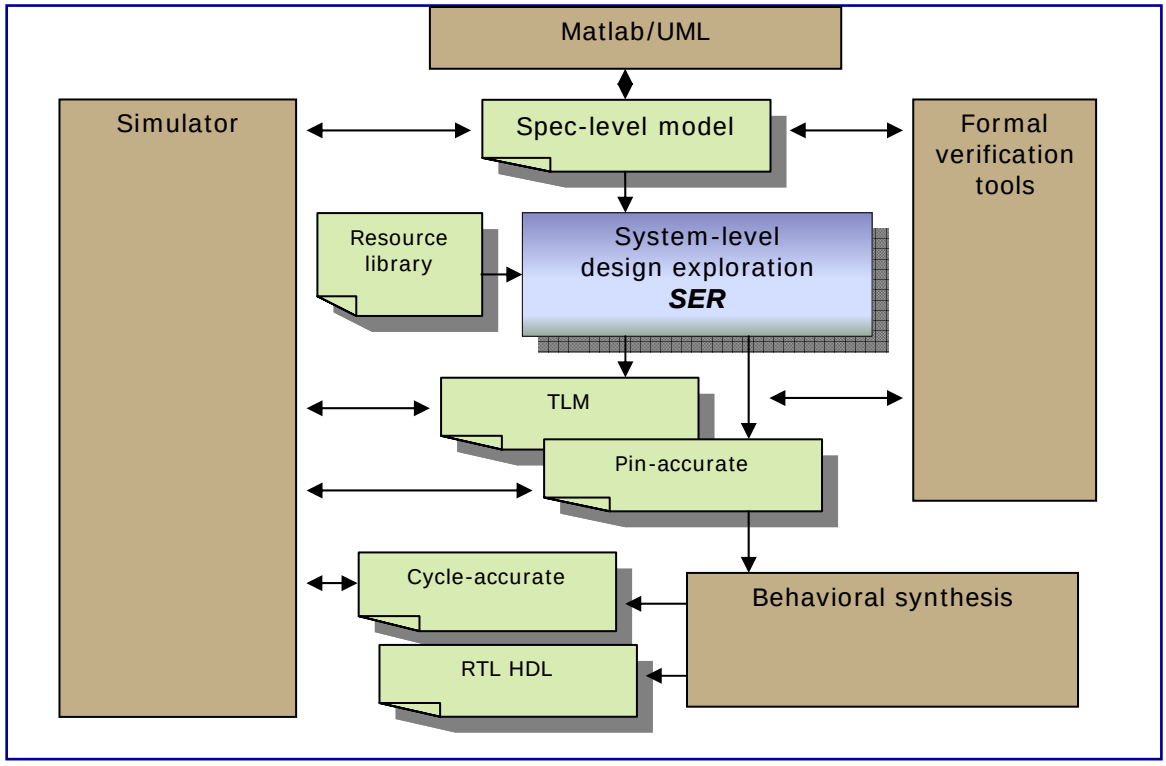
SER Tool Commercialization

CECS is pleased to announce the commercial availability of the Specify-Explore-Refine (SER) tools. SER has been developed by the Center for Embedded Computer Systems with the support of the Japanese Aerospace Exploration Agency (JAXA), and it has been licensed to InterDesign Technologies, Inc. (IDT), Japan for sale and commercialization. The SER tools were introduced to the market and successfully demonstrated at the InterDesign booth at this year's 43rd Design Automation Conference (DAC) in San Francisco.

SER is based on concepts and solutions from the System-on-Chip Environment (SCE, see http://www.cecs.uci.edu/~cad/sce.html) project, originally developed here at CECS by a group of researchers including Dr. Andreas Gerstlauer, Dr. Junyu Peng and Dr. Dongwan Shin under the leadership of Prof. Daniel Gajski. SER is a derivative of SCE and as such it incorporates experience and results of more than 10 years of research and development in system-level design.



SER provides an environment for true top-down electronic system-level (ESL) design following a consistent and powerful methodology and tool chain from a top-level specification model all the way down to RTL design. SER accepts architecture-independent, algorithmic specification models written in C and it enables interactive and step-wise system-level design space exploration with HW/SW partitioning, network topology design, bus protocol selection and bus interface synthesis. Given the application specification and design decisions, SER automatically generates transaction level platform models (TLMs) which enable performance analysis and software testing within the virtual platform simulator. In addition, SER generates C model descriptions for backend behavioral synthesis tools down to RTL and implementation.

SER will be available from, sold and supported by InterDesign Technologies, Inc. (http://www.interdesigntech.co.jp).

The following were published by CECS faculty affiliates from October 2005 to September 2006

Focus	Titles, Author, Publication
MPSoCs	"A Framework for Memory and Communication Architecture Co-synthesis in MPSoCs," S. Pasricha and N. Dutt, TR 06-03, February 2006.
Power vs Quality Trade-offs	"Using Annotations to Facilitate Power vs Quality Trade-offs in Streaming Applications," R. Cornea, A. Nicolau, N. Dutt, TR 06-02, March 2006.
SoC Communication	"Necessary and Sufficient Functionality and Parameters for SoC Communication," A. Gerstlauer, G. Schirner, D. Shin, and J. Peng, TR 06-01, May 2006.

Visitor Profile

Qiang Zhu

Qiang Zhu was born in Shanghai, China. He obtained a B.C. degree in Computer Science from Osaka University in 1998. He obtained his M.C. degree in Information Science from Nara Institute of Science and Technology in 2000. He joined Fujitsu Laboratories as a research engineer in 2000. His work at Fujitsu involves evaluation of design and verification methodologies for System-on-a-Chip (SoC) development. He has been working in System-Level design using Unified Modeling Language (UML) and SystemC. He focuses on the SoC verification techniques using format method and automatic test generation.

He has been a visitor at UCI since August 2005 on a sabbatical from his company Fujitsu. He is working at CECS Laboratory with Professor Nikil Dutt and is investigating contemporary issues with System-Level verification, like specification validation and test generation techniques for SoC design. Qiang is very thankful to the faculty, staff and students at CECS for their help and constructive ideas.

Like all good things, Qiang's stint at UCI is about to end – he will be returning back to Japan in August. He is delighted to say that his stay at UCI was fulfilling and enriching in all respects and he would look forward to visiting UCI again.

Student Profile

Sudeep Pasricha :: Cont'd from page 5

violations early in the design flow, thus drastically cutting down design time of modern embedded designs. He recently presented an approach for the automated synthesis of bus matrix type communication architectures (*BMSYN*) for next generation MPSoC designs. Most recently, he proposed a novel co-synthesis framework (*COSMECA*) to couple the synthesis of memory and communication architectures, to reduce system cost and die area for MPSoC designs.

Sudeep has an notable publication record, and has received the Best Paper Award at the Asia and South Pacific Design Automation Conference in 2006 for his paper titled *"Constraint-Driven Bus Matrix Synthesis for MPSoC"*; and a Best Paper Award nomination at the Design Automation Conference in 2005 for his research paper titled "*Floorplan-aware Automated Synthesis of Bus-based Communication Architectures"*. He is the recipient of the CPCC (Center for Pervasive Communication and Computing) research fellowships in 2005 and 2006, and is also affiliated with the Semiconductor Research Consortium (SRC). His thesis topic is titled *"Modeling, Exploration and Synthesis of Communication Architectures for Multi-processor System-on-Chips"*. His research interests include MPSoC Communication Architecture Exploration, System Level Modeling Languages and Methodologies and CAD for Embedded Systems.

CECS Renews Contract with JAXA :: Cont'd from Front Page

nation concludes. CECS director Dr. Gajski agrees, "This contract confirms and establishes CECS as a leading research institution worldwide with a proven track record of successful technology transfers to industry."

Givargis Gets Best Paper Award :: Cont'd from Front Page

the index portion of the memory address bus consists of the K least significant bits. However, in devices where the application set is known and characterized there is an opportunity to improve cache performance be choosing a near-optimal set of bits used as index into the cache. This technique does not add any overhead in terms of area or delay. In this article, we present an efficient heuristic algorithm for selecting K index bits for improved cache performance. We show the feasibility of our algorithm by applying it to a large number of embedded system applications as well as the integer SPEC CPU 2000 benchmarks. On average, we show a 30% performance improvement when using our technique.

Project Profile

Nano Scale Communication Among Biological Nanomachines

The molecular communication project explores the possibility of using communication mechanisms that biological entities (such as cells) use as a solution for communication between nanomachines (i.e., artificial or biological nano-scale devices that perform simple computation, sensing or actuation).

Figure 1

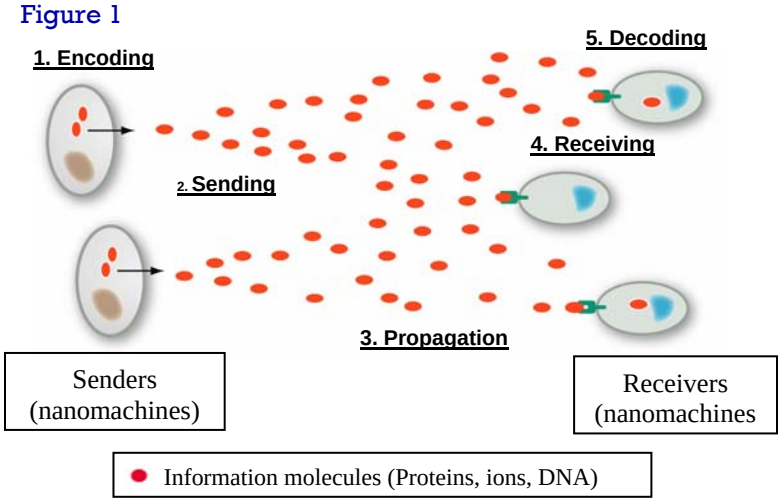


Figure 2

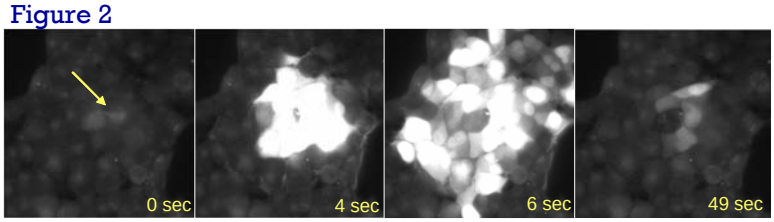
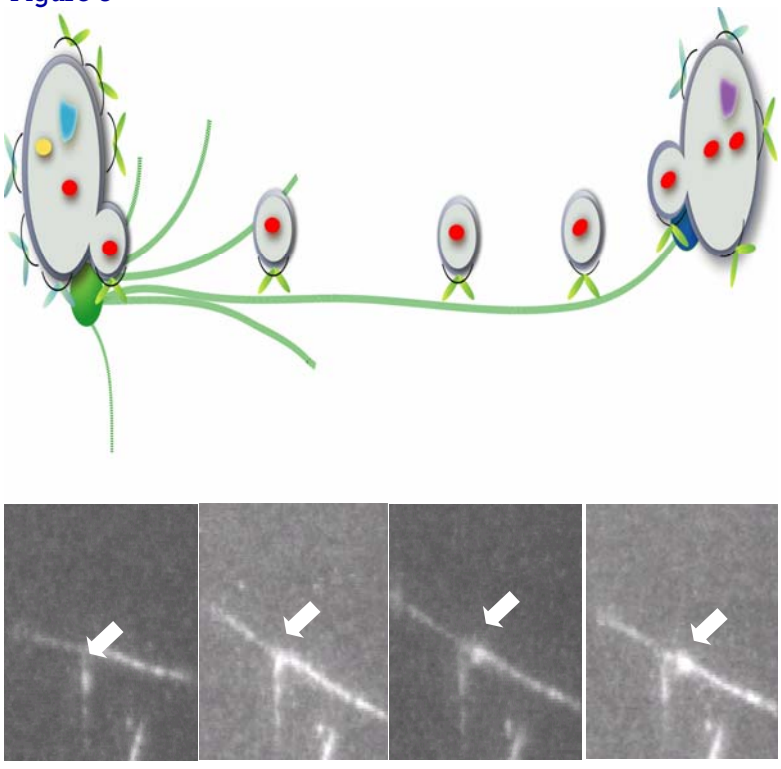


Figure 3



The molecular communication may benefit applications that require communications between nanomachines and logic operations by nanomachines. Such applications include biomedical applications, emerging molecular computing, and nano-scale manufacturing through self-organizing nanomachines. For example, nanomachines embedded in a human body may monitor health and treat disease by directly interacting with the cells and molecules of the human body. Such nanomachines sense the molecular-level status of the body, communicate among each other to coordinate, and use their logic to select appropriate responses to the molecular-level status of the body.

The molecular communication project has developed a basic architecture to describe the system (Figure 1). Key architecture components include sender and receiver nanomachines (such as cells), information molecules (to encode information on) carrier molecules (such as motors to transport information molecules), and the environment that these operate in.

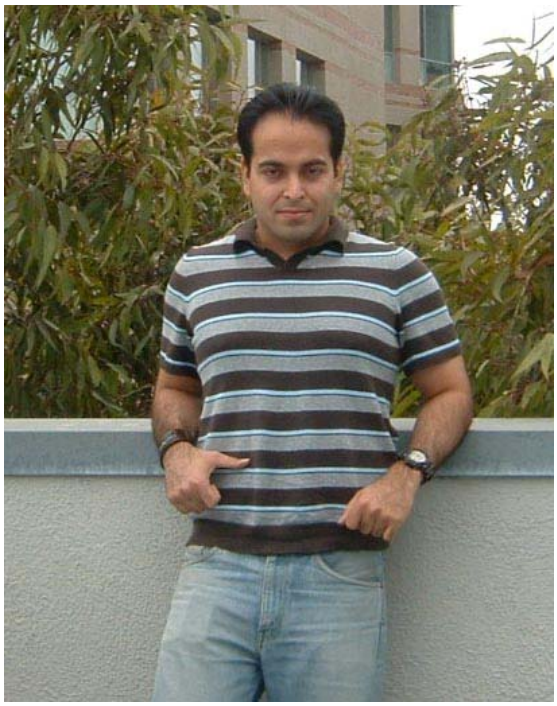
Currently, the project investigates empirically and through simulations two molecular communication systems, one that uses mechanisms from calcium signaling between cells and another that uses mechanisms from intracellular signaling using molecular motors. In the first system using the calcium signaling mechanism, an information source stimulates cells which in turn use calcium signaling pathways to propagate the signal to receivers (Figure 2). In the second system using the intracellular signaling mechanism, the sender releases molecules that bind to molecular motors which walk along rails of proteins to carry information to receivers (Figure 3).

Dr. Suda and his collaborators have filed two patents on molecular communication and are in the process of filing the third patent.

Profiles

Student Profile

Sudeep Pasricha



CECS is pleased to profile Sudeep Pasricha as an Outstanding Graduate Student. He was born in New Delhi, India in 1978. He received a B.E in Electronics and Communications Engineering from Delhi Institute of Technology, Delhi, India in 2000. Following graduation, he was employed by STMicroelectronics as a member of the Embedded Systems Team at the Center for Research and Development (CR&D) for two years, till 2002. He worked at the Noida (India) and Crolles (France) R&D centers to create a development and validation framework for fast processor/memory design space exploration. He also worked in collaboration with the System Architecture Group to spearhead the development of a Transaction Level Modeling (TLM) methodology and models for SoC development, verification and eSW development.

In Fall 2002, Sudeep joined Prof Nikil Dutt's ACES (Architectures and Compilers for Embedded Systems) group at the Center for Embedded Computer Systems. Since the summer of 2003, his primary research focus has been on efficient modeling, exploration and synthesis of communication architectures for multi-processor system-on-chip (MPSoC) designs, under the supervision of Prof Nikil Dutt. He has made significant contributions in this research area, such as the development of a fast modeling abstraction (*CCATB*) for speeding up the modeling effort and simulation speed of SoC designs at the system level. He has proposed the *FABSYN* methodology for the physical implementation-aware automated synthesis of hierarchical bus-based communication architectures; *FABSYN* enables the detection and elimination of bus-cycle timing

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Visitor Profile

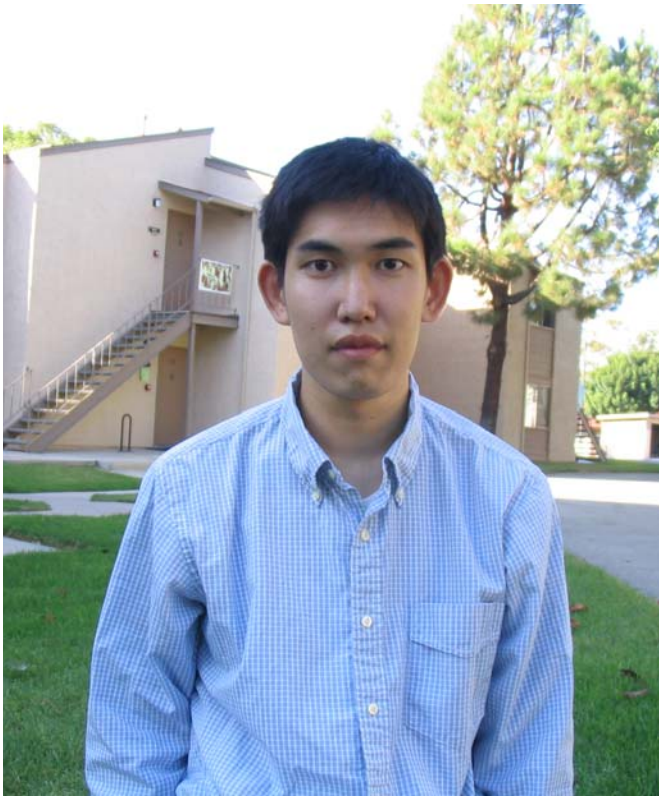
Yuji Ishikawa

Yuji Ishikawa is visiting CECS from the EE department at the University of Tokyo, Japan. Yuji is working with Professor Gajski's team on the IDE (Integrated Design Environment) for VLSI design, a project the team has been developing and working on in conjunction with JAXA (Japan Aerospace Exploration Agency) for several years; Yuji is here to learn how to improve the IDE and use the system-level design environment.

Yuji is a graduate student of the electric engineering department at the University of Tokyo and has been a member of the Fujita Laboratory since his last undergraduate year at the university. He has been researching synthesizing protocol transducers that can be applied to the existing module of the VLSI. This research will aid in matching the interface-protocol of modules to other modules when one wants to reuse the existing design; Yuji is working on the method of capturing the specification of the target protocol.

"I think I got much more experience than I had expected from my one week stay [at UCI]," Yuji says. He noticed that students and researchers at UCI were interested in a broad range of research topics aside from their own and that they discussed these topics freely and often.

Yuji enjoyed his time at UCI and found the people at CECS to be kind and attentive to his questions. "I think the experience in UCI has grown me up."



PUBLICATIONS

The following were published by CECS faculty affiliates from October 2005 to September 2006

Focus	Titles, Author, Publication
Model Transformations	"Verification of System Level Model Transformations," S. Abdi, D. Gajski, *International Journal of Parallel Programming*, February 2006.
Pipelined Datapaths	"Generic Architecture Description for Re-targetable Compilation and Synthesis of Application-Specific Pipelined Datapaths," B. Gorjiara, M. Reshadi, D. D. Gajski, *IEEE International Conference on Computer Design* (ICCD)October 2006.
Duplex AMA-TMS Transducer	"Design and Implementation of a Duplex AMBA-TMS Transducer," H. Cho, S. Abdi, and D. D. Gajski, *Asia and South Pacific Design Automation Conference* (ASP-DAC), Yokohama, Japan, January 2006.
System Level Design	"New Strategies for System Level Design," D. D. Gajski, *International Symposium on VLSI Design, Automation, and Test*, Hsiuchu, Taiwan, April 2006, pp. 1-5.
Algorithm for Data Path Optimization	"A Graph Based Algorithm for Data Path Optimization in Custom Processors," J. Trajkovic, M. Reshadi, B. Gorjiara, and D. D. Gajski, *Euromicro Conference on Digital System Design*, Dubrovnik, Croatia, September 2006.
Custom Processors	"Automatic Architecture Selection for Custom Processors," J. Trajkovic and D. D. Gajski, Proceedings of *SRC Student Symposium*, October 2006.
Cycle Accurate Stimulators	"Generic Processor Modeling for Automatically Generating Very Fast Cycle-Accurate Simlutors," M. Reshadi, B. Gorjiara, N. Dutt, to appear in IEEE Transactions on Computer Aided Design (TCAD).
Instruction-Set Architecture Simulation	"A Retargetable Framework for Instruction-Set Architecture Simulation," M. Reshadi, P. Mishra, N. Dutt, ACM Transactions on Embedded Computing Systems (TECS), v 5 n2, May 2006.
Level Modeling	"Transaction Level Modeling of Computation," R. Doemer, TR 06-11, August 2006.
System-on-Chip	"System-On-Chip Component Models," A. Gerstlauer, G. Schirner, D. Shin, J. Peng, R. Doemer, D. Gajski, TR 06-10, May 2006.
Stream Annotations for Energy Trade-offs	"Stream Annotations for Energy Trade-offs in a Video Decoder for Multimedia Applications," R. Cornea, A. Nicolau, N. Dutt, TR 06-09, May 2006.
Debugging and Tracing System Level Designs	"Efficient Debugging and Tracing of System Level Designs," E. Johnson, A. Gerstlauer, R. Doemer, TR 06-08, May 2006.
ARM Processor	"Modeling, Simulation and Synthesis in an Embedded Software Design Flow for an ARM Processor," G. Schirner, G. Sachdeva, A. Gerstalauer, R. Doemer, TR 06-06, April 2006.
Xilinx Multimedia Board	"Processor Customization on a Xilinx Multimedia Board," P. Biswas, S. Banerjee, and N. Dutt, TR 06-04, March 2006.

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Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Gaming Nirvana at E3 :: Sudeep Pasricha

I recently had the opportunity to visit the Electronic Entertainment Expo (E3) in Los Angeles. It is the biggest annual event for the electronic entertainment industry to come together under one roof and display its wares in a chaotic, neon mass of exhibits. Think of the Design Automation Conference (DAC) conference and multiply its scale by about five times. Then on top of it add a plethora of light, sound and laser displays, wildly imaginative company booths giving out gaming freebies, giant video screens and 360 degree theaters showing in-game videos and trailers, people dressed up as characters from your favorite games walking around and posing for pics, eagerly awaited media events from leading console makers such as Sony, Microsoft and Nintendo … and then you might possibly be able to grasp how huge this event was. E3 is undoubtedly every gamer's dream come true.

Aside from hundreds of new games at display, several of which were based on popular TV and movie franchises (Desperate Housewives, CSI, Pirates of the Caribean, Superman), the leading console makers disclosed eagerly awaited information about their next generation consoles. Nintendo displayed and allowed hands-on previews of its soon to be released console 'Nintendo Wii' which features a motion sensitive controller. Imagine playing tennis by actually moving your hands every time you hit a shot! And Sony displayed the next generation of its wildly popular Playstation 2 console, 'Sony PS3', which is nothing short of a technological marvel – a multi-core Cell processor engine jointly developed by IBM, Sony and Toshiba; a high-end graphics processor co-developed with NVIDIA and SECI, high bandwidth XDR memory from RAMBUS, a BD-ROM (Blu-Ray Disc ROM) that allows a 54 GB maximum storage capacity and a wireless Bluetooth-based controller with inbuilt tilting accelerometer. Phew! Not to be outdone, Microsoft, which released its newest console 'Xbox 360' a few months ago (and is the PS3's biggest competitor), had an enormous booth that allowed people to play some of its soon-to-be-released games.