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# CECS eNEWS

*Center for Embedded Computer Systems, University of California, Irvine*

**Highlights**

- Heydari wins Darlington Award at 42nd DAC
- Bob Larsen's Retirement
- Trip into the Jungle

**Inside this Issue:**



## CECS at Design Automation Conference '05

*** * * 3 papers presented * * ***

The latest in design methodologies and Electronic Design Automation (EDA) tool developments are presented each year at the Design Automation Conference. The four day event, held in 2005 at the Anaheim Convention Center in Anaheim, CA from June 13-17, showcases research done by companies and universities world-wide for the advancement of technology related to electricity, silicon solutions, and the development of new tools for designing and producing electronic systems. Research affiliates and graduate students from the Center of Embedded Computer Systems (CECS) at the University of California, Irvine (UCI) presented three technical papers and received two major awards at the 42nd Design Automation Conference.

**Papers**

The following papers were presented by CECS research affiliates (with the cited pages from the conference proceedings). They discuss dynamic slack reclamation techniques, tools and methods to support design space exploration and specialization of embedded computing systems, floorplan-aware synthesis of communication architectures, and new ideas for energy management in a wide variety of scenarios, respectively.

- *Dynamic Slack Reclamation with Procrastination Scheduling in Real-Time Embedded Systems*, Ravindara Jejurikar, pp. 111-116
- *Physically-Aware HW-SW Partitioning for Reconfigurable Architectures with Partial Dynamic Reconfiguration*, Sudarshan Banerjee, Elaheh Bozorgzadeh, and Nikil Dutt, pp. 335-340
- *Floorplan-Aware Automated Synthesis of Bus-based Communication Architectures,* Sudeep Pasricha, Nikil Dutt, and Eleheh Bozorgzadeh, pp. 565-570


- *Application/Architecture Power Co-Optimization for Embedded Systems Powered by Renewable Sources,* Dexin Li and Pai H. Chou, pp.618-623

**Awards**

- IEEE Circuits & Systems Society 2005 Darlington Award

**Payam Heydari** for his *Analysis of the PLL Jitter Due to Power/Ground and Substrate Noise*

- 2005 IEEE Fellows

**Fadi Joseph Kurdahi** for his contributions to design automation of digital systems and to reconfigurable computing.

**Committees**

- Technical Program Committee

**Professor Pai Chou**

## CECS Grads Awarded Nicholas Fellowship

The Henry T. Nicholas, III Research Fellowship has been awarded to CECS graduate students Keun-sik No and Pramod Chandraiah for the 2005-2006 academic year. The prize is administered by the California Institute for Telecommunications and Information Technology (Cal-(IT)2) and is funded by The Nicholas Foundation, an organization committed to enhancing quality of life by providing grants to non-profit organizations. This

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## Grad Students Awarded Fellowship

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is the first year this fellowship will be available to UCI students and Cal-(IT)2 hopes that it will promote collaboration among UCI's faculty as well as recognize projects with potential for leading to further discoveries.

Keun-sik No received the Fellowship award for his research on the Mini-FDPM, which he began working on when he arrived at UC Irvine two years ago. He had studied microwave tomography at Sungkyunkwan University in Seoul, Korea as an undergraduate and is now applying his knowledge to developing a handheld, non-invasive breast cancer detector based on frequency domain photon migration that will operate using the principles of microwave tomography. The Mini-FDPM handheld device emits broadband-modulated near-infrared light into a patient's tissue and measures its reflection to determine the relative concentration of contents, including water, hemoglobin and fat. No's research aims to improve the frequency range and speed of the Mini-FDPM while working with CAD researchers as a case study for a new generation tool design. The miniaturization of the breast cancer detector will encourage regular testing for breast cancer due to its non-invasive nature, and the Mini-FDPM's higher frequency will allow for better resolution and accuracy due to a shorter wavelength. This will help detect cancer in shallower tissue where current reference design has not had much success. No is thankful for the fellowship because, though the National Cancer Society and other similar organizations have pitched in for funding the project, the Nicholas Fellowship is a stable grant that covers not only funding for research but No's tuition and payroll as well.

Pramod Chandraiah is the second Nicholas Fellow. The fellowship grant will aid his research on creating and optimizing the specification model for System-on-Chip design. Though there has been much research on the tools required to synthesize the SoC, not much time has been spent on the development of specification itself; Chandraiah's research will aid the designer in synthesizing SoC with more speed and efficiency, which will have a remarkable impact on the cost and quality of the resulting system implementation. The funding from the Nicholas Grant will allow Chandraiah to expand upon the preliminary work he and his advisor, Professor Rainer Domer, have been doing, and will also allow Chandraiah to develop prototype tools for specification generation, automated re-coding, and source code optimization. Chandraiah completed his undergraduate studies at S.J. College of Engineering in Mysore, India and went on to design firmware for the Broadcom Corporation in Bangalore, India; he received his Master at UCI in the Winter of 2005 and is now pursuing his Ph.D. in the EECS department at UCI.

## Visitor Profile

### Dr. Dirk Jansen

Dr. Dirk Jansen hails from the University of Offenburg in the south of Germany and has been on sabbatical at UC Irvine since 18 March 2005 researching System-on-Chip design and production. His research will aid in building more efficient systems that can be housed on smaller and smaller chips, which will eventually lead to better product design and a fluency in system to system compatibility.

"It's an ongoing, scientific relationship," Dr. Jansen says of his connection with CECS at UC Irvine. The relationship was bridged five years ago when Dr. Jansen was invited to UCI to participate in researching SW/HW co-design for medical applications; the hospitality with which he was received at the university then fostered the friendly relations that exist informally between the University of Offenburg and UC Irvine now. "I would come back every year if that was the situation," Dr. Jensen says of UC Irvine, "Irvine is a great place for living, a great place for research too."

During his stay here, Dr. Jensen has made some significant advantages in the field of compiler design for small embedded systems and has enjoyed discussing his interests with people working in similar fields.

He spoke at a seminar on Friday, July 22, about the systems his research has aided CECS in developing, the graphical representation of complex behavioral systems, and about the way the average compiler is designed.

Dr. Jansen has enjoyed his stay at CECS and is very thankful for the kindness and hospitality that the department and the university have shown him.

## Project Profile

### COMMEX:

### SoC Communication Architecture Modeling, Exploration and Synthesis

Communication architectures are responsible for supporting the ever increasing data traffic in modern embedded systems. They form a backbone in these designs through which processors, memories and other system components are inter-connected and act cohesively to fulfill application requirements. Most importantly, communication architectures have an enormous impact on the performance, cost and time-to-market of embedded systems, which makes them a very relevant topic in embedded systems research.

The COMMEX project was started back in the summer of 2003 in Professor Dutt's laboratory, with Sudeep Pasricha as the lead researcher collaborating with Conexant Inc. The primary objective of the collaboration was to model and explore bus-based communication architectures, such as the ARM AMBA bus architecture. Early work in this project dealt with creating a convenient modeling abstraction to capture embedded systems for the purpose of communication architecture exploration. The result of this work was the development of a new modeling abstraction model called CCATB, presented at the DAC 2004 and CODES-ISSS 2004 conferences. This new development allowed designers to capture an embedded system design with a high level language quickly, accurately, and with faster simulation performance than existing abstractions used for communication architecture exploration. Subsequently, Dutt's and Pasricha's work evolved to look at the problem of generation (or synthesis) of bus-based communication architectures. The two CECS affiliates presented a comprehensive, fully automated bus-architecture synthesis approach at ASPDAC 2005, which intelligently pruned the design space to generate bus architecture topology and parameter values in a matter of a few hours, instead of the days or even weeks it would normally take for the enormous exploration space created in the complex embedded systems of today.

A major project milestone was the development of the FABSYN methodology, which not only automated hierarchical bus-based communication architecture synthesis, but also made the process physical implementation aware. Bus cycle timing violations, which are an artifact of deep submicron effects caused by shrinking process technology, are normally detected during the physical implementation phase of the design and can take several weeks or even months to detect and eliminate. FABSYN enabled the detection and elimination of bus-cycle timing violations early in the design flow, thus drastically cutting down design time of modern embedded designs. FABSYN was presented and received a Best Paper Award Nomination at DAC 2005.

This research project illustrates the cut-

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## Heydari Receives Darlington Award at DAC 2005

Professor Payam Heydari was awarded the IEEE Circuits and Systems Society 2005 Darlington Award at the 42nd Design Automation Conference in 2005 for his journal paper, "Analysis of the PLL Jitter Due to Power/Ground and Substrate Noise." The paper analyzes the effect of the substrate and power/ground noise on the timing jitter of Phase-Locked Loops with the intention of first discovering where it comes from and eventually eliminating it altogether. Reducing substrate noise could be crucial for designing high performance integrated circuits such as PLLs that will be extensively used as a key component in wireless/wireline transceivers and microprocessors. A particular contribution of this paper, which had made it a candidate for the Darlington Award, is that it provided a bridge between theory and practice with practice.

The Darlington Award is given in honor of the pioneer of design of electronic circuits and systems, Dr. Sidney Darlington, and was first awarded in 1968. The award is given based on research that spans two years and effectively merges theory with practical applications; over 900 papers were eligible for the award.

Professor Heydari is very pleased to have received this award. He has been with CECS for four years and is currently an assistant professor of electrical engineering at UCI. He has recently been awarded the Henry Samueli Teaching Excellence Award and NSF CAREER Award, and is currently working on 3 full projects at UCI. "We're trying to be the first people across the world who ever dared to design a 120 GHz radio in silicon technology," Professor Heydari explains. Such high frequency circuits are usually designed and fabricated in advanced and more expensive processes, but Heydari is optimistic about exploring novel circuit topologies that can be implemented easily in mainstream silicon technology.

# EVENTS

## A Trip into the Jungle: The International Embedded Systems Symposium 2005

The International Embedded Systems Symposium (IESS) 2005, sponsored by the International Federation for Information Processing (IFIP), was held in Manaus, Brazil, from August 15 to 17, 2005. The conference theme addressed issues on the specification, design, and validation of embedded systems, including modeling, synthesis, and architectures for dependability and reconfigurability. This year the focus of IESS was on automotive applications emphasizing safety, reliability, and functionality. The symposium included 30 papers in 10 sessions presented by speakers from four continents and covering a wide variety of topics ranging from software via hardware to mechatronics.

After a 30 hour trip by plane, bus, and boat Gunar and I reached the conference location, the Ariau Amazon Towers Hotel. The conference hotel is the only hotel complex at tree top level in the Amazon rainforest.

Exotic plants and animals spot the area.

We had the opportunity to see sneaky snakes, huge bugs and beetles, freely flying parrots, and monkeys stealing food from tourists. We also went crocodile hunting where, after an hour of canoeing in the dark, we caught a caiman, one of the smaller reptiles in the Amazon region.

In summary, we have presented 3 papers, chaired 2 technical sessions, and received 1 best paper award.

Finally, mark your calendars for the next IESS which will be organized by CECS and is planned to take place in Irvine, California, in 2007.

*Submitted by Rainer Doemer and Gunar Schirner*

### Papers Presented

"Abstract Communication Modeling: A Case Study Using the CAN Automotive Bus", G. Schirner, R. Dömer

"Software and Driver Synthesis from Transaction Level Models", H. Yu, R. Dömer, D. Gajski

"Automatic Generation of Communication Architectures", D. Shin, A. Gerstlauer, R. Dömer, D. Gajski

## Project Profile, continued from page 3

ting-edge research being conducted by the Architectures and Compilers for Embedded Systems (ACES) labs as part of the Center for Embedded Computer Systems (CECS), together with funding from a CPCC, UC Micro and SRC. To keep up to date with the latest developments in the COMMEX project, track their web site at *http://www.cecs.uci.edu/~aces*. For questions, comments or feedback on the project, send email to *sudeep@cecs.uci.edu*

# PUBLICATIONS

The following were published by CECS faculty affiliates from June 1, 2005 to September 30, 2005

| Focus | Titles, Author, Publication |
|---|---|
| ***Dynamic Slack Reclamation*** | "Dynamic Slack Reclamation with Procrastination Scheduling in Real-Time Embedded Systems", Ravindara Jejurikar, Proceedings of the Design Automation Conference (DAC), June 13-16, 2005, pp 111-116 |
| ***HW-SW Partitioning*** | "Physically-Aware HW-SW Partitioning for Reconfigurable Architectures with Partial Dynamic Reconfiguration", Sudarshan Banerjee, Elaheh Bozorgzadeh, and Nikil Dutt, Proceedings of the Design Automation Conference (DAC), June 13-16, 2005, pp. 335-340. |
| ***Automated Synthesis*** | "Floorplan-Aware Automated Synthesis of Bus-based Communication Architectures", Sudeep Pasricha, Nikil Dutt, and Eleheh Bozorgzadeh, Proceedings of the Design Automation Conference (DAC), June 13-17, 2005, pp. 565-570. |
| ***Power Co-Optimization*** | "Application/Architecture Power Co-Optimization for Embedded Systems Powered by Renewable Sources", Dexin Li and Pai H. Chou, Proceedings of the Design Automation Conference (DAC), June 13-17, 2005, pp.618-623. |
| ***System-on-Chip Communication Design*** | "Automatic Network Generation for System-on-Chip Communication Design", D. Shin, A. Gerstlauer, R. Domer, D. Gajski,, Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis, September 2005. |
| ***Abstract Communication Modeling*** | "Abstract Communication Modeling: A Case Study Using the CAN Automotive Bus", G. Schirner, R. Dömer, Proceedings of the International Embedded Systems Symposium, "From Specification to Embedded Systems Application" (ed. A. Rettberg, Z. Mauro, F. Rammig), August 2005. |
| ***Software and Driver Synthesis*** | "Software and Driver Synthesis from Transaction Level Models", H. Yu, R. Dömer, D. Gajski, Proceedings of the International Embedded Systems Symposium, "From Specification to Embedded Systems Application" (ed. A. Rettberg, Z. Mauro, F. Rammig), August 2005. |
| ***Communication Architectures*** | "Automatic Generation of Communication Architectures", D. Shin, A. Gerstlauer, R. Dömer, D. Gajski, Proceedings of the International Embedded Systems Symposium, "From Specification to Embedded Systems Application" (ed. A. Rettberg, Z. Mauro, F. Rammig), August 2005. |
| ***Fast Evaluation*** | "Equivalence Checking of Arithmetic Expressions Using Fast Evaluation", M. Ghodrat, and T. Givargis, UCI CECS Technical Report 05-07, July 2005. |
| ***Transducer Architecture*** | "General Transducer Architecture", D. Gajski, H. Cho, and S. Abdi, UCI CECS Technical Report 05-08, August 2005. |
| ***No Instruction Set Computer*** | "Communication Design for No Instruction Set Computer", D. Gajski, and J. Trajkovic, UCI CECS Technical Report 05-09, July 2005. |
| ***TL Environment*** | "TL Environment", D.Gajski, A. Gerstlauer, R. Doemer, S. Abdi, J. Peng, D. Shin, UCI CECS Technical Report 05-10, July 2005. |
| ***NISC Technology*** | "NISC Technology and Preliminary Results", M. Reshadi, B. Gorjiara, and D. Gajski, UCI CECS Technical Report 05-11, August 2005 |

CECS—*promoting creativity and pursuing discovery!*

*Center for Embedded Computer Systems, University of California, Irvine*

***CECS** Mission Statement:*

*To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.*

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## Farewell Bob Larsen

CECS would like to say good bye to Bob Larsen. Bob diligently put out the *CECS eNews* and contributed to this column for the duration of his time with CECS; he retired from CECS in June of 2005 and is now raising his eleven year old grandson, Matthew.

Bob was a CECS member for close to a decade and a Rockwell Fellow prior to that. He is spoken of most highly in the department and is wished a happy and cheerful retirement from his friends and colleagues at CECS.

Sudeep Pasricha will be carrying on Bob's column.

Sudeep Pasricha is a fourth year graduate student affiliated with the Center for Embedded Computer Systems. He has written several articles for computer magazines in the past, and is currently a regula contributor to an online gaming magazine. He is especially interested in the more glamorous side of embedded systems - mp3 players, digital cameras, cell phones, portable gaming devices and any other sleek and shiny new gadgets he comes across during his regular sojourns to Gi modo or Engadget. He looks forward to contributing to the CECS newsletter.