CECS eNEWS

Volume 4, Issue 4, October 2004

Center for Embedded Computer Systems, University of California, Irvine

Highlights:

- CECS at ISLPED
- CECS at ICCSS
- *SPARK* Book Published
- Student Profiles
- NISC Processor

Inside this issue:

CECS influences ISLPED

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5 Papers Presented + Open House

Research affiliates and graduate students from the Center for Embedded Computer Systems (CECS) at the University of California, Irvine (UCI) influenced the International Symposium on Low Power Electronics and Design held at the Newport Beach Marriott Hotel, Newport Beach, CA from August 9—11, 2004 by presenting papers, serving on committees, and holding an Open House for symposium attendees.

Papers

The following technical papers were presented by CECS research affiliates with the cited pages from the conference proceedings:

- *Dynamic Voltage Scaling Techniques for System-Wide Energy Minimization in Real Time Embedded Systems*, Ravindra Jejurikar and Rajesh Gupta, pp 78—81
- *A Way-Halting Cache for Low-Energy High-Performance Systems*, Chuanjun Zhang, Frank Vahid, Jun Yang and Walid Najjar, pp 126—131
- *Maximizing Efficiency of Solar-Powered Systems by Load Matching*, Dexin Li and Pai Chou, pp 162—167
- *Power Utility Maximization for Multiple-Supply Systems by a Load-Matching Switch*, Chulsung Park and Pai Chou, pp 168—173
- *An Efficient Voltage Scaling Algorithm for Complex SoCs with Few Number of Voltage Modes*, Bita Gorjiara, Nader Bagherzadeh and Pai Chou, pp 381—386

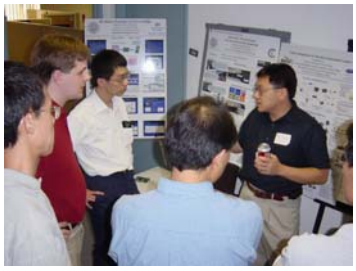
Committees

Professor Payam Heydari served as Local Arrangements Chair. Professors Pai Chou, Nikil Dutt, and Payam Heydari served as members of the Technical Program Committee.

Professor Payham Heydari severed as Co-Chair of a session titled *Circuits for Low Power Wireless* and Professor Pai Chou served as Co-Chair of a session titled *Energy Efficient Architectural Techniques*.

Open House

On Sunday evening, August 8, 2004, from 5:00 PM to 8:00 PM, CECS hosted an Open House for over seventy symposium attendees. Everyone enjoyed the delightful Southern California weather on the patio and the buffet contributed to a wonderful atmosphere enjoyed by all. Many graduate students presented posters defining their research projects which promoted several beneficial technology exchanges.



Shown above is Professor Pai Chou discussing CECS low power research projects with Graduate Student Nathaniel Pettis and Professor Yung-Hsiang Lu, Purdue University (2nd and 3rd left) and others.

CECS at ICCSS

CECS presented 5 papers and was well represented on committees at the IEEE/ ACM/IFIP International Conference on Hardware/ Software Codesign and System Synthesis (ICCSS) held in Stockholm, Sweden on September 8-10, 2004.

Papers

The following technical papers were presented by CECS research affiliates with the cited pages from the conference proceedings:

- *Efficient Mapping of Hierarchical Trees on Coarse-Grain Reconfigurable Architectures*, F. Rivera, M. Sanchez-Elez, M. Fernandez, R. Hermida and N. Bagherzadeh, pp 30—35
- *Efficient Search Space Exploration for HW/SW Partitioning*, S. Banerjee and N. Dutt, pp 122—127
- *Analytical Models for Leakage Power Estimation of Memory Array Structures*, M. Mamidipaka, K. Khouri, N. Dutt and M. Abadir, pp 146—151
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- *Fast Exploration of Bus-based On-chip Commination Architectures*, S. Pasricha, N. Dutt and M. Ben-Romdhane, pp 242—247

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ICCSS article continued from page 1 column 3.

Committees

Professors Alex Orailoglu and Pai Chou served as conference General Co-chairs. Professor Rajesh Gupta served as conference Past Co-chair. Professor Tony Givargis served as Publicity Chair and Professor Nikil Dutt served as IFIP Liaison. Professors Daniel Gajski, Fadi Kurdahi, Frank Vahid served as members of the Program committee. Professors Nikil Dutt, Daniel Gajski, Fadi Kurdahi, and Frank Vahid served as members of the 2003-2004 Steering Committee.

This year's conference organization and technical program was significantly influenced by these CECS researchers.

Veidenbaum/Orailoglu in IEEE Micro

Two CECS research affiliates made substantial contributions to the May/June 2004 issue of IEEE Micro magazine.

Professor Alex Veidenbaum served as Guest Editor of the issue and wrote the Guest Editor's Introduction: *Application-Specific Processors* appearing on pages 8 and 9.

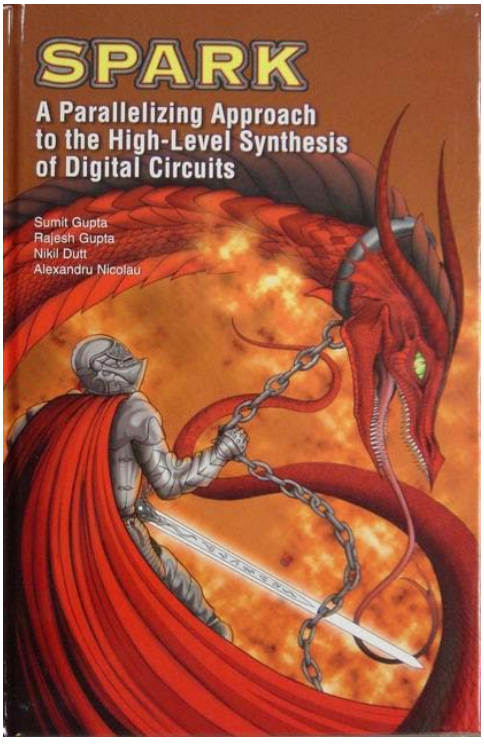
Professor Alex Orailoglu with Peter Petrov wrote a paper titled *Transforming Binary Code for Low-Power Embedded Processors* appearing on pages 21 through 33.

Congratulations are extended to Professors Veidenbaum and Orailoglu on their significant contributions to the May/June 2004 issue of IEEE Micro.

SPARK Book Published

Dr. Sumit Gupta and Professors Rajesh Gupta, Nikil Dutt, and Alexandru Nicolau are the authors of a new book titled *SPARK: A Parallelizing Approach To the High-Level Synthesis of Digital Circuits* published by Kluwer Academic Publishers in 2004. This book presents a novel approach to the high-level synthesis of digital circuits—that of parallelizing high-level synthesis (PHLS). This approach uses aggressive code parallelizing and code motion techniques to discover circuit optimization opportunities beyond what is possible with traditional high-level synthesis. This PHLS approach addresses the problems of the poor quality of synthesis results and the lack of controllability over the transformations applied during the high-level synthesis of system descriptions with complex control flows, that is, with nested conditionals and loops.

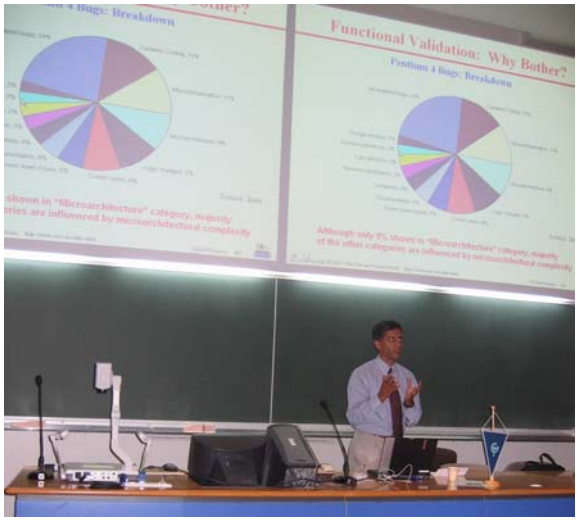
Also described are speculative code motion techniques and dynamic compiler transformations that optimize the circuit quality in terms of cycle time, circuit size and interconnect costs. The SPARK parallelizing high-level synthesis framework is described. The utility of the SPARK's PHLS approach is discussed using designs derived from multimedia and image processing applications. A case study is presented of an instruction length decoder derived from the Intel Pentium-class of microprocessors. This case study serves as an example of a typical microprocessor functional block with complex control flow and demonstrates how this methodology is useful for such designs.



The book also includes a CD of the SPARK software for downloading to a workstation or laptop computer.

Dutt Delivers Keynote Speech

Professor Nikil D. Dutt delivered a keynote speech to the Euromicro Symposium on Digital System Design (DSD 2004) held in Rennes, France on August 31—September 3, 2004. Professor Dutt's presentation was titled *Functional Validation of Programmable Architectures* and was coauthored with Prabhat Mishra. He identified the major bottleneck in current System-on-Chip (SoC) design methodologies to be the validation of programmable architectures consisting of processor cores, coprocessors, and memory subsystems. A critical challenge in the validation of such systems is the lack of a golden reference. Traditional validation techniques employ different reference models depending on the abstraction level and verification task, resulting in potential inconsistencies between multiple reference models. He then presented a validation methodology that uses an Architecture Description Language (ADL) based specification as a golden reference model for the validation of programmable architectures, and generation of executable models. He also presented a validation framework that uses the generated hardware as a reference model to verify the hand-written implementation using a combination of symbolic simulation and equivalence checking.



Mahesh Mamidipaka

CECS is honored to profile Mahesh Mamidipaka as an Outstanding Graduate Student and Research Assistant. He was born in Bapatla, India, in 1976. He received a B. Tech. in Computer Science and Engineering from Regional Engineering College, Warangal, India in 1997. In 1999, he received a M. E. in Micoelectronic Systems from the Indian Institute of Science, Bangalore, India.

Following graduation he was employed by Texas Instruments, Bangalore, India for one and a half years. During the summer of 2001 and 2002, he served as a Summer Intern with the Somerset Design Group, Motorola, Inc., Austin, Texas. His research focuses on developing power estimation algorithms for SRAMs at various levels of design hierarchy under the supervision of Professor Nikil D. Dutt. His thesis topic is titled *Power Estimation of Low-Power High-Performance Memory Array Structures*. His research on this topic has been done in collaboration with the Somerset Design Group, Motorola, Inc., Austin, Texas. His primary research interests are in the areas of power estimation, low power design, design space exploration, and computer architectures.

Some of Mahesh's recent publications are:

- *IDAP: A Tool for High-Level Power Estimation of Custom Array Structures*, Mahesh Mamidipaka, Kamal Khouri, Nikil Dutt and Maggdy Abadir, IEEE Transactions on Computer Aided Design (TCAD), September 2004, pp 1361-1369

- *Analytical Models for Leakage Power Estimation of Memory Array Structures*, Mahesh Mamidipaka, Kamal Khouri, Nikil Dutt and Maggdy Abadir, Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis, Stockholm, Sweden, September 1-3, 2004, pp 146-151

- *Processor-Memory Coexploration Using an Architecture Description Language*, Prabhat Mishra, Mahesh Mamidipaka and Nikil Dutt, ACM Transactions on Embedded Computing Systems (TECS), Volume 3, Number 1, February 2004, pp 143-162

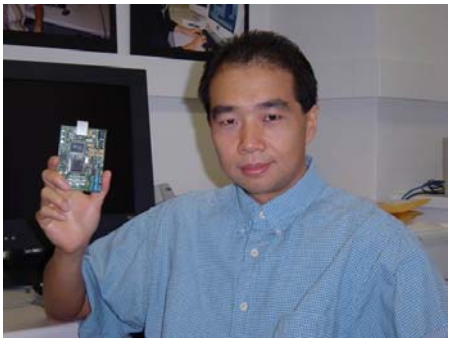
- *Adaptive Low Power Address Encoding Using Self-Organizing Lists*, Mahesh Mamidipaka, Dan Hirschberg and Nikil Dutt, IEEE Transactions on VLSI Systems (TVLSI), Volume 11, Number 5, October 2003, pp 827-834

- *On-Chip Stack Based Memory Organization for Low Power Embedded Architectures*, Mahesh Mamidipaka and Nikil Dutt, Proceedings of Design, Automation and Test in Europe (DATE), Messe Munich, Germany, March 3-7, 2003, pp 1082-1087

Jinfeng Liu

CECS is pleased and proud to profile Jinfeng Liu as an Outstanding Graduate Student and Research Assistant. Jinfeng Liu was born in Beijing, China. He received a BS in Electrical Engineering from Tsinghua University in 1994 and an MS in Computer Science from the Chinese Academy of Sciences in 1997. In 2000 he became a graduate student at UCI and has been conducting his research under the supervision of Professor Pai H. Chou.

Jinfeng Liu has made a number of significant technical contributions on the fields of power-aware systems and power instrumentation for battery-powered embedded systems. He has developed a timing/power constraint-driven system specification model and the corresponding scheduling algorithms for power-aware systems. He has also proposed a system-level energy optimization algorithm that performs simultaneous functional partitioning, communication speed selection, processor voltage/frequency scaling, and data compression for data-regular applications in a distributed architecture. His most recent contribution is the mode-transition analysis and optimization for multi-mode embedded systems. His new geometric formulation represents a breakthrough in power management by subsuming the conventional break-even-time analysis, and the optimization algorithms can automatically discover optimal mode transition sequences for both individual components and the entire system. In the field power instrumentation, Jinfeng Liu has developed possibly the most accurate, validated battery models to work with the B# battery emulator systems. He has also made key contributions to the host software for both the B# system and Eco, the smallest wireless sensor node. His contributions to these two research projects resulted in two Low Power Design Contest Awards at the International Symposium on Low Power Electronics and Design (ISLPED) in 2003 and 2004.



Jinfeng Liu research interests include design tools for power-aware embedded systems, hardware/software codesign, and distributed embedded systems. Some of his most recent publications are:

- *Optimizing Mode Transition Sequences in Idle Intervals for Component-Level Energy Minimization*, Jinfeng Liu and Pai H. Chou, to appear in Proceedings of the International Conference on Computer Aided Design (ICCAD), November 2004

- *Energy Optimization of Distributed Embedded Processors by Combined Data Compression and Functional Partitioning*, Jinfeng Liu and Pai H. Chou, Proceedings of the International Conference on Computer Aided Design (ICCAD), November 2003, pp 201-208

- *Combined Functional Partitioning and Communication Speed Selection for Networked Voltage-Scalable Processors*, Jinfeng Liu, Pai H. Chou and Nader Bagherzadeh, Proceedings of the 14th International Symposium on System Synthesis, Tokyo, Japan, October 2002, pp 14-19

CICS → RISC → NISC

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NISC: A novel processor architecture

Professor Daniel D. Gajski and graduate student Mehrdad Reshadi have been pursuing the development of a novel processor architecture—No Instruction Set Computer (NISC). This research has been partially funded by the Semiconductor Research Corporation (SRC).

Let's briefly examine the evolution of processor architecture.

CISC

The popular processor architecture of the 1970s was Complex Instruction Set Computer (CISC). The CISC program memory (PM) was slow so designers tried to improve performance by constructing complex instructions. Each complex instruction took several clock cycles to execute, with the data path control words for each clock cycle stored in a much faster micro program memory (μPM). The concept of micro programming allowed for emulation of any instruction set and construction of specialized instructions, while speeding up program execution. Unfortunately, micro programming did not allow for efficient pipelining of the Datapath.

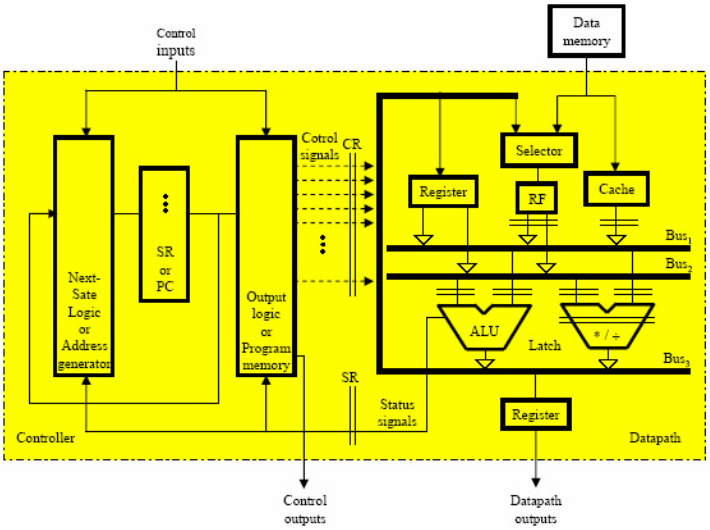
RISC

In the late 1980s, Reduced Instruction Set Computer (RISC) became popular by eliminating complex instructions and the μPM. All instructions in a RISC architecture are simple and execute in one clock cycle allowing the datapath to be efficiently pipelined in 4 to 8 pipeline stages. The μPM was replaced with a decoding stage that followed the instruction fetch from the μPM. Since instructions are simpler, a RISC processor needs approximately two instructions for each complex instruction and, therefore, the size of the PM is doubled. However, the Fetch-Decode-Execute-Store pipeline of the RISC improves the execution speed by several magnitudes.

NISC

The proposed No Instruction Set Computer (NISC) being developed at CECS, completely removes the decode stage and stores the control words in the PM. Since control words are 2 to 3 times wider than instructions, the PM increases in width by 2 to 3 times. Fortunately, each control word can execute 2 to 3 RISC instructions. Therefore, the NISC PM is equal in size to the RISC PM. Furthermore, each NISC control word is parameterizable and reconfigurable which allows for very fine tuning to any specific application and desired performance.

NISC Processor



The above schematic illustrates the NISC processor architecture. The NISC processor is a combination of a Controller and Datapath. The Controller can be fixed or programmable. The Datapath can be reprogrammable and reconfigurable. Reprogrammable means that the Datapath ban be extended or reduced by adding or omitting some components while reconfigurable means that the Datapath can be reconnected with the same components. Reconfiguring the NISC architecture means the original C code must be recompiled.

In order to speed up the NISC pipelining, a Control Register (CR) and a Status Register (SR) can be inserted between the Controller and the Datapath.

NISC Advantages

The benefits of the NISC architecture are:

1. The distinction between software and hardware implementation disappear. The hardware implementation is represented by control words that are stored in RAM or gate logic, while the software implementation is stored in RAM.
2. Since the data path can be pipelined by introducing any number of stages with any level of parallelism, it is extremely difficult to outperform NISC.
3. Since there is no instruction set, NISC eliminates the last stage of interpretation between C code and hardware. The C code runs directly on the hardware.
4. NISC can emulate any instruction set, since NISC control words can execute any operation as long as the datapath resources are available. Therefore, any legacy code can be executed on a properly defined NISC processor by converting the legacy instructions into NISC control words through a table look-up algorithm.
5. The NISC processor uses the High-Level Synthesis algorithms for covering a parse tree with control words.
6. Since NISC is a sufficient component for any computation, only one compiler is needed world wide. Hopefully, such a compiler will be in the public domain.
7. Similarly, only one NISC processor, although in different versions and with different parameters, is needed world wide. That uniqueness will greatly simplify education, design, testing, trade, and many other aspects of system design, in similar fashion as gate libraries led to standardization of digital design.

This research program illustrates the cutting-edge research being conducted at the Center for Embedded Computer Systems (CECS) at the University of California, Irvine. This type of innovative research we hope will significantly impact the development of future products. CECS is striving to develop technology transfer programs that will benefit the individual and society. Keep following this innovative research as it unfolds by tracking our web site: *www.cecs.uci.edu*. This research exemplifies our motto: *Solving tomorrow's problems*!

The following were published by CECS faculty affiliates during the period of July 1, 2004 to September 30, 2004:

Focus	Title, Authors, Publication
Transforming Binary Code	*Transforming Binary Code for Low-Power Embedded Processors*, Peter Petrov and Alex Orailoglu, IEEE Micro, May/June 2004, pp 21—33
Voltage Scaling	*Dynamic Voltage Scaling Techniques for System-Wide Energy Minimization in Real-Time Embedded Systems*, Ravindra Jejurikar and Rajesh Gupta, Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED), August 9-11, 2004, pp 78—81
Way-Halting Cache	*A Way-Halting Cache for Low-Energy High-Performance Systems*, Chuanjun Zhang, Frank Vahid, Jun Yang and Walid Najjar, Proceedings of the Symposium on Low Power Electronics and Design (ISLPED), August 9-11, 2004, pp 126—131
Load Balancing	*Maximizing Efficiency of Solar-Powered Systems by Load Balancing*, Dexin Li and Pai Chou, Proceedings of the Symposium on Low Power Electronics and Design (ISLPED), August 9-11, 2004, pp 162—167
Power Utility Maximization	*Power Utility Maximization for Multiple-Supply Systems by a Load-Matching Switch*, Chulsung Park and Pai Chou, Proceedings of the Symposium on Low Power Electronics and Design (ISLPED), August 9-11, 2004, pp 168—173
Voltage Scaling Algorithm	*An Efficient Voltage Scaling Algorithm for Complex SoC's with Few Number of Voltage Modes*, Bita Goriara, Nader Bagherzadeh and Pai Chou, Proceedings of the Symposium on Low Power Electronics and Design (ISLPED), August 9-11, 2004, pp 381—386
Hierarchical Trees	*Efficient Mapping of Hierarchical Trees on Coarse-Grain Reconfigurable Architectures*, F. Rivera, M. Sanchez-Elez, M. Fernandez, R. Hermida and N. Bagheradeh, Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (ICCSS), September 8-10, 2004, pp 30—35
Search Space Exploration	*Efficient Search Space Exploration for HW/SW Partitioning*, S. Banerjee and N. Dutt, Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (ICCSS), September 8-10, 2004, pp 122—127
Leakage Power Models	*Analytical Models for Leakage Power Estimation of Memory Array Structures,* M. Mamidipaka, N. Dutt, K. Khouri and M. Abadir, Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (ICCSS), September 8-10, 2004, pp 146—151
Operation Tables	*Operation Tables for Scheduling in the Presence of Incomplete Bypassing,* A. Shrivastava, N, Dutt and A. Nicolau, Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (ICCSS), September 8-10, 2004, pp 194—199
Communication Architectures	*Fast Exploration of Bus-based On-chip Communication Architectures*, S. Pasricha, N. Dutt and M. Ben-Romdhane, Proceedings of the IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (ICCSS), September 8-10, 2004, pp 242—247
Functional Validation	*Functional Validation of Programmable Architectures*, P. Mishra and N. Dutt, Proceedings of the Euromicro Symposium on Digital System Design (DSD 2004), August 31—September 3, 2004, pp 12-19
RTL Modeling	*Cycle-Accurate RTL Modeling with Multi-Cycled and Pipelined Components*, Rainer Doemer, Andreas Gerstlauer and Dongwan Shin, UCI CECS Technical Report 04-19, July 2004
Instruction Set Extensions	*ISEGEN: Adapting Kernighan-Lin Min-Cut Heuristic for Generation of Instruction Set Extensions*, Partha Biswas, Sudarshan Banerjee, Nikil Dutt, Lara Pozzi, and Paolo Ienne, UCI CECS Technical Report 04-21, August 2004
Power Management	*Systematic Power Management of Heterogeneous Real-Time Systems by Dynamic Schedule Analysis*, Bita Gorjiara and Nader Bagherzadeh, UCI CECS Technical Report 04-26, September 2004

CECS—Solving Tomorrow's Problems!

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Design Simplicity

I recently had an eye opening experience in design simplicity. The last week of July, I attended an intergenerational, one week, space camp at Johnson Space Center in Houston, Texas with my 10 year old grandson, Matthew Larsen. We did several interesting and challenging experiments demonstrating Newton's three laws of motion. We constructed and launched a rocket, built and played with a robot, and built and dynamically tested astronaut environments. I will discuss only two of these experiments.

Experiment I

We had to design an astronaut environment for the Space Shuttle. A miniature space shuttle was launched down a 20 foot wire at a 45 angle. The astronaut was an egg within the miniature shuttle. We were given different materials; each type of material had an associated cost. The problem was to design a minimum cost astronaut environment that would survived the crash.

Experiment II

We had to design an astronaut space suit to withstand a meteor collision. The astronaut was a small balloon. We were again given different materials; each type of material had an associated cost. The encapsulated balloon, representing the space suit, was tested by a pseudo meteor; sending a nail sinker down a 6' 1/2" PVP pipe. The problem was to design a minimum cost astronaut space suit to survive a meteor collision.

At first encounter, these experiments may seem trivial. However, try protecting a small balloon with only cloth, wax paper, or aluminum foil. This is a difficult problem given only a small amount of material. However, the design experience was really fun!

Stress Simplicity

What can we learn by doing simple experiments involving complex design issues? First, we must thoroughly comprehend the underlying sciences and technology. Second, we must thoroughly understand the problem and goals. Third, we must create an innovative and economically feasible solution. Fourth, we must dynamically test our design. And fifth, we must correct any detected design flaws. These rules also apply to complex embedded systems. Let's ruthlessly attack design complexity with a vengeance and emphasize design simplicity more! The resulting design elegance and potential gains in designer productivity could be enormous.

Bob Larsen