CECS eNEWS

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Center for Embedded Computer Systems, University of California, Irvine

Highlights:

- 2003 SCESS
- SPARK Tool Release
- Wolf Distinguished Lecture
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2003 Southern California Embedded Systems Symposium

The Center for Embedded Computer Systems (CECS) at the University of California, Irvine hosted the 2003 Southern California Embedded Systems Symposium ('03 SCESS) at the Beckman Conference Center on September 30, 2003.

SCESS Welcome Address being delivered by Dean Nicolaos Alexopoulos

SCESS is specifically targeted for the Orange County technical community and engineers desiring to stay abreast of reconfigurable and adaptive design technologies as applied to embedded systems.

CECS is striving to make SCESS a premiere technology transfer event and an opportunity to showcase and promote its research capabilities to the Orange County technical community.

About 125 SCESS attendees listened attentively to the lunch keynote address, titled *Technologies Driving the Digital Home,* delivered by Matt Rhodes, President, Conexant Systems, Inc., Newport Beach, CA.

Matt Rhodes, President, Conexant Systems, Inc. delivering SCESS Keynote Address

The closing executive address, titled *Commercialization Challenges Confronting Reconfigurable Technology,* was delivered by Shahriar Sadri, CEO, Morpho Technologies, Inc., Irvine, CA.

Shahriar Sadri, CEO, Morpho Technologies, Inc. delivering SCESS Executive Address

CECS gratefully acknowledges the generous donations of this year's SCESS sponsors: Conexant Systems, Inc, Newport Beach, CA, Emulex Corporation, Costa Mesa, CA and Intel Corporation, Santa Clara, CA.

SPARK Tool Release

Dr. Sumit Gupta and Professors Nikil Dutt, Rajesh Gupta and Alex Nicolau have announced the release of the SPARK parallelizing high-level synthesis tool developed at the Center for Embedded Computer Systems. SPARK translates the behavior of an application, specified in C, and produces register-transfer level (RTL) VHDL. SPARK employs several parallelizing compiler and high-level synthesizing transformations to generate a scheduled, resource bound, data path along with a finite state machine (FSM) controller. The SPARK download can be achieved at: www.cecs.uci.edu/~spark. This download has SPARK binaries for Solaris and Linux platforms, a User Manual, and a Tutorial with a MPEG-1 player as an example.

2003 SCESS Posters & Winners

1st Place SCESS Poster Award Winner Chuangjun Zhang with Marshall Lee, Emulex Corp.

2nd Place SCESS Poster Award Winner Sudeep Pasricha with Marshall Lee, Emulex Corp.

3rd Place SCESS Poster Award Winner Roman Lysecky with Marshall Lee, Emulex Corp.

A Poster Display area showcased the CECS research programs to the SCESS attendees. CECS graduate students submitted 31 posters for consideration of which the committee selected 28 to be showcased at the symposium. The '03 SCESS Poster committee was: Professor Tony Givargas, CECS, UCI, Marshall Lee, Emulex Corp. and Dr. Frank Micheletti, Conexant Systems, Inc.

The graduate student highlight of SCESS was the anticipated announcement of the winning posters. Marshall Lee hosted the poster awards presentations. The first place award of $500 was presented to Chuangjun Zhang (Professors Vahid and Najjar) for the poster titled *A Highly Configurable Cache Architecture for Embedded Systems*, the second place award of $250 was presented to Sudeep Pasricha (Professor Dutt) for the poster titled *Reducing Backlight Power Consumption for Streaming Video Applications on Mobile Handheld Devices*, and the third place award of $100 was presented to Roman Lysecky (Professor Vahid) for the poster titled *WARP Processors*. Three honorable mention awards went to: Nikhil Bansal (Professor Dutt) for the poster titled *Network Topology Exploration of Mesh-Based Coarse-Grain Reconfigurable Architectures*, Susan Cotterel (Professor Vahid) for the poster titled *First Results with eBlocks: Embedded Systems Building Blocks*, and Andre Nacul (Professor Givargis) for the poster titled *Dynamic Voltage and Cache Reconfiguration for Low Power*.

Congratulations to these 2003 SCESS Poster Award winners who are pictured on this page receiving their award citation from Marshall Lee, Vice President of Engineering, Emulex Corporation, Costa Mesa, CA.

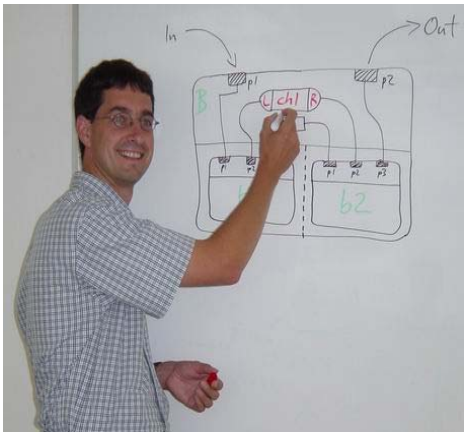
Honorable Mention SCESS Poster Award Winner Susan Cotterel with Marshall Lee, Emulex Corp.

Honorable Mention SCESS Poster Award Winner Andre Nacul with Marshall Lee, Emulex Corp.

Honorable Mention SCESS Poster Award Winner Nikhil Bansal with Marshall Lee, Emulex Corp.

Introducing Prof. Doemer

The Center for Embedded Computer Systems (CECS) is pleased to introduce a new research affiliate Assistant Professor Rainer Doemer, Department of Electrical Engineering and Computer Science, the Henry Samueli School of Engineering, University of California, Irvine.



Professor Doemer was born in Luedinghausen, Germany and received a Diploma in Information and Computer Science from the University of Dortmund, Germany in 1995 and a PhD in Computer Science from the University of Dortmund, Germany in 2000. His PhD research and thesis defined the *SpecC* language and methodology which created a world-wide impact in industry and academia resulting in the organization of the international *SpecC* Technology Open Consortium (STOC) in 1999; today, STOC comprises over 30 universities and 30 companies.

Professor Doemer joined CECS as a Post Doctoral Researcher in January 2001. He was instrumental in leading the development of the *SpecC* Reference Compiler and Simulator which are freely available from STOC. He led the discussion and refinement on execution and synchronization semantics in the language working group and was chosen to document the official *SpecC* language reference manual. He contributed and coordinated the development of a new system design tool, System-on-Chip Environment (SCE) with support for estimation, validation and synthesis of SoC. SCE features automatic model refinement down to a cycle-accurate implementation.

Professor Doemer is the coauthor of 2 books on *SpecC* technology: *System Design: A Practical Guide with SpecC*, A. Gerstlauer, R. Doemer, J. Peng and D. Gajski, Kluwer Academic Publishers, Boston, June 2001 and *SpecC: Specification Language and Methodology*, D. Gajski, J. Zhu, R. Doemer, A. Gerstlauer, and S. Zhao, Kluwer Academic Publishers, Boston, March 2000.

Professor Doemer's research interests include embedded systems software and middleware, architecture exploration, system synthesis, and system design standardization for communications, networking and automotive applications.

Professor Doemer lives in University Hills with his wife, Julia, and daughters, Sophie and Klara, and son Simon.

Contracts and Gifts

- Professor Daniel Gajski received a gift of a Virtex-II Multimedia Development Board donated by the Xilinx Corporation, San Jose, CA valued at $3,895
- Professor Alex Veidenbaum received a gift of a Network Appliance File Server from Smartech Consulting, Inc., Markham, Ontario, Canada valued at $10,500
- Professor Nikil Dutt received a contract titled *Compiler-in-the-Loop ADL-Driven Early Architectural Exploration* from the Semiconductor Research Corporation for $318,000
- Professor Daniel D. Gajski received a contract titled *No-Instruction-Set-Computer (NISC) Technology* from the Semiconductor Research Corporation for $309,000
- Professor Alex Veidenbaum received a contract titled *A Framework for Speeding Up Mobile Code Execution in Embedded Systems Using Annotations* from the National Science Foundation for $250,000
- Professor Nikil Dutt received a MICRO contract titled *Bus-Based SoC Architectural Exploration* from Conexant Systems, Inc.
- Professors Nikil Dutt and Alex Nicolau received a MICRO contract titled *ADL-Driven, Compiler-in-the-Loop Early Architectural Exploration* from Intel Corp.

Wolf Delivers CECS Distinguished Lecture

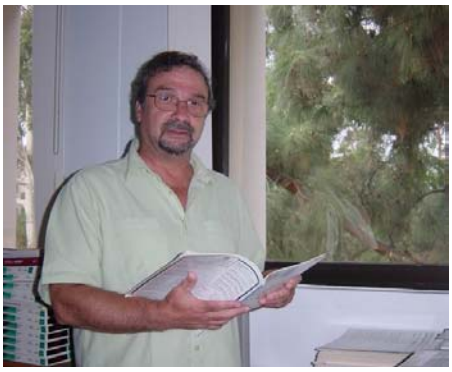
On July 22, 2003, Professor Wayne H. Wolf, Professor of Electrical Engineering, Department of Electrical Engineering, Princeton University, Princeton, New Jersey, delivered a CECS Distinguished Lecture titled *Smart Cameras as High Performance Embedded Systems* to an overflowing audience at the UCI McDonnell Douglas Auditorium. Professor Daniel D. Gajski, CECS Director, introduced Professor Wolf and served as his host during his visitation to CECS.

Professor Wolf discussed the research activities of the Embedded Systems Research Group at Princeton in developing a smart camera as an example of a high-performance embedded computing system. This prototype smart camera performs real-time computations on an image/video stream and performs human gesture recognition. Professor Wolf described the design challenges in developing the smart camera from software executing on a general-purpose computer through an application-specific multiprocessor.

Prior to joining the faculty at Princeton University, Professor Wolf was a researcher at A T & T Bell Laboratories, Murray Hill, New Jersey. He received the BS, MS, and PhD degrees in electrical engineering from Stanford University in 1980, 1981, and 1984, respectively. His research interests include embedded computing, VLSI systems, and multimedia information systems. He is the author of *Computers as Components: Principles of Embedded Systems Design*, *Hardware-Software Co-Synthesis of Distributed Embedded Systems*, and *Modern VLSI Design* (for which he won the ASEE/CSE and HP Frederick E. Terman Award). Professor Wolf has been elected to Phi Beta Kappa and Tau Beta Pi. He is a Fellow of the IEEE and ACM and a member of SPIE and ASEE.

Introducing Prof. Scherson

CECS would like to introduce a new research affiliate—Professor Isaac D. Scherson. Professor Scherson is academically affiliated with the Department of Computer Science, School of Information and Computer Science and the Department of Electrical Engineering and Computer Science, the Henry Samueli School of Engineering, University of California, Irvine since 1991.



Professor Scherson was born in Santiago, Chile. He received a BSEE and MSEE from the National University of Mexico, Mexico City, Mexico and a PhD in Computer Science from the Weizmann Institute of Science, Rehovot, Israel. He was elected to Eta Kappa Nu Electrical Engineering Honor Society.

Professor Scherson was a member of the faculty in the Department of Electrical and Computer Engineering, University of California, Santa Barbara from 1983 to 1987 and the Department of Electrical Engineering, Princeton University, Princeton, NJ from 1987 to 1991.

Professor Scherson is a member of ACM and IEEE. Since 1992, he has served as a member of the IEEE Computer Society Technical Committee on Computer Architecture (TCCA) and the IEEE Computer Society Technical Committee on Parallel Processing (TCPP). The author of numerous technical articles, he edited the Frontier's 92 workshop book, the IEEE Tutorial on Interconnection Networks (1994—currently in its second edition), and was the Guest Editor of the IEEE Special Issue of the Visual Computer on Foundations of Ray Tracing, June 1990.

Givargis Receives Teaching Award

At the 10th Annual Celebration of Teaching, hosted by the UCI Division of Undergraduate Education on May 29, 2003, Assistant Professor Tony Givargis was honored and received an engraved plaque. The Annual Celebration of Teaching honors Senate and non-Senate faculty for Teaching Excellence.

Congratulations, Tony, on receiving this distinguished teaching award and we hope your commitment to teaching excellence will continue impacting UCI students for many more semesters!

Scherson, continued

His current research interests include concurrent computing systems, interconnection networks for embedded systems, resource management for embedded systems, operating systems for concurrent computers, massively parallel computer architectures, computer graphics, algorithms and their complexity, and VLSI.

Professor Scherson lives in Irvine, is happily married to Sandrine, and the proud father of a son at the University of California, Berkeley studying Mechanical Engineering.

Heydari, continued

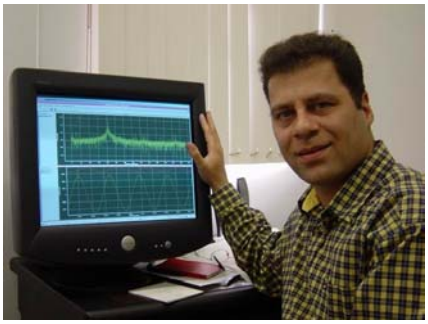
posium on Physical Design (ISPD), and the International Symposium on Quality Electronic Design (ISQED). He also serves as a Student Design Contest Judge for the Design Automation Conference (DAC).

Professor Heydari's research interests include the design and simulation of analog, RF, and mixed-signal integrated circuits and VLSI interconnect architecture, analysis and simulation.

Professor Heydari lives in University Hills with his wife Negaah.

Introducing Prof. Heydari

CECS is pleased to introduce Assistant Professor Payam Heydari as a new research affiliate. Professor Heydari received the BS and MS degrees, with honors, in Electrical Engineering from Sharif University of Technology, Tehran, Iran in 1992 and 1995, respectively. He received the PhD degree from the University of Southern California in 2001. He has been an Assistant Professor of Electrical Engineering, Department of Electrical Engineering and Computer Science, the Henry Samueli School of Engineering, University of California, Irvine since September 2001.



During the summer of 1997 he conducted research on noise analysis in deep submicron VLSI circuits at Bell Laboratories, Lucent Technology, Inc. During the summer of 1998 he conducted research on gradient-based optimization and sensitivity analysis of custom integrated circuits at T. J. Watson Research Center, IBM.

Professor Heydari received the the Best Paper Award at the 2000 IEEE International Conference on Computer Design. In 2000, he received the Honorable Mention Award from the Department of Electrical Engineering—Systems at the University of Southern California. In 2001, he received the USC Technical Excellence Award and the Best Iranian Graduate Student Award in Electrical Engineering from the Association of Professors and Scholars of Iranian Heritage in California.

Professor Heydari serves as a member of the Technical Program Committee of the IEEE Design and Test in Europe Conference (DATE), the International Sym

Configurable Processors

This presentation is a condensed version of a paper titled ***Configurable Processors for Embedded Computing*** *by Nikil Dutt and Kiyoung Choi published in IEEE Computer dated January 2003.*

We have all heard about the increasing software content of embedded systems. To those who think of embedded software as autonomous programs hidden deep within the system, plugging away transparently and reliably on dedicated tasks, this increase might suggest that these programs are somehow becoming larger. In reality, the ongoing increases in processor performance let system designers implement in software what previously required dedicated or custom hardware blocks and accelerators.

Indeed, given a choice, system designers might actually prefer the flexibility of implementing all embedded applications in software on programmable processors. However, parts of the applications must often run under critical time, performance, power, and cost constraints. Thus, designers have traditionally mapped these segments into custom hardware, such as application-specific integrated circuits (ASICs), or into reprogrammable fabrics, such as field-programmable gate arrays (FPGAs).

Embedded Processor Landscape

With the continuing integration of yesterday's board into today's chip, the role of embedded processors is also changing. The contemporary embedded system landscape cuts a broad swath—from low-end microcontrollers to high-performance processing engines.

Designers can integrate the processors into SoCs as either hard cores with fixed layouts or custom designed soft cores synthesized from Hardware Description Language specifications. But the processor's instruction set and the architectural features and parameters are typically fixed and not configurable for application-specific optimization. Integrating the processing cores with reconfigurable logic is another way to boost performance while retaining hardware-acceleration benefits.

However, the need for differentiation in the marketplace, coupled with ever-increasing chip capacities, opens the door for significant customization of the processor cores themselves.

Configurable Processors

Companies such as ARC, Improv, and Tensilica now offer configurable processors. This gives embedded systems designers virtually unlimited choices in processor architectures, allowing them to customize several features to suit the application and design constraints at hand.

While the idea of customizing processors is appealing, it opens up new challenges: customization of the entire software tool chain, including compilers, simulators, debuggers; synthesis of processor models; and validation and verification of generated processor designs.

Analyze This…Configure That

Since configurability increases the design space, taking maximum advantage of this potential requires a design system supporting efficient design space exploration. This design system must support aggressive optimization; e.g. instruction set architecture, memory organization, and overall system architecture in conjunction with coprocessors, hardware logic, parallelism, multiprocessor and bus architecture.

Thus, a separate exploration phase for design flow efficiency would let system designers evaluate different base processor candidates and memory organizations. A simulator and a compiler generated in this phase could support rapid design space exploration in an estimation mode. A subsequent refinement phase could generate a cycle-accurate simulator and an optimizing compiler that allows the designer to fine-tune the processor characteristics and memory subsystem.

To fully evaluate the effects of different processor configurations, the design system must consider not only the processor but also the interactions with the entire SoC, including memory subsystem, buses, peripherals, and any other processing or coprocessing engines.

And Then There Were More

Many current SoCs already contain multiple processors that work collaboratively on application tasks. Local optimization of a configurable processor is insufficient for such systems. A critical need exists for design tools that let system designers explore a heterogeneous multiprocessor system, selecting and customizing each processor core and performing system-level optimization across multiple configurable processors.

Further, designers typically base existing configurable processors on one of three architectural styles: reduced-instruction-set computing, very large instruction word, or digital signal processing. As designers investigate alternative architectures, such as simultaneous multithreading, they will need tools that permit the exploitation of thread-level and instruction parallelism in an application.

Configure or Reconfigure?

Configurable implies a one-time customization of the processing engine prior to manufacturing. By comparison, reconfigurable processors support both post manufacturing and dynamic runtime configurability. Reconfigurability promises effective design reuse across multiple applications, without incurring new fabrication costs. An application could reuse the reconfigurable block on silicon across multiple tasks by dynamically changing the configuration. System designers could also combine reconfigurability with configurable processor technology—for instance, as a reconfigurable coprocessor or as a part of the data path, control, or interconnect of the configurable processor itself.

Proponents of configurable processor technology claim that it presents a paradigm shift in the design of next-generation embedded SoCs. They see it empowering application designers to create customized processors that can run their application codes efficiently while eliminating the entire complex chain of the processor flow design.

While this is true in principle, significant challenges remain in making this technology robust across a variety of architectural models and platforms. Although the technology has demonstrated its viability for niche application domains, whether its applications will actually extend broadly across embedded system design remains to be seen. Nevertheless, research in Architecture Description Languages is moving the design process in this direction, and recent commercial offerings have already demonstrated the power of configurable processors for some application domains.

The following were published by CECS faculty affiliates during the period of July 1, 2003 to September 30, 2003:

Focus	Title, Authors, Publication
Compacting Test Responses	*Compacting Test Responses for Deeply Embedded SoC Cores*, Ozgur Sinanoglu, and Alex Orailoglu, IEEE Design & Test of Computers, July-August 2003, pp 22—30
Rapid Exploration	*Rapid Exploration of Pipelined Processors Through Automatic Generation of Synthesizable RTL Models*, Prabhat Mishra, Arun Kejariwal and Nikil Dutt, Proceedings of the 14th IEEE Workshop on Rapid System Prototyping, June 9-11, 2003, pp 226—232
Validation Methodology	*A Methodology for Validation of Microprocessors using Equivalence Checking Communication Refinement for System Level Design*, Prabhat Mishra and Nikil Dutt, Proceedings of the 4th Workshop on Microprocessor Test and Verification, May 29-30, 2003
Data Cache Energy Consumption	*Reducing Data Cache Energy Consumption via Cached Load/Store Queue*, D. Nicolaescu, A. Veidenbaum and A. Nicolau, Proceedings of the 2003 International Symposium on Low Power Electronics and Design, Seoul, Korea, August 25-27, 2003, pp 252—257
Battery Emulator	*B#: a Battery Emulator and Power Profiling Instrument*, P. H. Chou, C. Park, J. Park, K. Pham and J. Liu, Proceedings of the 2003 International Symposium on Low Power Electronics and Design, Seoul, Korea, August 25-27, 2003, pp 288—293
Instruction Set Synthesis	*Energy-Efficient Instruction Set Synthesis for Application-Specific Processors*, J.-e. Lee, K. Choi and N. D. Dutt, Proceedings of the 2003 International Symposium on Low Power Electronics and Design, Seoul, Korea, August 25-27, 2003, pp 330—333
Power Amplifier	*A Novel High Frequency, High-Efficiency, Differential Class-E Power Amplifier in 0.18um CMOS*, Payam Heydari and Ying Zhang, Proceedings of the 2003 International Symposium on Low Power Electronics and Design, Seoul, Korea, August 25-27, 2003, pp 455—458
Interface Synthesis	*Interface Synthesis Using memory Mapping for an FPGA Platform*, Manev Luthra, Sumit Gupta, Nikil Dutt, Rajesh Gupta and Alex Nicolau, UCI CECS Technical Report 03-20, June 9, 2003
SoC Specification Guide	*System-on-Chip Specification Style Guide*, Andreas Gerstlauer, Kiran Ramineni, Rainer Doemer and Daniel Gajski, UCI CECS Technical Report 03-21, June 2003
On Demand Paging	*On Demand Paging Using Bluetooth Radios on 802.11 Based Networks*, Yuvraj Agarwal and Rajesh Gupta, UCI CECS Technical Report 03-22, July 2003
Hybrid Simulation	*Hybrid Compiled Simulation*, Mehrdad Reshad and Nikil Dutt, UCI CECS Technical Report 03-23, July 2003
Branch Prediction	*Novel Techniques to Improve Branch Prediction Accuracy for Embedded Processors in the Presence of Context Switches*, Sudeep Pasricha and Alex Veidenbaum, UCI CECS Technical Report 03-24, August 2003
ADL Validation	*Architectural Description Language Driven Validation of Dynamic Behavior in Pipelined Processor Specifications*, Prabhat Mishra, Nikil Dutt, and Hiroyuki Tomiyama, UCI CECS Technical Report 03-25, July 28, 2003
SoC Component Models	*System-on-Chip Component Models,* Andreas Gerstlauer, Lukai Cai, Dongwan Shin, Rainer Doemer and Daniel D. Gajski, UCI CECS Technical Report 03-28, September 2003
Reconfigurable Component	*NISC: The Ultimate Reconfigurable Component,* Daniel D. Gajski, UCI CECS Technical Report 03-28, September 2003
Architecture Refinement	*Provably Correct Architecture Refinement,* Samar Abdi and Daniel Gajski, UCI CECS Technical Report 03-29, September 2003
Debugging & Verification	*System Debugging and Verification: A New Challenge,* Samar Abdi and Daniel Gajski, UCI CECS Technical Report 03-31, September 2003

CECS—Solving Tomorrow's Problems!

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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What's in a name?

I recently realized the **e**lite status of the vowel **e**. As you **e**valuate corporate literature and advertisements today, **e** appears **e**verywhere. **e**Business is **e**normous! For the last month, I have been collecting **e**<thing> from corporate literature and advertisements. The following is a sampling that I have observed:

eBags	**e**Seminars
eBlocks	**e**Server
eDiets	**e**Soft
eEye	**e**Synergy
eHarmony	**e**Team
eHelp	**e**Token
eGovernment	**e**Trust
eSafe	**e**Universe
eSecurity	**e**Week

and of course **CECS** *eNEWS*!

In late 2000, Professor Daniel Gajski and I were discussing various means of **e**loquently **e**xposing the research activities and accomplishments of CECS to the outside world. The major challenge was to **e**xecute any idea at very low cost. Thus, we ruled out the conventionally printed and mailed newsletter. We suddenly realized that **e**mail would be a very cost-**e**ffective distribution media. Thus was born **CECS** *eNEWS*. The first issue was published and **e**lectronically distributed via **e**mail in April 2001.

When we were seeking a catchy name for our quarterly newsletter, we **e**lected **CECS** *eNEWS*. Little did we realize that we were an **e**arly part of the **e** **e**volution.

In **CECS** *eNEWS*, we have strived to **e**loquently **e**mphasize our research activities and accomplishments. We have strived to **e**xemplify **e**xceptional **e**xcellence in our research presentations and reporting. In the future, we hope to **e**mphasize more **e**xpositions on seminal topics relating to **e**mbedded systems, **e**xperiments and theories.

We hope you continue to **e**njoy our quarterly newsletter. Our **e**ditorial philosophy is quit simple. We will continue to **e**nergetically **e**mphasize the pictorial content because we believe pictures are **e**loquent conveyors of information. We will **e**laborate, **e**xplore, **e**xperiment, **e**xhibit and **e**xplain new ideas and presentation styles as we strive to **e**ducate and **e**nlighten our reader community using **e**lectronic distribution. The satisfaction we receive is your **e**levating complimentary **e**xpressions; we hope you will continue to **e**njoy reading **CECS** *eNEWS*!

Bob **e**Larsen