October 2001

CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights

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Inside this issue:

CECS Interns

The Center for Embedded Computer Systems (CECS) at the University of California, Irvine had several graduate students spend the summer months as interns with several cooperating companies. These assignments allow our graduate students to be exposed to the challenges of an industrial design environment. They return to CECS with an enlightened technical perspective toward their research activities. These industrial assignments are an important part of our graduate education program for developing future engineers and teachers. The following graduate students were CECS Interns this summer:

- **Lukai Cai**

Graduate Student Lukai Cai spent the summer as an Industrial Intern at the Advanced System Architecture Laboratory, Motorola, Inc. in Austin, TX. He was associated with the System-on-Chip (SoC) design technology team and reported to Paul Kritzinger. His assignment was related to improving the top-down SoC design methodology by using the **SpecC** language and design methodology. Lukai's research at CECS is being supervised by Professor Daniel D. Gajski.

- **Sumit Gupta**

Graduate Student Sumit Gupta spent the summer as an Industrial Intern at the Strategic CAD Laboratory, Intel, Inc. in Hillsboro, Oregon. He was associated with the high-level design team and reported to Timothy Kam. His work centered around going beyond the classical notions of high-level synthesis as an automated design technique for ASIC design, to targeting high-level synthesis for high performance microprocessor blocks. Sumit's research at CECS is being supervised by Professor Rajesh K. Gupta.

- **Mahesh Mamidipaka**

Graduate Student Mahesh Mamidipaka spent the summer as an Industrial Intern at the Somerset PowerPC Microprocessor Design Center, Motorola, Inc. in Austin, TX. He was associated with the High Performance Tools and Methodology Group and reported to Derek Beatty. His assignment involved developing models and methodologies for micro-architecture level power estimation necessary for evaluating different power-performance trade-offs for SoC designs. Mahesh's research at CECS is being supervised by Professor Nikil D. Dutt.

- **Prabhat Mishra**

Graduate Student Prabhat Mishra spent the summer as an Industrial Intern at the Somerset PowerPC Microprocessor Design Center, Motorola, Inc. in Austin, TX. He was associated with the High Performance Tools and Methodology Group and reported to Magdy Abadir. His assignment was related to Architectural Description Language (ADL) driven validation of microprocessors. Prabhat's research at CECS is being supervised by Professor Nikil D. Dutt.

- **Srikanth Srinivasan**

Graduate Student Srikanth Srinvasan spent the summer as an Industrial Intern at the Somerset PowerPC Microprocessor Design Center, Motorola, Inc. in Austin, TX. He

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CECS Research Advisory Board

In the maturing of CECS as an international leader in embedded systems research, we have decided to create a Research Advisory Board to help guide our future research program. We hope to appoint prominent business leaders who have broad experience in emerging technologies and product development. These prominent business leaders will be available to our faculty associates for discussing technology and product trends, fundamental research planning and funding issues. We are pleased to announce the following member to our Research Advisory Board:

- **Dr. Gilbert F. Amelio**

Dr. Gilbert (Gil) F. Amelio is Senior Partner of Sienna Ventures, Sausalito, CA, and is responsible for leading the firm's emerging technology investments. Gil received his BS, MS, PhD in physics from the Georgia Institute of Technology. He is the author of "On The Firing Line" and "Profit From Experience: The National Semiconductor Story of Transformation Management".

Gil has served as CEO and Chairman of Apple Computer Corp.; President, CEO and Chairman of National Semiconductor Corp.; and President of Rockwell Communication Systems, a unit of Rockwell International Corp.

Gil is a former Director and Chairmen of the Semiconductor Industry Association; he has served on the Board of Governors of the Electronics Industries Association and as a member of the Executive Committee of the Business and Higher Education Forum. His current and past Directorships include SBC Communications, Pacific Telesis Corp., Chiron Corp., Sematech, American Film Institute, and Chairman of the Georgia Institute of Technology Advisory Board.

Gil is a Fellow in the Institute of Electrical and Electronic Engineers (IEEE) and has been awarded 16 patents. Gil has been the recipient of the Albert Einstein Award for lifetime achievement in the technology industry, the FIU Entrepreneur of the Year Award, and the Masara Ibuka Consumer Electronics Award.

Summer Colloquia

- July 30, 2001 "ORINOCO—Low Power Algorithms, Low Power Architectures" by Professor Wolfgang Nebel, Computer Science Department, Oldenburg University, Germany
- August 2, 2001 "FLYSIG—A Fast Reconfigurable Asynchronous Architecture for Multimedia Applications" by Professor Achim Rettberg, Cooperative Computing and Communications Laboratory, University of Paderborn, Germany
- August 8, 2001 "Embedded System Design and Energy Optimization" by Professor Naehyuck Chang, School of Computer Science and Engineering, Seoul National University, Korea
- August 8, 2001 "Low Energy Intra-Task Voltage Scheduling Using Static Timing Analysis" by Professor Jihong Kim, School of Computer Science and Engineering, Seoul National University, Korea
- August 17, 2001 "Object Oriented Specification of System-on-Chip in SystemC" by Professor Wolfgang Rosenstiel, University of Tuebingen, Germany
- August 31, 2001 "Evaluation of VLSI Architectures" by Professor Walter Stechele, Institute for Integrated Circuits, Munich University of Technology, Germany

Invited Tutorial

Professor Nikil D. Dutt was invited to present an embedded systems tutorial titled "What's New in Compilers for Embedded Systems?" at the XIV Symposium on Integrated Circuits and System Design (SBCCI-2001) held in Brazilia, Brazil on September 10—13, 2001.

Embedded Systems Certificate Program

Under the leadership of Professor Rajesh K. Gupta, UCI University Extension is now offering a certificate program in Embedded Systems Design. This Embedded Systems Design curriculum is targeted for engineering professionals with education and/or industrial experience in circuit or system design but who are new to the specific challenges of designing embedded systems. The Embedded Systems Design curriculum comprises the following 30 hour courses: Embedded Hardware Design Concepts, Real-Time Embedded Systems Programming, Modeling Concepts for Embedded Systems Design, Real-Time Embedded Digital Signal Processing, Real-Time Operating Systems for Embedded Applications, and System Design Methodologies. Students successfully completing 150 course hours will be awarded a certificate in Embedded Systems Design from UCI University Extension.

Visitation

Professor Luciano Lavagno, University of Udine, Italy, University of California, Berkeley and Cadence Berkeley Laboratory visited CECS on July 25, 2001. He was hosted by Professor Rajesh K. Gupta.

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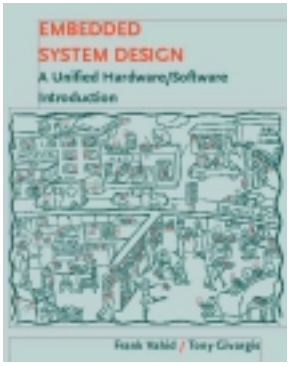
was associated with the System Performance, Modeling, and Simulation (SYSPERF) Group and reported to Nasr Ullah. He was working with the architecture design team on micro-architectural modeling and simulation of a new microprocessor in the PowerPC family using EXPRESSION tools developed at CECS. His assignments included performing micro-architectural design space exploration experiments to provide early performance and power estimations for the new architecture. Srikanth's research at CECS is being supervised by Professor Nikil D. Dutt.

Xilinx Donation

Professor Tony Givargis recently received a donation from Xilinx, Inc. consisting of 25 software licenses for their Xilinx Foundation Synthesis tools ($62,3745 market value) and 25 XS40 FPGA + Microcontroller boards ($8,725 market value). The donated software and hardware will be used to give undergraduate students hands-on experience designing embedded systems. The XS40 boards have integrated a number of components on a single board; eg. Xilinx FPGA, 8051 microcontroller, memory, and input/output devices. The boards can be used to execute applications that are hardware (mapped to FPGA) and software (mapped to 8051) based. CECS is extremely grateful to Xilinx, Inc.for their support of our educational activities in embedded systems.

New Book



"Embedded System Design: A Unified Hardware/Software Introduction" authored by Professor Frank Vahid and Professor Tony Givargis was published by John Wiley and Sons, Inc. in October 2001. In today's world, embedded systems are everywhere — homes, offices, cars, factories, hospitals, planes, and consumer electronics. Their huge numbers and new complexity call for a new design approach, one that emphasizes high-level assembly language programming and logic design. This exciting new book presents the traditional distinct fields of software and hardware design in a new unified approach. It covers trends and challenges, introduces the design and use of single-purpose processors (hardware) and general-purpose processors (software), describes memories and buses, illustrates hardware/software tradeoffs using a digital camera example, and discusses advanced computation models, control systems, chip technologies, and modern design tools.

Distinguished Lecture

On September 27, 2001, Professor Daniel D. Gajski delivered an ECE Distinguished Lecture at the University of Toronto, Toronto, Canada. His lecture was titled: "System Level Design: What is happening, what should be happening, and what should not". His lecture presented recent trends in design and methodology for System-on-Chip (SoC), including specification capture, design exploration with reuseable cores, and hardware/software codesign. Presently, there are many academic and industrial efforts in defining system-level design languages and methodologies that include new and legacy intellectual properties (IP). His lecture compared some of the hot technology concepts and he discussed the pros and cons in languages, tools, and methodologies. He also discussed recent experiments on selected design examples and the resulting productivity gains.

Strategic National Panel

Professor Nikil D. Dutt participated in a National Science Foundation Workshop on "New Directions in Compiler Technology" in Annapolis, MD on September 5 - 7, 2001. This strategic national workshop was organized by Dr. Fredica Darema, Director of the Next Generation Software Program at the National Science Foundation. This workshop was aimed at determining future research directions for compiler and systems software technology. Professor Dutt presented an embedded systems perspective and outlined challenges in compiler research for embedded systems.

CANDE Charts EDA's Future

Professor Rajesh K. Gupta, outgoing IEEE CANDE Chairman, was quoted in an article titled "CANDE Charts EDA's Future" that appeared on the front page of the October 3, 2001 issue of EE Times. CANDE, which stands for Computer-Aided Network Design, members recently gathered for a weekend retreat in a remote mountain resort near Jackson Hole, WY to talk about next generation EDA design challenges. Some of CANDE's 2001 predictions are:

- ASIC design styles will largely be replaced by programmable platforms
- Hardware/software codesign is irrelevant—the real problem is one of mapping system functions into programmable sources
- Power consumption considerations will dominate high-end and portable designs
- Speech recognition will become a major function of electronic systems
- An integration of synthesis, placement, and routing will replace point tools
- Signal integrity will displace timing closure as the dominant design implementation problem
- The language question will remain unresolved for the foreseeable future

Annual CANDE EDA predictions go back for over 2 decades. To review the EDA history, please visit the CANDE web site at: *www.cande.net*.

Research Grants

- Professor Rajesh K. Gupta received an additional increment of funding for $65,790 to cover research costs through May 31, 2002 on U. S. Air Force Research Laboratory (AFRL) contract titled "Power Aware Distributed Systems".
- Professor Rajesh K. Gupta received a 2001-2002 MICRO titled "Coordinated Course Grain and Fine Grain Optimizations for High-Level Synthesis" valued at $75,000 of which the Intel Corporation will provide $50,000. Mike Kishinevsky will serve as the Intel sponsor.

Professor Profile

CECS is proud to profile Associate Professor Bruce J. Tromberg, College of Medicine, University of California, Irvine (UCI), as an outstanding research affiliate. Professor Tromberg received a BA from Vanderbilt University in 1979 and a PhD in chemistry from the University of Tennessee in 1988. He has been a professor at UCI since 1990 and currently holds a joint appointment in the Department of Electrical and Computer Engineering.. In 1998, he was a Visiting Professor at the Institute of Applied Optics, Swiss Federal Institute of Technology, Lausanne, Switzerland.

Professor Tromberg is the recipient of the following awards: OE Magazine Technology Innovator Award (2001); Coherent Young Investigator Award in Biophotonics (2001); Cornelius Hopper Innovation Award, California Breast Cancer Research Program (1999); Avon Foundation Breast Cancer Research Scholar (2000—present); National Institute of Health FIRST Award (1994—1999); Whitaker Foundation Young Investigator Award (1992—1995) and the Hewitt Foundation Postdoctoral Fellow, Beckman Laser Institute (1988—1990).

The following are some of Professor Tromberg's most recent publications:

- "Sources of Absorption and Scattering Contrast for Near-Infrared Optical Mammography", A. E. Cerussi, A. J. Berger, F. Bevilacqua, N. Shah, D. Jakubowski, J. Butler, R. F. Holcombe, B. J. Tromberg, Academic Radiology, Vol. 8, pp 211—218, 2001
- "Non-Invasive Functional Optical Spectroscopy of Human Breast Tissue", N. Shah, A. Cerussi, C. Eker, J. Espinoza, J. Butler, J. Fishkin, R. Hornung, B. J. Tromberg, Proceedings of the National Academy of Science, Vol. 98, pp 4420—4425, 2001
- "Influence of Optical Properties on Two-Photon Fluorescence Imaging in Turbid Samples", A. K. Dunn, V. P. Wallace, M. Coleno, M. W. Berns, B. J. Tromberg, Applied Optics, Vol. 39, pp 1 –8, 2000

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Graduate Student Profile

CECS has selected Sumit Gupta to be profiled as an outstanding graduate student. He was born in Bhilai, India and received a Btech from the Indian Institute of Technology, Delhi, India in 1995. Following graduation he did a short stint with IBM India and then joined a start-up company, Think-It, working on architecture design and implementation of a multimedia microprocessor targeted at the PC add-in card market. He enrolled as a graduate student at UCI in 1997. During the summer of 1998, he was an intern at IMEC, Leuven, Belgium, and during the summer of 2001, he was an intern at Intel, Inc., Hillsboro, Oregon.

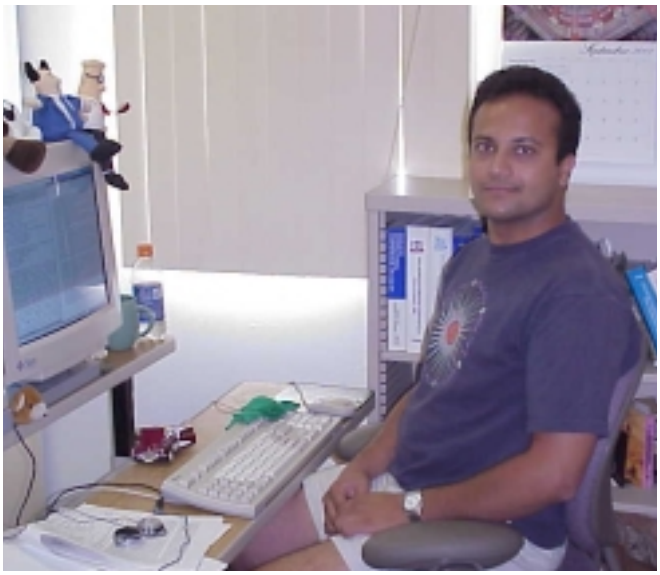
His PhD research is focused on utilizing parallelizing compiler techniques for high-level synthesis and is being supervised by Professor Rajesh K. Gupta. He is a co-author of a high-level synthesis framework, called SPARK, which takes as input a behavioral description in ANSI-C and outputs synthesizable RTL in VHDL. This research is exploring various synthesis optimizations and their effects on final netlist results. He is the co-author of the following technical publications:

- "Conditional Speculation and Its Effects on Performance and Area for High-Level Synthesis", S. Gupta, N. Savoiu, N. D. Dutt, R. K. Gupta, A. Nicolau, International Symposium on System Synthesis, October 2001

- "Speculation Techniques for High-Level Synthesis of Control Intensive Designs", S. Gupta, N. Savoiu, S. Kim, N. D. Dutt, R. K. Gupta, A. Nicolau, Design Automation Conference, June 2001

- "Analysis of High-Level Address Code Transformations for Programmable Processors", S. Gupta, M. Miranda, F. Catthoor, R. K. Gupta, Design, Automation and Test in Europe Conference, March 2000

- "Synthesis of Testable TRL Designs Using Adaptive Simulated Annealing Algorithm", C. P. Ravikumar, S. Gupta, A. Jajoo, International Conference on VLSI Design, January 1998



The following were published by CECS faculty affiliates during the period of July 1, 2001 to October 1, 2001:

Focus	Title, Authors, Publication
Concurrent Test	"Concurrent Test for Digital Linear Systems", I. Bayraktaroglu and A. Orailoglu, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 9, September 2001, pp 1132—1142
Control Algorithms	"Specification and Validation of New Control Algorithms for Electric Drives Using SpecC Language", S. Ben Saoud and D. D. Gajski, UCI ICS Technical Report #01-44, July 25, 2001
SpecC Methodology	"SpecC Methodology Applied to the Design of Control Systems for Power Electronics and Electric Drives", S. Ben Saoud and D. D. Gajski, UCI ICS Technical Report #01-45, July 25, 2001
Power Electronics Emulators	"Codesign of Emulators for Power Electronic Processes Using SpecC Methodology", S. Ben Saoud and D. D. Gajski, UCI ICS Technical Report #01-46, July 25 2001
Authentication	"Authentication for Clone-Cyber Entities in Bio-Net Environments", Young I. K. Eum and Tatsuya Suda, UCI ICS Technical Report #01-43
Memory Adaptation	"Memory Adaptation Techniques: A Unified Overview Across benchmark Suites", Haito Du, Paolu D'Alberto, and Rajesh Gupta, UCI ICS Technical Report #01-41, August 13, 2001
Interference Analysis	"Interference Analysis of Parameterized Loop Nests to Determine Optimal Line Size for Direct Mapped Cache", Paola D'Alberto, A. Nicolau, and A. Veidenbaum, UCI ICS Technical Report #01-42
Interoperability	"Interoperability as a Design Issue in C++ Based Modeling Environments", Frederic Doucet, Sandeep K. Shukla, Rajesh K. Gupta and Masato Otsuka, UCI ICS Technical Report #01-53, September 17, 2001
Concurrency Models	"Efficient Usage of Concurrency Models in an Object-Oriented Co-Design Framework", Piyush Garg, Sandeep K. Shukla and Rajesh K. Gupta, UCI ICS Technical Report #01-52, September 17, 2001
Concurrency Reassignment	"Automated Concurrency Reassignment in High Level Systems Models for Efficient System-Level Simulation", Nic Savoiu, Sandeep K. Shukla and Rajesh K. Gupta, UCI ICS Technical Report #01-51, September 17, 2001
Management Strategies	"Competitive Analysis of Dynamic Management Strategies for Systems with Multiple Power Saving States", Sandra Irani, Sasndeep K. Shukla and Rajesh K. Gupta, UCI ICS Technical Report #01-50, September 17, 2001
Power Management Strategies	"A Model Checking Approach to Evaluating System Level Dynamic Power Management Policies for Embedded Systems", Sandeep K. Shukla and Rajesh K. Gupta, UCI ICS Technical Report #01-49, September 17, 2001
Split Level Programming	"Efficient System-Level Co-Design Environment Using Split Level Programming", Frederic Doucet, Masato Otsuka, Rajesh K. Gupta and Sandeep K. Shukla, UCI ICS Technical Report #01-34, July 1, 2001
Low Power Address Encoding	"Low Power Address Encoding Using Self-Organizing Lists", M. Mamidipaka, D. Hirschberg, and N. D. Dutt, Proceedings of ISLPED-01, August 2001
Loop Nests	"Static Analysis of Parameterized Loop Nests for Energy Efficient Use of Data Caches", Paolo D'Alberto, Alexandru Nicolau, Alexander Veidenbaum, and Rajesh Gupta, Proceedings of the Second Workshop on Compilers and Operating Systems for Low Power (COLP'01), Barcellona, Spain, September 9, 2001, pp 11.1—11.7

Organization

Center for Embedded Computer Systems, University of California, Irvine

CECS Mission Statement:

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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RoboToys Galore!

I've been fascinated lately by reading about RoboToys; eg. RoboDogs, RoboCats, RoboFish. There's I-Cybie by Tiger Electronics and Aibo (means "pal" in Japanese) by Sony Electronics that are particularly interesting and intriguing; even to older kids—ha, ha. The companies are releasing them in time for Christmas 2001 hoping to improve their bottom line.

I-Cybie is composed of 1,400 parts, 16 computer controlled motors, coupled with light, touch, sound, and movement sensors all powered by a rechargeable NiCad battery. The voice recognition technology allows you to train this robotic rover by voice or clap commands while the audio technology supports barking and whining. You experience all the normal dog behaviors and are relieved of all the messing dog waste problems. Now that's real FUN!

These RoboToys are fantastic examples of embedded systems for students. Students are fascinated by their functional capabilities. The inquisitive students want to know more about these electromechanical toys so they dissect them; remember Biology class when we dissected a frog. Once inside, they can start to dream about implementing new features. That's what challenging education is all about. Arousing the curiosity in the student and challenging them to create and innovate. RoboToys may be new educational vehicles for students at all ages.

Some day we may be riding down the freeway on a RoboHorse. That will make freeway commuting exciting and fun! Hope I live to see it.

Bob Larsen