Volume 7, Issue 3
July '07

CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights

- CECS at IESS 2007
- NISC Technology
- CECS at DAC 2007
- Heydari wins Guillemin-Cauer Award
- Gorjiara wins Hami and Best Paper Award

Inside this Issue:

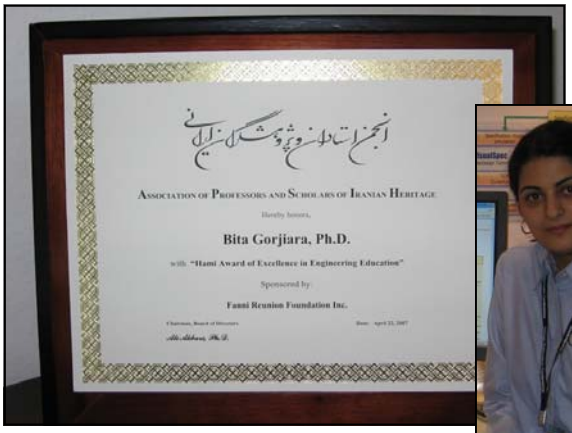
NISC Technology Praised at DAC 2007

CECS-developed No-Instruction-Set-Computer (NISC) Technology is the next generation of tools for Design Synthesis. Before NISC, the designers had to choose between high productivity and high quality but could not achieve both simultaneously. Higher productivity gains are possible through software implementation using a processor, but this option does not lead to high quality results. On the other hand, manual RTL implementation can improve quality but at the cost of increased design time and hence reduced productivity.

Unfortunately, technologies such as High-Level Synthesis (HLS) and Application Specific Instruction-set Processors (ASIP) were unable to deliver on their goals and bridge this gap completely. In

Continued on page 2

Bita Gorjiara Takes Hami and Best Paper Award



Bita Gorjiara has won the prestigious Hami Award of Excellence in Engineering Education for the year 2007. Sponsored by the Fanni Reunion Foundation, the Hami award recognizes outstanding M.Sc. and Ph.D. graduates with a previous degree from University of Tehran. Each year, Hami award is given to one or two students with excellent academic record in terms of GPA, number of publications, and overall contribution in their field of study.

Bita has also received the Best Student Paper Award for her journal paper, "Ultra-Fast and Efficient Algorithm for Energy Optimization by Gradient-based Stochastic Voltage and Task Scheduling," which has also been accepted for publication in ACM Transactions on Design Automation of Electronic Systems (TODAES). This

Continued on page 4

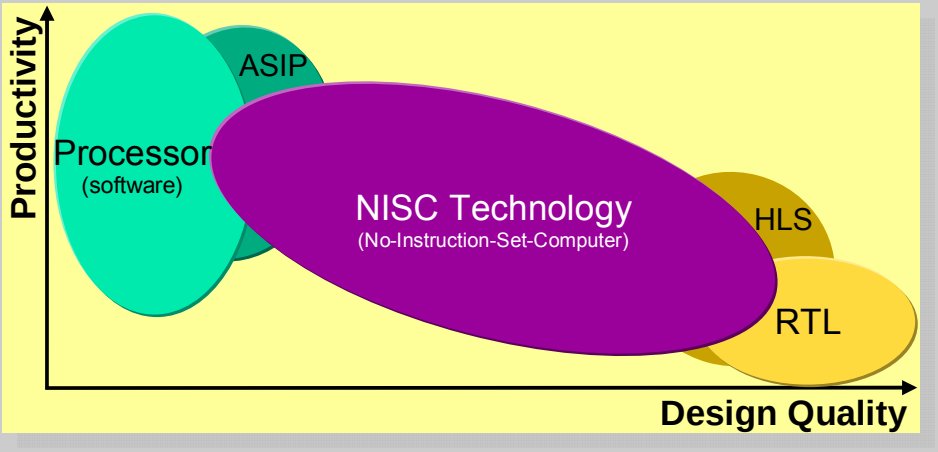
Jelena and Gajski Receive IESS Best Paper Award

Jelena Trajkovic, a PhD candidate in computer science, and Professor Daniel D Gajski, received best paper award at the second International Embedded System Symposium that took place in Irvine, California from May 30th to June 1st 2007. Their paper is titled "Automatic Data Path Generation from C Code for Custom Processors." The paper was selected from over 60 submissions on the basis of technical quality and presentation. The authors of the best paper received an Altera Nios II Embedded Development Kit.

Automatic generation of architectures from C code is a fundamentally novel way of addressing the problem of system design. In traditional design methods, architecture is assumed as fixed for implementing an application. Compilers must then figure out the best mapping of the application on the given architecture. This method may result in poor performance because the given architecture may not carry the best features to execute the application code. Moreover, the architecture may carry features that are

Continued on page 5

NISC Technology:: Cont'd from Front Page



ASIP, a base-processor is "extended" to support application-specific custom instructions. Finding proper custom instructions is a very challenging and time-consuming task. Additionally, since the base-processor is always extended, the designer must always pay for all of the resources of the base-processor even if the application does not use all of them. On the other hand, HLS offers a one-direction path from application (C code) to implementation (RTL). HLS techniques typically can only support a sub-set of language features and can handle small application sizes. Additionally, the designer cannot directly correlate the effect of application modifications to final implementation quality metrics such as area, power, clock frequency, routable layout …. Therefore, the designer can only rely on try and error and guess work for improving the quality. Because of this major drawback, result quality of HLS tools is significantly lower than manual RTL.

NISC technology combines traditional compiler, high-level synthesis, and processor-customization techniques; and provides a single universal technology/toolset for designing IPs ranging from simple components to custom processors in an MPSoC. In addition to application (C code) the designer can also choose to provide the datapath as input to the toolset. Therefore, it is possible to directly control different quality metrics of the final implementation. By providing a predictable path from specification to implementation, NISC technology enables the designers to quickly generate very efficient designs.

For the past several years, the Embedded Systems Methodology Group at CECS has been working on the NISC toolset in order to turn the NISC Technology from an idea into reality. The bulk of the tools are now in a relatively mature state and the main NISC toolset, including a datapath generator, a NISC compiler, and a n RTL generator are now available at NISC Technology website (http://www.cecs.uci.edu/~nisc) for download. An online version of the tools is also available which can be run in any internet browser without requiring any software installation. The tools can generate generic or Xilinx specific Verilog RTL from ANSI C code.

Currently, the NISC Technology comes with the complete set of tools for generating IP blocks to be used in SoCs and embedded systems. These production quality tools have been rigorously tested and have been used in several commercial and research projects worldwide. The tools can be uses as fully functional C-to-RTL as well as custom-processor design toolset. The ESMG has been also informed that the NISC Technology toolset is also being used by a research group in Japan for equivalence checking!

NISC Technology along with two other products of the ESMG was presented in the Design Automation Conference (DAC) of 2007 held in San Diego, CA. Close to 100 experts from industry and academia saw the NISC tools demo and many explicitly expressed that they were impressed by both the concept and the robustness of the tools. Semiconductor companies such as Qualcomm showed interest in using the tools while EDA companies such as Synopsys were interested in collaboration and further development of the technology.

Several people from the press also visited the ESMG booth at DAC. After seeing the NISC demo, John Cooley, the moderator of famous ESNUG newsletter (www.deepchip.com), left the booth saying: "This is very interesting stuff, I will definitely write about it soon!"

CECS Co-Organizes IESS 2007, Runs Successful Conference

The International Embedded Systems Symposium IESS 2007, was held at the Beckman Center at UC Irvine from May 30 to June 1, 2007. Organized by the Computer System Technology committee of the International Federation for Information Processing and co-organized by Rainer Doemer and Andreas Gerstlauer of CECS, the 2007 conference was held in the Beckman Conference Center at UC Irvine. The symposium is a unique forum to present novel ideas, exchange timely research results, and discuss the state of the art and future trends in the field of embedded systems. Over 60 participants from 13 different countries and from both industry and acadamia attended and took active participation in this year's event, making IESS 2007 a truly international and inter-disciplinary conference on various embedded system topics.

Timely topics, techniques and trends in embedded system design were covered in 12 sessions at the conference, including design methodology, specification and modeling, embedded software and hardware synthesis, networks-on-chip, distributed and networked systems, and system verification and validation. Particular emphasis was paid to automotive and medical applications, and a set of actual case studies and special aspects in embedded system design were also included.

The papers presented at this year's conference were the result of a rigorous double-blind review process implemented by the technical program committee. Out of a total of 64 valid submissions, 35 papers had been accepted for publication, yielding an overall acceptance rate of 54.7%. Based upon a strong technical program with 2 keynotes, 2 tutorials, and 1 panel, IESS 2007 was a very fruitful conference.

Payam Heydari Wins Guillemin-Cauer

Payam Heydari, associate professor of electrical engineering and computer science, and a Calit2 academic affiliate at UC Irvine, has won this year's prestigious Guillemin-Cauer Award from the IEEE Circuits and Systems Society. Heydari is also the recipient of the 2005 IEEE Circuits and Systems Society Darlington Award, which puts him in an elite group of only seven researchers who, in the 40-year history of the awards, have received both.

Heydari was recognized for his paper "Model-Order Reduction Using Variational Balanced Truncation with Spectral Shaping," which was published in the IEEE Transactions on Circuits and Systems, Vol. 53, April 2006.

The latest integrated circuit technology – geared to the nanoscale – continues to create new possibilities for designers to substantially reduce chip size and increase speed. The technology, however, also presents challenges, most notably to the yield and reliability of the circuits and on-chip wires.

It is essential to capture statistical fluctuations caused by process variations, but testing such complicated systems can require days of computer simulation. Heydari's approach dramatically reduces the time needed for this statistical modeling from days to just minutes. It significantly reduces the order of the original system while retaining important circuit characteristics, such as frequency and time-domain. Most notably, this technique accounts for statistical variation due to changes in process.

In addition, Heydari's approach provides a proven boundary for error between the reduced order model and the original system. The work has since been the foundation for several key papers published by other researchers on the same topic.

The Guillemin-Cauer Award recognizes the best journal paper published in IEEE Transactions on Circuits and Systems during the two calendar years preceding the award. The award is based on general quality, originality, contributions, subject matter and timeliness.

-By Anna Lynn Spitzer, reprinted from Calit@.net

CECS at 2007 Design Automation Conference

- Rainer Doemer co-organized (together with Wolfgang Ecker from Infineon, Munich, Germany) a workshop on Sunday about " Hardware-dependent Software (HdS)."
- Andreas Gerstlauer and co-authors from UCI and University of Paderborn, Germany, presented a talked about "OS and Processor Modeling."
- Members of CECS presented papers in technical sessions.

IESS Best Paper Award :: Cont'd from Page 2

never used by the application, resulting in wasted power and area. Architecture generation from C code attempts to solve this problem by automatically creating an architecture that "matches" the C code.

In their paper, Jelena and Prof. Gajski present first results for the generation of matching architecture from C code. They address the selection of function units to meet performance goals while maximizing architecture utilization. Their experimental results demonstrate that the architecture could be generated for large C code, including an MP3 decoder with over 14K lines of code, under an hour.

The optimizations improved architecture utilization by 30 to 60 percent while meeting performance constraints.

CECS congratulates the researchers on their achievement and wishes them success in their future endeavors.

Bita Gorjiara Takes Hami and Best Paper Award :: Cont'd from Front Page

paper award is an honor given by the EECS department for first-time authors.

In her paper, co-authored by Professor Bagherzadeh and Professor Chou, Bita proposes an ultra-fast and voltage scheduling algorithm called Adaptive Stocahstic Gradient Voltage-and-Task Scheduling (ASG-VTS) that is used for power optimization of designs with voltage islands. This unique technique was shows to surpass the energy savings of previously published results while reducing number of voltage transitions. Compared to an optimal ILP algorithm, her technique converges 1000 times faster while generating results as good as the optimal solution. She has also developed a web-based tool for her algorithm that allows researchers to capture the model of their system and run ASG-VTS. Research groups use Bita's tool for evaluating new algorithms, and some universities have used as part of their course curriculum.

Currently, and for the past three years, Bita has been working on No-Instruction-Set Computer (NISC) project under supervision of Prof. Gajski. She has developed an Architecture Description Language (ADL) for NISC called GNR that is used for automatic generation of RTL code. She has also proposed techniques to reduce power consumption and code size of NISCs while improving their performance via architecture customization.

Student Profiles

Student Profile

Carmen Badea

Carmen joined the CECS Ph.D. program in Fall 2003 after receiving her M.S. in Computer Science from UCI in March of 2006. She has been working on developing a Java runtime environment targeted for embedded systems and is currently evaluating the energy consumption savings achieved by the Java runtime system.

The Java runtime system employs a technique that combines some of the main benefits of just-in-time (JIT) compilation, superoperators(SOs), and profile-guided optimization in order to deliver a lightweight Java runtime environment targeted for resource-constrained environments. This allows the environment to achieve runtime performance similar to that of state-of-the-art JIT compilers and/or adaptive optimization (AO) systems while having a minimal impact on runtime memory consumption.

The key ideas are to use profile-selected, extended bytecode basic blocks as superoperators (new bytecode instructions), and to perform few but very targeted standard JIT/AO optimizations at compile time only on the superoperators' bytecode, as directed by compilation "hints" passed on as annotations. This way, the proposed system achieves competitive performance for a JIT/AO system, but with a much lower impact on runtime memory consumption. Moreover, due to the superoperators' structure, the aforementioned Java runtime environment is able to further improve upon the achieved runtime performance by selectively inlining method calls embedded in the chosen superoperators (as directed by runtime profiling data) with negligible impact on applications' size.

"I have enjoyed being a graduate student in the CECS group," Carmen says. "Undoubtedly, it has been hard sometimes, having to do research, take classes and exams, and be a Teaching Assistant at the same time, but there are so many great people in CECS who are always willing to help out."

Visitor Profile

Radu Cornea

While at CECS, Radu has worked as part of the FORGE group. His research focuses on power optimizations for multimedia on mobile/embedded devices. In today's world, mobile devices are becoming ubiquitous and increasingly more powerful, enabling a range of new multimedia-rich applications. But, all these come at a price: lower battery. This limitation negatively impacts the user experience. In his PhD research, Radu has looked at ways through which information extracted from the multimedia content (especially video) can help to decrease the power consumption during video streaming and reduce quality loss. The techniques Radu has developed with the help of his advisor, Prof. Alex Nicolau, and his co-advisor, Prof. Nikil Dutt, work by pre-processing the multimedia stream and annotating the profiled data back to the stream. During the actual video playback, this annotated data is used to drive more aggressive power management techniques, which take advantage of the extra knowledge of the content in the video stream to reduce power consumption. One example is the LCD display, which consumes a large part (one third or more) of a regular handheld device. However, during typical movies, there are parts with a lower overall brightness (dark scenes), during which the LCD backlight can be turned down by a factor while the brightness of the video is increased to compensate. The overall effect achieved is similar to the original unmodified video stream, but with a significant lower power consumption.

Radu joined CECS in 1999 with a BS in Computer Science from "Politehnica" University of Timisoara, Romania. He received his PhD from UCI in Winter 2007 and has enjoyed all the time he's spent at CECS. He has especially liked working with many students and professors from the center as part of his different projects during the years. His experience at CECS has both strengthened his knowledge and increased

Continued on page 7

PUBLICATIONS

The following were published by CECS faculty affiliates from April 2007 to July 2007

Focus	Titles, Author, Publication
Multithreading Processors	Kyueun Yi and Jean-Luc Gaudiot, "Architectural Support for Network Applications on Simultaneous MultiThreading Processors." IPDPS 2007.
Reconfigurable Array Template	Akira Hatanaka, Nader Baghe rzadeh, "A Modulo Scheduling Algorithm for a Coarse-Grain Reconfigurable Array Template," IPDPS 2007.
NoC Architecture	Jun Ho Bahn, Seung Eun Lee, Nader Baghe rzadeh, "Design and Analysis of a Feasible Network-on-Chip(NoC) Architecture," ITNG 2007.
Hybrid Power Estimation	"Mohammad Ali Ghodrat, Kanishka Lahiri, Anand Raghunathan, "Accelerating System-on-Chip Power Analysis Using Hybrid Power Estimation," DAC 2007.
Data Reuse Driven Memory	Ilya Issenin, Nikil Dutt, "Data Reuse Driven Memory and Network-on-Chip Co-Synthesis," IESS 2007.
Resource-Constrained Embedded Processors	Carmen Badea, Alexandru Nicolau, Alexander Veidenbaum, "A Simplified Java Compilation System for Resource-Constrained Embedded Processors", TR 07-03, June 2007.
Automatic Data Path Generation	J. Trajkovic, D. Gajski, "Automatic Data Path Generation from C code for Custom Processors," IESS 2007.
NISC Technology	B. Gorjiara, M. Reshadi, D. Gajski, "Low-Power Design with NISC Technology", J. Henkel, S. Parameswaran, Designing Embedded Processors: A Low Power Perspective, Springer, ISBN: 978-1-4020-5868-4, April 2007.

Student Profile :: Cont'd from Page 6

his interest in the embedded systems' world.

After graduation, Radu accepted a position at Google (Mountain View) as a Software Engineer in the Search Quality group and became a member of the Google Alerts team. As part of his 20% project at Google, Radu plans to use the expertise in power optimization that he's developed during his research at CECS to work on improving power management for the up coming One Laptop Per Child project (OLPC), a low cost Linux-based laptop targeted at children in developing nations.

CECS—*promoting creativity and pursuing discovery!*

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

Primary Contact
Leila Mironova
Center for Embedded Computer Sciences
University of California, Irvine
Email: Lmironov@uci.edu

Botnets

Several factors have combined to dramatically increase the significance of the embedded system security problem and the need for computer security research. Our society has become dependent on the use of networked embedded systems for all manner of endeavor, even in cost-critical and life-critical applications. At the same time, the number of attacks on computers has skyrocketed. Automated attack tools have enabled the growth of massive ``botnets'' which are groups of computers whose operating systems have been completely compromised by rootkits. These botnets, which can control thousands of computers, are leveraged to perform all manner of large-scale network attacks, including simple spam, DDoS attacks, click fraud, and port redirection.

The mechanisms which enable the vast majority of computer attacks are based on design and programming errors in software. Software security involves the protection of software which interacts with a network, either directly or indirectly. We investigate the use of security testing as a method to detect security vulnerabilities in software.

An embedded application area which we are investigating is voice over IP (VOIP) phone technology. VOIP uses the internet to transfer phone call data, as opposed to the separate dedicated copper-based phone network used by traditional phone carriers. Specific threats to VOIP include denial of service, eavesdropping, and voicemail password exposure. We propose the use of security testing to identify vulnerabilities in VOIP phones. Session Initiation Protocol (SIP) is the almost universally accepted standard for establishing calls between VOIP phones. We have developed a security testing tool to generate a sequence of SIP messages designed to reveal security weaknesses in VOIP phones.