CECS eNEWS

Volume 4, Issue 3, July 2004

Center for Embedded Computer Systems, University of California, Irvine

Highlights:

Inside this issue:

CECS at DAC

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7 Papers Presented!

Research affiliates and graduate students from the Center for Embedded Computer Systems (CECS) at the University of California, Irvine (UCI) played a significant technical program role in the success of the 41st Design Automation Conference (DAC) held at the San Diego Convention Center, San Diego, CA from June 711, 2004.

Professor Pai H. Chou served as a member of the Technical Program Committee that evaluated 785 submitted technical papers and accepted 163 technical papers for presentation at the conference.

The following technical papers were presented by CECS research affiliates with the cited pages from the conference proceedings:

- *Extending the Transaction Level Modeling Approach for Fast Communication Architecture Exploration*, Sudeep Pasricha, Nikil Dutt and Mohamed Ben-Romdhane, pp 113—118
- *Leakage Aware Dynamic Voltage Scaling for Real-Time Embedded Systems*, Ravindra Jejurikar, Cristiano Pereira and Rajesh Gupta, pp 275—280
- *Retargetable Profiling for Rapid, Early System-Level Design Space Exploration*, Lukai Cai, Andreas Gerstlauer and Daniel Gajski, pp 281—286
- *Proxy-Based Task Partitioning of Watermarking Algorithms for Reducing Energy Consumption in Mobile Devices*, Arun Kejariwal, Sumit Gupta, Alexandru Nicolau, Nikil Dutt and Rajesh Gupta, pp 556—561
- *Automatic Generation of Equivalent Architecture Model from Functional Specification*, Samar Abdi and Daniel Gajski, pp 608—613
- *Introduction of Local Memory Elements in Instruction Set Extensions*, Partha Biswas, Vinay Choudhary, Kubilay Atasailay Atasu, Laura Pozzi, Paolo Ienne and Nikil Dutt, pp 729—734
- *Dynamic FPGA Routing for Just-in-Time FPGA Compilation,* Bita Gorji-Ara, Roman Lysecky, Frank Vahid and Sheldon X.-D. Tan, pp 659—662

Professor Daniel Gajski served as a panelist at a session titled *Were the Good Old Days all That Good? EDA Then and Now.*

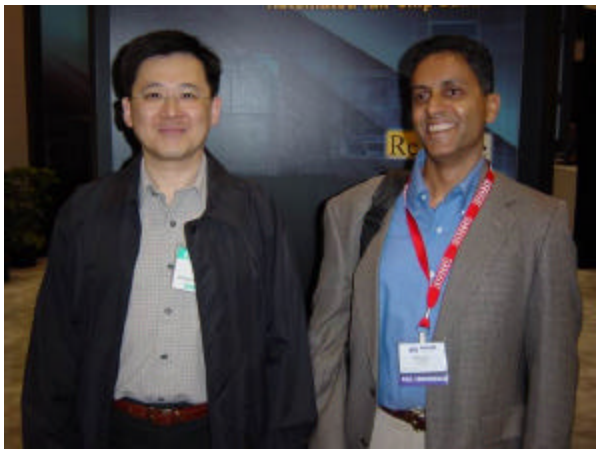
These mentioned CECS research affiliates and their graduate students made substantial contributions to the technical program and organization of this year's 41st Design Automation Conference (DAC). CECS is expecting to continue its significant technical and organizational influence of next year's conference which will be held at the Anaheim Convention Center on June 13-17, 2005. Hope to see you there!

CECS Alumni at DAC Exhibits

Dr. Tedd Hadley (PhD '95), CEO
Y Explorations, Inc., Lake Forest, CA

Dr. Peter Grun (PhD '01), Engineering Manager
Axys Design Automation, Inc., Irvine, CA

A San Diego "June gloom" landscape



Professor Allen C-H Wu (PhD '92), Tsing Hua University, Taiwan and Professor Nikil Dutt enjoying the DAC exhibits

Graduate student Mehrdad Reshadi and Dr. Prabhat Mishra (PhD '04) enjoying a lunch break. Dr. Mishra will become an Assistant Professor at the University of Florida, Gainesville, FL effective July 15, 2004.

Introducing Prof. Harris

Assistant Professor Ian G. Harris, Department of Computer Systems, Donald Bren School of Information and Computer Sciences, University of California, Irvine has become a research affiliate of the Center for Embedded Computer Systems. Professor Harris was born in Brooklyn, NY and received a BS from Massachusetts Institute of Technology in 1990 and an MS and PhD from the University of California, San Diego in 1992 and 1997, respectively. From 1997 to 2003 he served as an assistant professor at the University of Massachusetts, Amherst, MA in the Department of Electrical and Computer Engineering.

Professor Harris received the Ben Dasher Best Paper Award for the paper titled *Educational Innovations in Multimedia Systems*, W. Burleson, A. Ganz, and I. G. Harris at the ASEE/IEEE Frontiers in Education Conference in 1999; the University of Massachusetts CES Faculty Award in 2002; and the IEEE Computer Society Certificate of Appreciation in 2003.

Professor Harris has served as General Chair, North Atlantic Test Workshop (NATW), Program Chair, International Test Synthesis Workshop (ITSW), and Program Chair, Workshop on High Level Design Validation and Test (HLDVT).

Professor Harris's research interests are in the areas of hardware-software covalidation, behavioral validation, testing of FPGA architectures, and pseudo-random built-in self-test (BIST).

Some of Professor Harris's most recent publications are:

- *Application of Built-in Self-Test for Interconnect Testing of FPGAs*, D. A. Fernandes and I. G. Harris, IEEE International Test Conference, September 2003
- *Fault Models and Test Generation for Hardware-Software Covalidation*, I. G. Harris, IEEE Design and Test of Computers, July-August 2003
- *ATPG for Timing Errors in Globally Asynchronous Locally Synchronous Systems*, S. Arekapudi, F. Xin, J. Peng and I. G. Harris, Journal of Circuits, Systems and Computers, Vol. 12, No. 3, June 2003, pp 305-332
- *Partial BIST Insertion to Eliminate Data Correlation*, Q. Zhang and I. G. Harris, IEEE Transactions on Computer-Aided Design, March 2003
- *Fast Computation of Data Correlation Using BDDs*, Z. Zeng, Q. Zhang, I. G. Harris and M. Ciesielski, IEEE Design and Test in Europe Conference (DATE), February 2003

Professor Harris will live in University Park when his new house is completed in December with his wife Jennifer and sons Dakari and Kyler.

ISLPED Open House

The International Symposium on Low Power Electronics and Design (ISLPED) is being held in Newport Beach, CA on August 9-11, 2004. CECS is inviting all ISLPED attendees to an Open House on Sunday evening, August 8, 2004 from 5:00 PM to 8:00 PM on the 3rd floor of the IERF Building. We are planning a buffet of sandwiches, cookies, and soft drinks which will create an atmosphere to promote technology exchanges. Many of our research affiliates and graduate students will present posters of their research projects and be available for informal exploratory technology and research discussions.

For those attending ISLPED, kindly consider attending this open house to see first hand our research programs and visit with our graduate students and professors. Please visit our web site at *www.cecs.uci.edu* to purchase a virtual ticket (only joking) and obtain directions to our facility on the UCI campus. We are planning an informal environment and hope you will attend and enjoy the CECS hospitality.

Cassen Addresses Palm Springs Area Radio Club

On April 15, 2004, Quentin C. Cassen, Director of Research Relations, and long-time licensed radio amateur, addressed the Greater Palm Springs Area Chapter of the Quarter Century Wireless Association, Inc. (QCWA) at the Palm Desert Greens Country Club in Palm Desert, CA. With about 30 members in attendance, Cassen discussed *The Evolution of Embedded Computing*. Following his presentation, Dr. Gene Pentecost, Chapter President, presented Cassen with an award and certificate commemorating fifty years of distinguished service as a licensed radio amateur. Quent's call letters are W6RI.

In his address, Cassen described the impact embedded computer systems have made on the world, beginning with their first use in calculators and toys in the 1960's and growing in their pervasiveness year by year since then. He went on to explain Moore's Law (doubling the number of transistors on a chip every couple of years), which has increased silicon performance while reducing manufacturing costs for almost forty years. Embedded computer systems have significantly impacted automotive, communications, and medical applications for the benefit of the individual and society over these years. Although we will see billion-transistor chips (SoC) within a year or two, Cassen described ongoing research in smart dust—tiny wireless sensors intelligent enough to organize themselves into autonomous networks.

Congratulations Quent on accomplishing this longevity milestone as a licensed radio amateur!

Gajski Hosts Japanese Visitors

On June 14 and 15, 2004, Professor Daniel Gajski hosted six Japanese researchers visiting CECS for technical discussions. These researchers represented the Japan Aerospace Exploration Agency (JAXA), Tokyo, Japan, InterDesign Technologies, Inc., Tokyo, Japan and the University of Tokyo. The picture on the right portrays these visitors and their respective affiliations.

There ain't no rules around here!
We're trying to accomplish something!

Thomas Edison

Pictured above in the UCI Chancellor's Rose Garden, from left to right: Dr. Dai Araki, Vice President—Technology Development, InterDesign; Professor Masahiro Fujita, The University of Tokyo; Keizo Nakagawa, Senior Engineer, Information Technology Center, JAXA; Professor Daniel Gajski, CECS Director, UCI; Setsuo Yamamoto, President & CEO, InterDesign; Professor Rainer Doemer, UCI; Masanobu Tsuji , Associate Senior Engineer, Information Technology Center, JAXA; and Atsushi Nakamura, Senior Engineer, InterDesign.

CECS Students Receive PhD

Several CECS graduate students proudly marched in the UCI Commencement held June 19, 2004. The following graduate students were awarded their Doctor of Philosophy (PhD) degree:

Lukai Cai, April 12, 2004: Thesis: "Estimation and Exploration Automation of System Level Design", Advisor: Professor Daniel Gajski

Andreas Gerstlauer, May 5, 2004: Thesis: "Modeling Flow for Automated System Design and Exploration", Advisor: Professor Daniel Gajski

Prabhat Mishra, March 19, 2004; Thesis: "Specification-Driven Validation of Programmable Embedded Systems", Advisor: Professor Nikil Dutt

Junyu Peng, June 7, 2004, Thesis: "System-Level Automatic Model Refinement", Advisor: Professor Daniel Gajski

Dongwan Shin, April 29, 2004, Thesis: "Communication Synthesis for System-on-Chip", Advisor: Professor Daniel Gajski

Congratulations to these new doctoral graduates and we wish them all extremely successful careers in education or industry.

Gajski Receives Award

Professor Daniel D. Gajski received the first ever 2004 Graduate Mentor of the Year Award from the Donald Bren School of Information and Computer Sciences. This award was given in recognition of his devotion to graduating 4 PhD students in 2004 and 4 PhD students in 2003.

Congratulations Dan on receiving this award which was richly deserved for your many years of dedication in mentoring your graduate students.

If you want to increase your success rate, double your failure rate.

Thomas Watson
IBM Founder

New SpecC Reference Compiler Released

Professor Rainer Doemer announced the release of a new version of the SpecC Reference Compiler (SCRC), Version 2.0, on June 24, 2004. The SCRC V2.0 includes the following new features:

? Full support of the SpecC Language Standard Version 2.0

? Standard SpecC Channel Library included

As always, the SCRC source and binary software packages can be freely downloaded from the CECS web site at: www.cecs.uci.edu/~specc/reference/.

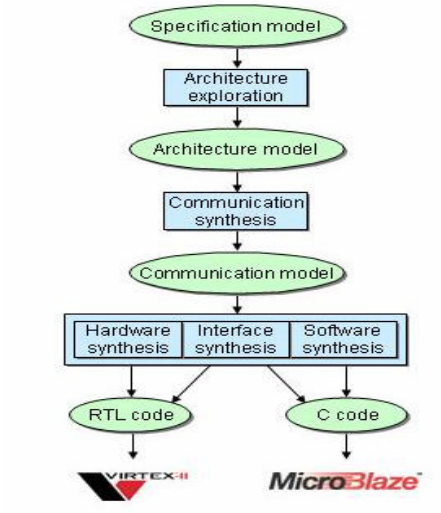
More information on the SpecC design language and methodology and the SCRC V2.0 can be found on the CECS web site at: www/cecs/uci/~specc/ and the SpecC Consortium web site at: www.specc.org.

"One Day" FPGA Design Methodology

Visiting Researcher Takaaki Imai, Design Engineer, Automotive Business Group, Renesas Technology Corporation, Tokyo, Japan had an idea—rapid FPGA synthesis to support customer prototyping of embedded systems.

This conceptual idea kept nagging him until he took action. So he contacted Professor Daniel Gajski to explore the idea further. He also was discussing the idea with Renesas management. Everyone liked the idea so he was able to convince his management to allow him to become a Visiting Researcher at CECS. He arrived at CECS in August 2003 to commence a one year research program under the guidance of Professor Gajski. After nearly a year of research, his idea is becoming a reality.

Using Gajski, et al's System-on-Chip Environment (SCE) methodology (see CECS *eNEWS* January 2002 page 5) as a foundation of his research, he has developed a coupling to a FPGA prototyping system. The Xilinx Corporation had donated a HW-v2000-MTA Microblaze/Multimedia board and Microblaze Developers Kit to CECS in October 2003 through its University Program. In simple terms, this is a Xilinx board and development software which includes the Microblaze soft microprocessor. This synergistic coupling has led to the development of a "one day" FPGA design methodology.



"One Day" FPGA Design Methodology

The design flow starts from the system executable specification which leads to a model defining the system behavior. The system architecture is then generated and modeled from this system behavior. Finally a communications model is developed to satisfy intermodule communications requirements. Now hardware, interface, and software synthesis can proceed using conventional synthesis tools. SCE's RTL design environment for the allocated hardware of the system provides synthesis refinement and exploration for the RTL design. SCE also includes a tool for creating ANSI C code for allocated software of the system. This tool has functions such as task creation, task code generation, and operating system targeting. Considering these desirable features, SCE is the most suitable design framework and methodology for rapid FPGA prototyping of embedded systems.

SCE can be coupled to the Xilinx Microblaze Developers Kit very easily. Implementing SCE generated RTL/C codes on a FPGA embedded platform, the generated RTL code can be validated with those generated by logic synthesis. Metrics such as speed, power consumption, and area can be compared. The generated C code can be also evaluated from the point of view of practical issues such as performance, code size, and cooperation with the allocated hardware of the designed system.

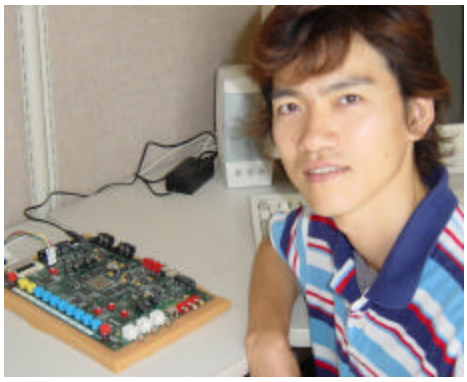
The technology difference between FPGAs and ASICs is becoming much less obvious. The programmable feature of FPGAs allows for rapid evaluate of different system design configurations. Utilizing his automotive experience, Takaaki has developed two technology drivers to test the "One Day" FPGA Design Methodology. The complexity of automotive embedded systems has continuously increased. Today's BMW 760Li is the ultimate electronics driving machine.

The first example centers on automobile infotainment systems such as a GPS-guided car navigation system or a rear-seat DVD entertainment system. The primary function of the automotive navigation system is to calculate the current vehicle position and portray a 3D graphics road map on a high resolution LCD. The road map data is usually stored in a hard disk drive. These many features of an automobile navigation system can be implemented in an SoC configuration.

The second example is in automotive control systems such as engine, transmission, and brake systems. These various control units are connected via a control network (CAN, LIN, FlexRay) and execute their functions individually and cooperatively. This means the designers must focus not only on the computational capabilities of each control unit but also on the communications among control units in the distributed in-vehicle network.

Raising the level of design abstraction from RTL has been proposed as a means of increasing designer productivity. To achieve this productivity goal, each abstraction level and its design model needs to be well defined. As the model fidelity increases, automatic model refinement under the control of the designer is paramount.

In the SCE methodology, higher abstraction levels and design models are clearly defined and different design models are integrated vertically by synthesis technology. This means that the designer's target specification can be transformed into an equivalent RTL model automatically on the basis of the designer's decisions. This vertical design flow enables the synergistic coupling of traditional FPGA design flow with the SCE methodology thus enabling a "one day" FPGA design methodology.



Takaaki Imai received a Bachelor and Master of Engineering Science from Osaka University in 1995 and 1997, respectively. He has been associated with Hitachi, Ltd and Renesas Technology Corp. for 6 years designing 2D/3D graphics accelerators embedded in SoC for Automotive Information Systems.

PUBLICATIONS

The following were published by CECS faculty affiliates during the period of April 1, 2004 to June 30, 2004:

Focus	Title, Authors, Publication
Transaction Level Modeling	*Extending the Transaction Level Modeling Approach for Fast Communication Architecture Exploration*, Sudeep Pasricha, Nikil Dutt and Mohamed Ben-Romdhane, Proceedings of the 41st Design Automation Conference (DAC), June 7-11, 2004, pp 113—118
Voltage Scaling	*Leakage Aware Dynamic Voltage Scaling for Real-Time Embedded Systems*, Ravindra Jejurikar, Cristiano Pereira and Rajesh Gupta, Proceedings of the 41st Design Automation Conference (DAC), June 7-11, 2004, pp 275—280
Retargetable Profiling	*Retargetable Profiling for Rapid, Early System-Level Design Space Exploration*, Lukai Cai, Andreas Gerstlauer and Daniel Gajski, Proceedings of the 41st Design Automation Conference (DAC), June 7-11, 2004, pp 281—286
Task Partitioning	*Proxy-Based Task Partitioning of Watermarking Algorithms for Reducing Energy Consumption in Mobile Devices*, Arun Kejariwal, Sumit Gupta, Alexandru Nicolau, Nikil Dutt and Rajesh Gupta, Proceedings of the 41st Design Automation Conference (DAC), June 7-11, 2004, pp 556—561
Architecture Model	*Automatic Generation of Equivalent Architecture Model from Functional Specification*, Samar Abdi and Daniel Gajski, Proceedings of the 41st Design Automation Conference (DAC), June 7-11, 2004, pp 608—613
Local Memory Elements	*Introduction of Local Memory Elements in Instruction Set Extensions*, Partha Biswas, Vinay Choudhary, Kubilay Atasailay Atasu, Laura Pozzi, Paolo Ienne and Nikil Dutt, Proceedings of the 41st Design Automation Conference (DAC), June 7-11, 2004, pp 729—734
FPGA Routing	*Dynamic FPGA Routing for Just-in-Time FPGA Compilation*, Aviral Bita Gorji-Ara, Roman Lysecky, Frank Vahid and Sheldon X.-D. Tan, Proceedings of the 41st Design Automation Conference (DAC), June 7-11, 2004, pp 659—662
Procrastination Scheduling	*Procrastination Scheduling in Fixed Priority Real-Time Systems,* R. Jejurikar and R. Gupta, UCI CECS Technical Report 04-09, April 2004
Optimized Slowdown	*Optimized Slowdown in Real-Time Task Systems,* R. Jejurikar and R. Gupta, UCI CECS Technical Report 04-10, April 2004
Rapid Exploration	*Rapid Exploration of Bus-Based Communication Architectures at the CCATB Abstraction,* S. Pasricha, N, Dutt and M. Ben-Romdhane, UCI CECS Technical Report 04-11, May 2004
Synchronization Errors	*On the Detection of Synchronization Errors*, I. G. Harris, UCI CECS Technical Report 04-13, May 2004
Energy Minimization	*Systemwide Energy Minimization in Real-Time Embedded Systems*, R. Jejurikar and R. Gupta, UCI CECS Technical Report 04-14, May 2004
Network Synthesis	*Network Synthesis for SoC*, D. Shin, A. Gerstlauer and D. Gajski, UCI CECS Technical Report 04-15, June 10, 2004
Communication Link Synthesis	*Communication Link Synthesis for SoC*, D. Shin, A. Gerstlauer and D. Gajski, UCI CECS Technical Report 04-16, June 10, 2004
SoC Modeling, Design	*System-on-Chip Modeling and Design: A Case Study on MP3 Decoder*, P. Chandraiah, H. Schirner, N. Srinivas and R. Doemer, UCI CECS Technical Report 04-17, June 21, 2004

CECS—Solving Tomorrow's Problems!

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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R U a CECSer?

CECSer

What is a *CECSer*? It is a person or organization dedicated to promoting the CECS research programs—graduate students, professors, and sponsors. If we don't have an ideal balance between these three groups, we fail to attain our desired pinnacle of research success.

Graduate Students

Our graduate students are the paramount source of our research creativity. Graduate students are energetic and eager to learn new technical disciplines and constantly questioning the conventional theories and practices. They possess an academic foundation that prepares them for exploring and experimenting with proposed hypotheses. This attitude is essential and vital to our research programs if we desire to impact the individual and society in the future. Graduate students are the eyes and ears of CECS and its research programs!

Professors

Our professors are the main source of our research exploration, student mentoring, and project management. Professors organize and develop graduate students into cohesive teams to explore meaningful topics and document their conclusions for all to comprehend. They motivate and question graduate students in a manner that develops their full investigative skills to accomplish and complete research tasks in a timely manner. Professors are the brain of CECS and its research programs!

Sponsors

Our sponsors are the primary source of our research support. They are the fuel for our research programs; primarily technology drivers and monetary funding. Sponsors also provide our graduate students with insightful engineering experiences through summer internships. Without their financial support our "Lego-style" core and domain research programs would collapse. Sponsors are the heart of CECS and its research programs!

CECS Needs You!

Teamwork

Our commitment to research excellence in embedded systems requires teamwork between our graduate students, professors, and sponsors. *Teamwork makes the technology dream work*. Please join our research team and become a proactive *CECSer*!

Bob Larsen