CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

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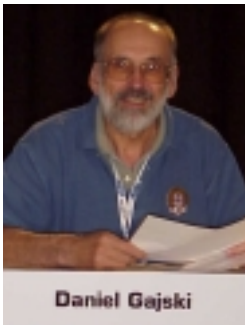
CECS at DAC 2001

The Center for Embedded Computer Systems (CECS) at UC Irvine had a significant presence at the 38th Design Automation Conference in Las Vegas, Nevada held June 18-22, 2001.

PANEL

Professor Rajesh K. Gupta was chair of the panel titled "The Next HDL: If C++ is the Answer, What Was the Question?". The panel was characterized by strong views supporting and opposing the use of C++ as a high-level design language to an audience of over 850 attendees. The White Team presented positions supporting C++ as an HDL.



The chief argument of the White Team was based on the intrinsic advantages of C++ with its flexibility to model complex systems consisting of diverse components and models of computation. With Professor Daniel D. Gajski leading the charge, the Blue Team, systematically tore through the supporting arguments. "We need semantics before syntax, abstraction before modeling, guidelines before language" said Gajski to a very attentive and participatory audience.

PAPER

Graduate Student Sumit Gupta presented a paper titled "Speculation Techniques for High Level Synthesis of Control Intensive Designs" authord by Sumit Gupta,

Nick Savolu, Sunwoo Kim, Nikil Dutt, Rajesh Gupta, and Alex Nicolau. He discussed the effectiveness of various types of code motions, such as moving operations across conditionals, out of conditionals (speculation) and into conditionals (reverse speculation), and how they can be effectively directed by heuristics so as to lead to improved synthesis results in terms of fewer execution cycles and fewer number of states in the finite state machine controller.

PAPER

Graduate Student Ismet Bayraktaroglu presented a paper

titled "Test Volume and Application Time Reduction Through Scan Chain Concealment" authored by Ismet Bayraktaroglu and Alex Orailoglu. He discussed a test pattern compression scheme that utilizes an on-chip decompressor which dramatically reduces the test data volume and application time.

PAPER

Graduate Student Peter Petrov presented a paper titled "Speeding

Up Control-Dominated Applications Through Microarchitectual Customizations in Embedded Processors" authored by Peter Petrov and Alex Orailoglu. He discussed a methodology for microarchitectural customization of embedded processors by exploiting application information, thus attaining the twin benefits of processor standardization and application-specific customization.

PAPER

Graduate Student Jinfeng Liu presented a paper titled "Power-

Aware Scheduling under Timing Constraints for Mission-Critical Embedded Systems" authored by Jinfeng Liu, Pai H. Chou, Nader Bagherzadeh, and Fadi

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DAC 2001 Keynote

Since CECS has several research associates who are faculty members of the Samueli School of Engineering, we take great pride in acknowledging Dr. Henry Samueli's keynote address at the 38th Design Automation Conference on June 19, 2001. Dr Samueli is Co-Chairman and Chief Technical Officer of Broadcom Corporation, Irvine, CA. His address was titled: "Designing in the New Millennium: It's Even Harder Then We Thought".

Peggy Aycinena, a writer covering the EDA industry summarized his presentation as follows: "In a muscular tour de force, Broadcom Corp. Co-Chairman and CTO Henry Samueli held his audience spellbound as he swiftly review the history of electronic design, the academic initiatives that led to seminal breakthroughs in the technology, the various business models that have dominated the semiconductor industry over time, today's increasingly voracious demand for connectivity bandwidth, the nature of design teams in the past, present, and future, as well as the emerging landscape for system-level design. He ended with a primer for the design tool vendors that articulated everything they must do to meet their customer's needs and to guarantee continued prosperity for the EDA industry. In short, it was a thorough and succinct presentation, elegantly compressed into 45 minutes."

CECS is extremely fortunate to have an industrial titan of Dr. Samueli's stature as an affiliate of the Samueli School of Engineering.

DAC 2001 Best Paper Award

At the 38th Design Automation Conference, Professor Chris Papachristou, Department of Electrical and Computer Engineering, Case Western Reserve University, Cleveland, OH, received the 2001 Best Paper Award, in the category of Design Methodology, for the technical paper titled: "Improving Bus Test via IDDT Testing and Boundary Scan" co-authored with his graduate student Massood Tabib-Azar. This paper describes a mixed-signal test scheme to detect bus interconnect faults.

Professor Papachristou has been a research collaborator with Professor Daniel D. Gajski and Professor Alex Orailoglu in the past. Congratulations Chris, on receiving this prestigious DAC award which acknowledges creativity and excellence in your testing research.

DAC 2001 Reception

Professor Rajesh K. Gupta, Chair of the Computer Aided Network Design Committee (CANDE), a technical committee of the IEEE Circuits and Systems Society (CAS), was chairman of the June 19, 2001 evening reception honoring Dr. Aart de Geus, Chairman and CEO, Synopsys, Inc., Mountain View, CA as recipient of the 2001 CAS Industrial Pioneer Award for pioneering logic synthesis. Dr. de Gues was President of CANDE in 1990-1991.

Visitations

- Masaki Ito and Yoshio Takamine, Systems LSI Research Department, Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan visited Professor Nikil D. Dutt on June 4, 2001.
- Paul Kritzinger, System Architect, Semiconductor Products Sector, Motorola, Inc., Austin, TX visitied Professors Daniel D. Gajski, Nikil D. Dutt, and Alex Nicholau on June 25, 2001.
- Assistant Professor Jianwen Zhu, Department of Electrical and Computer Engineering, University of Toronto, Toronto, Canada visited Professor Daniel D. Gajski on June 26 and 27, 2001.
- Chris Fitzsimmons, Project Manager, and Mack Lee, Product Application Engineer, Conexant Systems, Inc., Newport Beach, CA visited Professor Nikil D. Dutt on June 27, 2001.

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Kurdahi. He discussed a new scheduling technique for supporting the design and evaluation of a class of power-aware systems in mission-critical applications. The Mars Rover was used as an example of how the new scheduling technique can improve performance and reduce energy costs.

UNIVERSITY BOOTH

Graduate students of Professors Pai H. Chou, Nikil D. Dutt, Rajesh K. Gupta, and Alex Nicolau, held poster sessions in the University Booth which allowed conference attendees to visit and discuss their research projects.

PhD FORUM

Professor Pai H. Chou was the organizer and host of the PhD Forum held on June 19, 2001. This was an evening session that allowed industrial representatives to become acquainted with PhD candidates and discuss their research activities.

Power Aware Distributed Systems (PADS)

Power Aware Distributed Systems (PADS) is a collaborative research effort with USC Information Sciences Institute, UCLA, UCI, and Rockwell Science Center. The project is funded under the DARPA ITO PAC/C program. The general goal is to provide a framework for assessment of power-aware design strategies on a sensor network environment. Design strategies for intranode power-aware management and network-wide power-aware management will be provided so that a trade-off between quality and energy can be performed.

The UCI research program, under the direction of Professor Rajesh K. Gupta, is focusing on the development of intranode power-aware management techniques. For this, the real-time operating system (RTOS), which manages local computation and communication resources, is the logical place for making power management decisions. Essential components comprising the RTOS power management are: (1) power-aware resource scheduling in RTOS which relates to a power efficient use of the processor, I/O, and other subsystems, (2) energy-speed control knobs and energy-accuracy control knobs which enables the assessment of energy-speed and/or energy-accuracy trade-offs, and (3) tools for RTOS power management evaluation and power-aware RTOS kernel synthesis which will allow the user to evaluate how a specific RTOS and power management scheme will perform on a given task set from a power perspective.

Research Grants

Professor Rajesh K. Gupta was awarded a National Science Foundation (NSF) Basic Research Grant of $218, 958 for 3 years titled: "Constrained Power/Performance Optimization for Embedded Systems".

Compute Farm

The compute farm comes to CECS!

Recognizing the timely need to migrate from single machine processors to distributed clusters, Professor Rajesh K. Gupta's group is building a compute farm with SUN Blade 100 machines. In its first phase, the group has built an 8 machine cluster to support the ever increasing demand for computational power generated by his research activities. This compute farm, will be used primarily for compute-intensive simulation, synthesis, and verification activities related to embedded systems research. Each SUN Blade 100 machine is powered by a 500MHz UltraSPARC IIe processor with 1 GB RAM and 15GB hard disk. The cluster is running a NIS+ domain that enables a single login password and a single home directory which is ideal for large, compute-intensive, problem solving. Most remarkably, the compute farm is being administered by his Graduate Students Sumit Gupta and Dan Nicolaescu.

Colloquium

Professor Wolfgang Nebel, Computer Science Department, Oldenburg University, Germany, will deliver a lecture titled "ORINOCO—Low Power Algorithms, Low Power Architectures" on Monday, July 30, 2001 at 3:00 PM in CECS Conference Room 127.

ORINOCO is a tool suite for power estimation and optimization of C++ and VHDL descriptions at the behavioral and architectural design levels. Power consumption in embedded systems is increasingly becoming a design constraint. Battery life and reliability of products are demanding sever power savings. Increases in frequency and circuit density will continue to raise the natural power demands of systems. Until recently, tool support for high-level power design techniques was rudimentary. ORINOCO bridges the gap between system specification and low power implementation. It works directly on the C++ or VHDL description and provides support for power aware system partitioning, algorithm selection, and architecture.

This colloquium is open to all interested engineers.

Semantics Workshop 2001

Professor Daniel D. Gajski is a member of the organizing committee for the Semantics Workshop 2001 to be held at the University of California, Irvine campus on November 1 and 2, 2001. The Call for Papers is inviting paper submissions in the following areas:

1) Applications of the RTL semantics definitions
2) Semantic models for other domains of computation
3) Methods for defining semantics
4) Semantics for higher levels of abstraction

The Semantics Workshop 2001 is being sponsored by Accellera.

Colloquium

Professor Achim Rettberg, Cooperative Computing and Communication Laboratory, University of Paderborn, Germany, will deliver a lecture titled "FLYSIG - A Fast Reconfigurable Asynchronous Architecture for Multimedia Applications" on Thursday, August 2, 2001 at 2:00 PM in CECS Conference Room 127.

The FLYSIG (data Flow oriented delaY-insensitive SIGnal processing) architecture is based on a delay insensitive style with bit-serial operator implementation. Therefore, FLYSIG is a fast reconfigurable asynchronous architecture for multimedia applications. The asynchronous architecture reflects the data flow characteristics of such multimedia applications. As an example, the DCT/IDCT algorithms are realized. These algorithms are used for MPEG encoding and decoding. Only one operator network of different asynchronous components is used to map the DCT and the IDCT on it. Furthermore, first simulation results of VHDL models shows the effectiveness of the approach.

This colloquium is open to all interested engineers.

Professor Profile

CECS is proud to profile Professor Alex Orailoglu, Department of Computer Science and Engineering, University of California, San Diego (UCSD), as an outstanding research affiliate. Professor Orailoglu received the SB *cum laude degree* from Harvard University in 1977 and the MS and PhD degrees from the University of Illinois in 1979 and 1983. He has been a professor at UCSD since 1987 and currently is director of the Reliable Systems Synthesis Group. He is currently supervising 7 PhD students and 2 MS students.

Professor Orailoglu has recently served on the follow conference program committees: International Test Conference, IEEE VLSI Test Symposium, International Test Synthesis Workshop, Design Automation Technical Event in Europe (DATE), and Brazilian Symposium on Integrated Circuit Design.

The following are some of Professor Orailloglu's most recent publications:

- "Low-Cost, Software-Based Self-Test Methodologies for Performance Faults in Processor Control Subsystems", S. Almukhaizim, P. Petrov, and A. Orailoglu, Proceedings of the IEEE Custom Integrated Circuits Conference, May 6-9, 2001
- "Test Volume and Application Time Reduction Through Scan Chain Concealment" I. Bayraktaroglu and A. Orailoglu, Proceedings of the 38th Design Automation Conference, June 18-22, 2001, pp 151-155
- "Speeding Up Control-Dominated Applications Through Microarchitectural Customizations in Embedded Processors", P. Petrov and A. Orailoglu, Proceedings of the 38th Design Automation Conference, June 18-22, 2001, pp 512-517

Visitor Profile

CECS has been very privileged to host a Fulbright Scholar, Assistant Professor Slim Ben Saoud, Department of Electrical and Computer Engineering, National Institute of Applied Sciences and Technology, Tunisia, as a visiting researcher. Professor Ben Saoud was born in Menzel-Temime, Tunisia and received his BSEE from the National Higher Educational Engineering College, Toulouse, France in 1993 and the MS and PhD degrees from the Polytechnic National Institute, Toulouse, France in 1993 and 1996. He was appointed an Assistant Professor in 1997. His research interests are in the general areas of embedded systems design for control electronics and fault diagnosis of power electronics and electromechanical systems.

While at CECS, Professor Ben Saoud has been performing embedded systems research under the guidance of Professor Daniel D. Gajski. His research has been focused on developing a real-time electromechanical emulator for validating digital power controllers and performing failure diagnosis.

Professor Ben Saoud and his family will return to Tunisia in mid-August 2001 and CECS has been proud to host this outstanding Fulbright Scholar.

The following are some of Professor Ben Saoud's most recent publications:

- "Parallel Architectures Applied to Real Time Emulation" ,S. Ben Saoud, J. C. Hapiot, IEEE International Conference on Industrial Electronics, Control and Instrumentation, October 22-28, 2000, pp 1719—1724
- "ASIC Dedicated to Real Time Emulation", S. Ben Saoud, J. N. Contensou, J. C. Hapiot, IEEE International Symposium on Diagnostics for Electrical Machines, Power Electronics, and Drives, September 1-3, 1999
- "Universal Emulator of Static Converter/Electrical Machines/Sensor Sets. Test of New Control Unit", S. Ben Saoud, B. Dagues, J. C. Hapiot, Computational Engineering in Systems Applications, April 1-4, 1998

Professor Introduction

CECS is delighted to introduce Assistant Professor Tony D. Givargis, Department of Information and Computer Science, University of California, Irvine (UCI), as a new research affiliate. Professor Givargis was born in Tehran, Iran and received the BS and PhD degrees from the University of California, Riverside in 1997 and 2001. He recently joined the Department of Information and Computer Science at UCI on July 1, 2001. At UCR, he received the Department of Computer Science Best Thesis Award, the UCR College of Engineering Outstanding Student Award, and was the recipient of the GAANN Graduate Fellowship, a MICRO Fellowship, and a Design Automation Conference Scholarship.

Professor Givargis's research interests include embedded and real-time system design, low power design, and processor/system-on-chip (SoC) architectures. He is the co-author of the book titled "Embedded System Design: A Hardware Software Introduction" published by John Wiley & Sons, 2001.

The following are some of Professor Givargis's most recent publications:

- "System-Level Exploration for Pareto-Optical Configurations in Parameterized System-on-Chip" T. D. Givargis, F. Vahid, and J. Henkel, Proceedings of the International Conference on Computer-Aided Design (ICCAD), November 2001
- "Power Consumption of Parameterized Cache and Bus Architectures in System-on-Chip Designs", T. D. Givargis, F. Vahid, and J. Henkel, IEEE Transactions on Very Large Scale Integrated Systems, Vol. 9, No. 4, August, 2001
- "Trace-Driven System-Level Power Evaluation of System-on-Chip Peripheral Cores", T. D. Givargis, F. Vahid, and J. Henkel, Proceedings of the Asia South Pacific Design Automation Conference (ASP-DAC), January, 2001
- "Parameterized System Design", T. D. Givargis and F. Vahid, Proceedings of the International Workshop on Hardware/Software Codesign (CODES), San Diego, May 2000

UC LEAD Scholar

Rafael Lopez, an undergraduate student in Computer Science and Engineering at the University of California, Riverside, was selected as a UC LEAD Scholar and has chosen to study with Professor Nikil D. Dutt, who will serve as his research mentor. The UC LEAD (Leadership Excellence through Advanced Degrees) program is designed to identify promising undergraduate students and provide them with educational and research experiences that prepare them to assume positions of leadership in industry, government, and academia following completion of a doctoral degree. This summer, Rafael is conducting a research project with Conexant Systems, Inc. that investigates the feasibility of using an existing cordless telephone chipset for low data rate wireless transmission using Digital Spread Spectrum (DSS) technology. CECS is pleased to have this outstanding undergraduate student visiting for the summer and hope his research experience at CECS will be rewarding and profitable in his career development.

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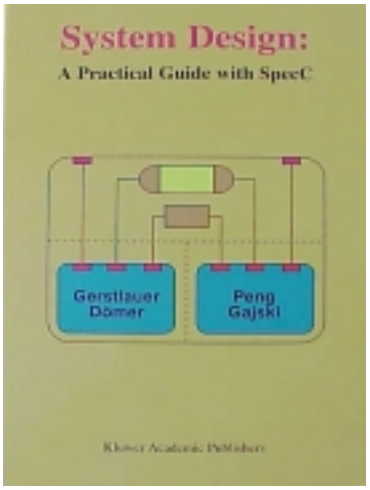
Book

Kluwer Academic Publishers has recently published a new book titled "System Design: A Practical Guide with SpecC", authored by Gerstlauer, Dömer, Peng, and Gajski. This book will benefit designers and design managers of complex SoCs, or embedded systems in general, by allowing them to develop new methodologies from these results, in order to increase design productivity by orders of magnitude. The design models in the book define IP models and functions for IP exchange between IP providers and their users. A well-defined design methodology, like the one presented in the book, will help product planning divisions to quickly develop new products or derive completely new business models, like e-design or product-on-demand.



The following were published by CECS faculty during the period of April 1, 2001 to July 1, 2001:

Focus	Title, Authors, Publication
Power-Aware Scheduling	"Power-Aware Scheduling Under Timing Constraints for Mission-Critical Embedded Systems," J. Liu, P. Chou, N. Bagherzadeh, F. Kurdahi, Proceedings of the 38th Design Automation Conference, June 18-22, 2001, pp 840-845
Speculation Techniques	"Speculation Techniques for High Level Synthesis of Control Intensive Designs," S. Gupta, N. Savoiu, S. Kim, N. Dutt, R. Gupta, A. Nicolau, Proceedings of the 38th Design Automation Conference, June 18-22, 2001, pp 269-272
Test Volume Reduction	"Test Volume and Application Time Reduction Through Scan Chain Concealment," I. Bayraktaroglu, A. Orailoglu, Proceedings of the 38th Design Automation Conference, June 18-22, 2001, pp 151-155
Control Dominated Applications	"Speeding Up Control-Dominated Applications Through Microarchitectural Customizations in Embedded Processors," P. Petrov and A. Orailoglu, Proceedings of the 38th Design Automation Conference, June 18-22, 2001, pp 512-517
Self-Test Methodologies	"Low-Cost, Software-Based Self-Test Methodologies for Performance Faults in Processor Control Subsystems," S. Almukhaizim, P. Petrov and A. Orailoglu,Proceedings of the IEEE Custom Integrated Circuits Conference, May 6-9, 2001
Visual Refinement and Exploration Tool	"Development of a Visual Refinement and Exploration Tool for SpecC," D. Berner, D. Jansen, D. Gajski, UCI ICS Technical Report #01-12, March 30, 2001
Enhanced Full Rate Vocoder	"Development of a Specification Model of the EFR Vocoder," M. von Weymarn, UCI ICS Technical Report #01-35, July 02, 2001
Timing/Power Analysis	"High-Level Timing and Power Analysis of Embedded Systems", Dinesh Ramanathan, UCI ICS Technical Report #01-24, May 18, 2001
Conditional Speculation	"Conditional Speculation and its Effects on Performance and Area for High-Level Synthesis", S. Gupta, N. Savoiu, N Dutt, R. Gupta, A. Nicolau, UCI ICS Technical Report #01-25, June 2001

Organization

Center for Embedded Computer Systems, University of California, Irvine

CECS Mission Statemnet:

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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DAC = BIG MAC

I just returned from the 38th Design Automation Conference in Las Vegas, NV. I arrived in Las Vegas expecting to be dazzled by all the new design automation technology. All day Monday I spent on the exhibition floor attending many presentations for which I received a small gift. Eventually I needed a tote bag to carry all the gifts.

When I returned home, I gave the tote bag to my 7 year old grandson, Matthew. He asked: "How did you get all these gifts?". I told him that I sat through sales presentations and then they gave me a gift. He said: "That sounds like McDonalds!".

At first I thought this was a silly childish response. But the more I thought about Matthew's response the more profound it became to me. All the designers I talked to still complained about managing design complexity and design closure problems; e.g. timing , noise, and low power estimation, and verification and testing inefficiencies. I now realize that DAC 2001 treated us all to a marketing show with very very little innovative technology. Matthew was right: DAC was like a BIG MAC. All marketing!

What do you think about DAC 2001? Send me your provocative and succinct comments and we will publish them in the next eNEWS. Please don't embarrass me with no responses. Let's communicate!

Bob Larsen