CECS eNEWS

Highlights

- Love Singhal gets FPL '06 Best Paper Award

- CECS Holiday Party

- CECS says good-bye to IERF

Love and Eli Take FPL'06 Best Paper Award

Love Singhal, a Ph.D. candidate in computer science, and professor of computer science Eli Bozorgzadeh received the Best Paper Award at the 2006 IEEE International Conference on Field Programmable Logic and Applications (FPL'06) that took place in Madrid, Spain, August 28-30 2006. The awarded paper is titled "Multi-layer Floorplanning on a Sequence of Reconfigurable Designs".

The dynamic partial reconfigurability of programmable devices such as FPGAs is characterized by their ability to reconfigure subsets of their logic and routing resources at runtime. This intrinsic dynamic reconfiguration results in accommodation of complex and dense designs, on-fly adaptivity, and design modification. Reconfigurable module can be

Good-bye to the IERF Building

The IERF Building will be torn down in January to make way for the new Engineering III building. The IERF has served as a pleasant space for the CECS faculty, staff, and students to meet. CECS held a small gathering to say good-bye.

NEWS

Good-bye IERF :: Continued from Front Page

**CECS is organizing and supporting the
IESS Conference,
May 29—June 1, 2007 at the Beckman Center in Irvine.**

**Call for papers below
Deadline to submit is
December 20, 2006**

CONFERENCE THEME:
Over recent years, embedded systems have gained an enormous amount of processing power and functionality. Many of the formerly external components can now be integrated into a single System-on-Chip. This tendency has resulted in a dramatic reduction in the size and cost of embedded systems. As a unique technology, the design of embedded systems is an essential element of many innovations. Embedded systems meet their performance goals, including real-time constraints, through a combination of special-purpose hardware and software components tailored to the system requirements. Both the development of new features and the reuse of existing intellectual property components are essential to keeping up with ever demanding customer requirements. Furthermore, design complexities are steadily growing with an increasing number of components that have to cooperate properly. Embedded system designers have to cope with multiple goals and constraints simultaneously, including timing, power, reliability, dependability, maintenance, packaging and, last but not least, price.

EVENTS

Love & Eli Take Best Paper Award :: Cont'd from Front Page

a new coprocessor implemented on a FPGA device, an upgraded implementation of the existing module, or a reconfigured memory block. However, partial reconfiguration comes with the cost of reconfiguration overhead delays. In order to reduce the reconfiguration overhead, two consecutive similar sub-designs should be placed in the same locations to get the maximum reuse of common components.

In this paper, a new multi-layer sequence-pair-based floorplanner is proposed for a given sequence of reconfigurable designs. In the experi-

ments, compared to a traditional sequential floorplanner, the new floorplanner removes infeasibility in many designs, and provides faster timing closure.

FPL is the first and largest conference on programmable logic which encompasses a wide range of research area on FPGAs, including applications, novel system architectures and CAD tools, embedded processors, dynamic recon figuration, etc. The acceptance rate in FPL 2006 was 28 percent, out of 307 submissions.

CECS/SER Christmas Party

● **May Garden** ● **November 11, 2006** ● **Relaxation and good food for all** ●

PROJECT PROFILES

Extracting Design Architecture from C Code
:: Submitted by Jelena Trajkovic

With shrinking time to market and tighter product performance constraints, system designers are struggling to deliver application specific, high quality designs within narrow time frames. With application C code becoming the de-facto starting point for almost all design projects, the natural question that is raised is: "What is the best architecture to execute a give C application?"

Ph.D. candidate Jelena Trajkovic and her adviser Prof. Daniel Gajski are developing a new technology to answer exactly this question. They have developed efficient and scalable algorithms to automatically generate RTL datapath from C code. This technique is very important since engineers in application domains such as aerospace, automotive, medical diagnostics, multimedia and consumer electronics write algorithms in C but they do not have sufficient knowledge in system design or computer architecture to create an optimal implementation platform for their applications.

Although there are myriad C to RTL techniques and several commercial offerings, the state of the art falls far short of rapidly growing design requirements. The CECS researchers are providing a fresh approach to the C to RTL problem by extracting architecture from application C code for NISC technology where datapath is driven directly by control words residing in a control memory. This approach provides the designer with three key advantages over traditional design. Firstly, the architecture is generated automatically for any size or any complexity of the C code.

Synthesizable Universal Bridge for MpSoC
:: Submitted by Hansu Cho

Current embedded systems require more processing power and have higher design complexity; therefore, multi-processor systems-on-chip (MPSoC) design at higher level of abstraction is essential. The Transaction Level Model (TLM) is one of the higher level abstraction models widely used for this purpose. In the TLM, systems are composed of the computational units and the communicational units. The communicational units are mapped into the bus wires and the universal bridges; hence, automatic synthesis of the universal bridge is necessary to generate MPSoC from the TLM. The universal bridge is a key component to make MPSoC. It not only translates one bus protocol to the other protocol, it also synchronizes one processor with the other. From a processor's point of view, the universal bridge can be seen as shared memory with interrupt controller and interface converter. Therefore any kinds of processors can communicate through the universal bridge and it makes heterogeneous MPSoC design very easy. On the other hand, the universal bridge can be seen as a router. In MPSoC, there can be multiple paths between two processors, so the universal bridge has to select one path. This decision can be made by PE (static routing) or by universal bridge (dynamic routing). These are described in the TLM. The universal bridge synthesis tool takes the TLM in XML format and the protocol library as inputs. The TLM has all information about routing, synchronization, arbitration, data transfer, and transducer structure. The protocol library describes the bus I/O signals and timing diagram in finite state machine format. The tool analyzes the TLM and generates synthesizable Verilog codes. By using the universal bridge synthesis tool, the system designer can be free from the communicational unit design. All communication between processors can be described using simple send() and recv() functions in TLM, and the tool generates MPSoC communication systems in few seconds from the TLM. Consequently, the system designer can achieve high productivity gain from these benefits.

Profiles

Professor Pai Chou on his experience at a recent ISLPED conference in Germany

"We went to Tegernsee, which was a vacation spot but somewhat far away from the cities. Beer was good but internet was expensive. The weather was nice for a day, but it also turned ugly for a day and a half. The conference attendance was a little lower than expected because the location was remote. We set up a demo although I am not sure how many people got to see it because the scheduling was too tight."

2006 CECS Summer Interns say...

Minyoung Kim

I did a summer internship at the Maude group, SRI (Stanford Research Institute) International. This was an opportunity for me to receive training in formal modeling and analysis. While at SRI, I had opportunities to participate in a broad spectrum of research-related activities, including conducting hands-on research, presenting my work, attending seminars, and interacting with SRI researchers. I worked for the joint project between SRI and UCI. It explores the notion of cross-layer timing in highly distributed embedded systems using a blend of formal methods and experimental systems. Specifically, we (a) developed novel formal methodologies for the modeling, specification, and reasoning about cross-layer timing properties in distributed embedded systems, and (b) designed policies/mechanisms that will cost-effectively address the QoS/performance tradeoffs based on the cross-layer timing analyses.

Jeff Furlong

I was at Emulex Corporation over the summer. I learned a ton of material by hands-on experience in: machine architectures, Operating Systems, embedded systems in the SAN domain, and fibre channel technologies. I designed and configured clusters of servers for automated testing of the company's hardware and software products, and I also presented Python training sessions to the company's engineers. The internship gave me a better understanding of the business part of development, and exposed me to a corporate model.

Mohammad Ali Ghodrat

I was in NEC research lab in Princeton, NJ. There I worked on "Hybrid power estimation". What we did was preparing a hardware-software co-simulation environment for power estimation. We also implemented several synchronization methods between software and hardware to reduce communication overhead.

PUBLICATIONS

The following were published by CECS faculty affiliates from September 2006 to December 2006

Focus	Titles, Author, Publication
Embedded Processors	**"Abstract, Multifaceted Modeling of Embedded Processors for System-Level Design,"** G. Schirner, A. Gerstlauer, R. Dömer: Proceedings of the Asia and South Pacific Design Automation Conference 2007, Yokohama, Japan, January 2007.
Interactive Recoding	*"***Creating Explicit Communication in SoC Models Using Interactive Re-Coding***,"* P. Chandraiah, J. Peng, R. Dömer: Proceedings of the Asia and South Pacific Design Automation Conference 2007, Yokohama, Japan, January 2007.
Duplex AMA-TMS Transducer	**"PBPAIR: An Energy-efficient Error-resilient Encoding Using Probability Based Power Aware Intra Refresh,"** Minyoung Kim, Hyunok Oh, Nikil Dutt, Alex Nicolau, Nalini VenkatasubramanianACM SIGMOBILE Mob. Comput. Commun. Rev. 10(3): 58-69, 2006.
Design Space Exploration	**"Design Space Exploration of Real-time Multi-media MPSoCs with Heterogeneous Scheduling Policies,"** Minyoung Kim, Sudarshan Banerjee, Nikil Dutt, Nalini Venkatasubramanian, IEEE/ACM/IFIP Conference on Hardware/Software Codesign and System Synthesis (CODES-ISSS'06), Oct. 2006, Seoul, South Korea.
Cross Layered Systems	**"Policy Construction and Validation for Energy Minimization in Cross Layered Systems: A Formal Method Approach,"** Minyoung Kim, Nikil Dutt, Nalini Venkatasubramanian, IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS'06) Work-in-Progress Session Apr. 2006, San Jose, CA, USA.
Result Oriented Modeling	**"Fast and Accurate Transaction Level Models using Result Oriented Modeling,"** G. Schirner, R. Dömer, Proceedings of the International Conference on Computer Aided Design, San Jose, California, November 2006.
RTL Modeling	**"Cycle-accurate RTL Modeling with Multi-Cycled and Pipelined Components,"** R. Dömer, A. Gerstlauer, D. Shin Proceedings of the International System-on-Chip Design Conference, Seoul, Korea, October 2006.
Modeling of Real-Time Communication	**"Accurate yet Fast Modeling of Real-Time Communication,"** G. Schirner, R. Dömer, Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis, Seoul, Korea, October 2006.
Transaction-Level Models	**"Automatic Generation of Transaction-Level Models for Rapid Design Space Exploration,"** D. Shin, A. Gerstlauer, J. Peng, R. Dömer, D. Gajski, Proceedings of the International Conference on Hardware/Software Codesign and System Synthesis, Seoul, Korea, October 2006.
Interval Analysis	**"Expression Equivalence Checking using Interval Analysis,"** Mohammad Ali Ghodrat, Tony Givargis, Alex Nicolau, IEEE Transaction on VLSI, Special Section on Hardware/Software Codesign and System Synthesis/, August 2006, pages 830-842

CECS—*promoting creativity and pursuing discovery!*

Center for Embedded Computer Systems, University of California, Irvine

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CECS *Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Published by CECS faculty affiliates from September 2006 to December 2006

Bus-based Communication Architecture

"Floorplan-aware Automated Synthesis of Bus-based Communication Architectures," S. Pasricha, N. Dutt, , E. Bozorgzadeh, M. Ben-Romdhane, in IEEE Transactions on VLSI (TVLSI), Vol. 14, No. 3, March 2006.

Multi-layer Floorplanning

"Multi-layer Floorplanning on a Sequence of Reconfigurable Designs," L. Singhal and E. Bozorgzadeh, in Proc. of IEEE International Conference on Field Programmable Logic and Applications (FPL), Madrid, Spain, 2006. (received the best paper award)

Partially Reconfigurable Architectures

"Physically-aware Exploitation of Component Reuse in Partially Reconfigurable Architectures," L. Singhal and E. Bozorgzadeh. in 13th Reconfigurable Architectures Workshop (RAW'06), Greece, April 2006

CAD Tool for FPGAs

"CAD Tool for FPGAs with Embedded Hard Cores for Design Space Exploration of Future Architectures," S. Dai and E. Bozorgzadeh, in Proc. of IEEE Symposium on Field-Programmable Custom Computing Machine(FCCM),2006.

HARP Routing Pattern

"Statistical Analysis and Design of HARP Routing Pattern FPGAs," G. Wang, S. Sivaswamy, C. Ababei, K. Bazargan, R. Kastner, and E. Bozorgzadeh, to appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), pp.2088-2102, Vol. 25, No. 10, 2006.