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CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights

- CECS presents 3 papers at 2005 CASES Conference
- Welcome, new grads
- Potluck highlights
- CECS at CASES '05

Inside this Issue:

CECS Welcomes New Grad Students

Gabor Madl graduated from Vanderbilt University in Nashville, Tennessee with a degree in Computer Science. His research focuses on the verification and analysis of distributed real-time embedded systems, and he is currently building an open-source framework which captures various QoS properties (e.g. real-time, energy consumption) in a formal setting to provide a way for design and runtime analysis. Gabor is originally from Budapest, Hungary and graduated from the Budapest University of Technology and Economics with a Masters in Computer Engineering. Gabor has recently begun sailing with the UCI Sailing Association and enjoys the beach.

Babak Salamat joins CECS from the University of Technology in Iran where he received his B.Sc in Computer Engineering-Hardware and his M.Sc in Computer Architecture. He is currently working on memory systems of multi-cluster processors under Professor Alexander Veidenbaum to decrease the performance gap between memory systems and processors.

Luis Angel D. Bathen completed his undergraduate studies here at UC Irvine and will now continue his graduate studies with the CECS department. This is Danny's first year as a graduate student and while he does not yet have a research topic, he is working in the area of System Level Modeling. Danny hopes to pursue his research interests in the areas of Design Space Exploration for Embedded Systems, High Level Modeling, Low Power Design, Reconfigurable Computing, Image and Video Processing, and Artificial Intelligence.

Jeff Furlong, originally from Pennsylvania, graduated from Chapman University in Orange. Jeff hopes to develop a specific focus for his research during his time with CECS but is, in the meanwhile, working on smaller projects for system level designs and synthesis operations. When not working, Jeff enjoys poker and golf.

AmirHossein Gholami-Pour finished his B.Sc. at Sharif University of Technology in Tehran, Iran in July 2005 and is working toward his Ph.D. here at UCI. He is researching embedded systems and studying Reconfigurable Architectures and CAD and FPGA architecture optimization, and hopes to contribute to the design of more efficient gadgets that we use on a day-to-day basis (cell phones, PDAs, etc). When not researching, AmirHossein listens to Persian music or "any kind of impressive music—impressive in my own opinion", plays the Setar, and practices Aikido. He also harbors an interest for the Social Sciences and History.

Continued on page 5

Related: read about the grad students' potluck on page 4

Visitor Profile

Munehiro Takimoto

Munehiro is visiting UCI from the Tokyo University of Science in Tokyo, Japan and has joined Alexandru Nicolau's SPARK team of investigators. In fact, it was upon finding Dutt's and Nicalou's *SPARK: A Paralleling Approach to the High- Level Synthesis of Digital Circuits* in a bookstore in Japan that inspired Munehiro's curiosity in parallelizing high-level synthesis methodology. When Munehiro found that the authors of the book all conducted research at UCI he decided to get in contact with them. And now here he is.

SPARK is a C-to-VHDL high-level synthesis framework that employs a set of innovative compilers, parallelizing compiler, and synthesis transformations to improve the quality of high-level synthesis results. The compiler transformations have been re-instrumented for synthesis by incorporating ideas of mutual exclusivity of operations, resource sharing and hardware cost models. The SPARK parallelizing high-level synthesis methodology is particularly targeted to multimedia and image processing applications along with control-intensive microprocessor functional blocks. Munehiro is focusing on the code optimizations of high level synthesis aspect of the project and will work with the team until March 2006.

Meanwhile, Munehiro is taking advantage of his time in California and doing as much sight-seeing as he can. He's been to Sea World and the San Diego Zoo, he's visited Yosemite ("the waterfalls were very beautiful"), an aircraft carrier in Middle Way, and Disneyland. "UCI is the best university in my research area," Munehiro says, then adds, "It is very wild and natural too—trees and bunnies everywhere."

Per Gunner Kjeldsberg

Ph.D. and Associate Professor Per Gunnar Kjeldsberg arrived at UC Irvine from Trondheim, Norway on October 3, 2005 to begin his research on memory optimization and wireless network applications. He will stay until the end of June 2006. Per Gunnar is working closely with CECS affiliate Nikil Dutt and hopes to contribute to the improvement of low power equipment with his research.

Per Gunnar received his Ph.D. in Electrical Engineering at the Norwegian University of Science and Technology (NTNU), where he is now Associate Professor. While working on his Ph.D. he cooperated with the Interuniversity MicroElectronics Center (IMEC) in Leuven, Belgium in researching System Level Design and Hardware/Software Codesign and continues working with them today. As modern electronic systems grow in complexity, system designers are faced with the challenge of shorter development time and lower development cost; Per Gunnar has worked on developing system level tools for optimized design and utilization of memory hierarchies. Per Gunnar is applying his experience with design techniques to his research at UCI. He is working with Nikil Dutt in the area of memory architecture exploration for embedded systems in conjunction with high level modeling of multimedia and wireless network applications.

This is Per Gunnar's first time visiting UC Irvine and he is enjoying his time (and the weather) here. "UCI is a very nice environment with respect to doing good research," Per Gunnar says, "and I like the park."

Selected Publication

- **"Storage Requirement Estimation and Optimization for Data Intensive Application", Doctoral Thesis, Norwegian University of Science and Technology, Defended March 23, 2001**

Project Profile

The Phantom Serializing Compiler

Submitted by Andre Nacul

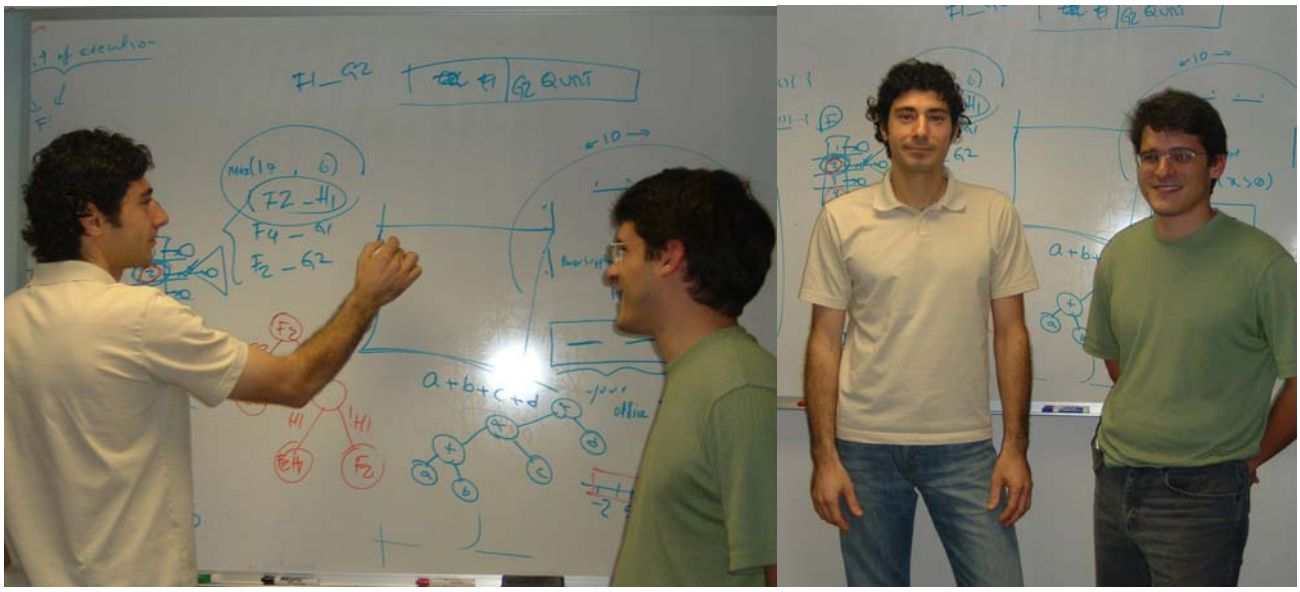
In order to cope with the rapidly raising complexity of embedded systems, engineers are turning to software. In part, well established programming models, highly evolved tool chains, ease of reuse, and expeditious nature of the design-compile-execute paradigm make developing a new feature in software more favorable. It is assumed that, in coming years, more than 70% of product features are going to be supported by software.

Embedded software is characterized by a set of concurrent, deadline-driven, synchronized, and communicating tasks. Hence, embedded software is best captured using the real-time concurrent programming model. The support for real time concurrent programming is usually provided by a real time operating system (RTOS). In general, an RTOS is built as a generic framework, which can be used across a large number of processors and applications. An RTOS provides coarse-grained timing support, and is loosely coupled to the running tasks. As a result, an RTOS, in terms of resource usage efficiency and performance, is seldom optimized for any particular application.

In the Phantom project, we propose an alternative to an RTOS based on the idea of serializing compilers. A serializing compiler is an automated software synthesis methodology that can transform a multitasking application into an equivalent and optimized monolithic sequential code, to be compiled with the embedded processor's native optimizing. The serializing compiler can analyze the tasks at compile time and generate a fine-tuned, application specific infrastructure to support multitasking, resulting in a more efficient executable than one that is intended to run on top of a generic RTOS. By having control over the application execution and context switches, the serializing compiler enables the fine grain control of task timing while enhancing overall performance.

The Phantom Serializing Compiler, our implementation of a serializing compiler, provides a fully automated mechanism to synthesize a single threaded, ANSI C/C++ program from a multithreaded C/C++ (extended with POSIX) program. The Phantom generated code is highly tuned for the input application.

Traditional compilers are good in utilizing platform specific resources, generating an optimized stream of instructions, and exploring pipelines and memory hierarchies. More recently, with VLIW and simultaneous multithreading (SMT) architectures, compilers have started to support the generation of concurrent code. However, compilers have a limited understanding of tasks, and lack support for timing constrained multitasking code. The Phantom serializing compiler technology strengthens existing compilers, making them timing and task-aware, resulting in a more efficient multitasking infrastructure.



Tony Givargis and Andre Nacul

The Phantom Project is supported by a NSF grant and a CAPES Foundation fellowship. More information is available at the project's website, http://www.ics.uci.edu/~nacul/phantom. For questions, comments or feedback, contact André Nácul [nacul@uci.edu].

EVENTS

New Grads Mingle with CECS at Potluck

At the beginning of each new school year CECS puts together an event to welcome its new graduate students. This October the department held a potluck at the University Hills Recreational Area in Irvine and gave faculty, staff, visitors, and new members the opportunity to take a break from the "technical stuff" and enjoy an afternoon of food, sports, and fun conversations.

"As a newcomer, I enjoyed it a lot, because I had the opportunity to know many of the CECS people," new grad student Babak Salamat says of the potluck. "We had very good times together."

"Nothing out of the ordinary happened this time," Tony Givargis, coordinator of the event and CECS faculty member, said, "But it was a lot of fun and I think many of us ate a bit too much."

CECS at CASES Conference, September 2005

*** * * 3 papers presented * * ***

The International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES) was held in San Francisco from September 24 through September 27 of 2005. This year, the conference focused on the complexity of system-level design and its associated challenges and requirements for compilers and architectures.

Every CASES conference provides a forum for emerging technology in embedded computing systems, and allows researchers with an interest in embedded systems to collaborate with each other and promote synergies. Participants in the conference discuss new challenges for embedded systems (such as time-to-time market, cost, code size, and real-time behavior), and strive to find application-specific solutions in embedded areas (such as digital audio/video, imaging, game consoles, and automotive systems).

This year, CECS presented 3 papers at the 2005 CASES conference:

- "Compilation Techniques for Energy Reduction in Horizontally Partitioned Cache Architectures," Aviral Shrivastava, Ilya Issenin, Nikil Dutt.
- "Equivalence Checking of Arithmetic Expressions using Fast Evaluation," Mohammad Ali Ghodrat, Tony Givargis, Alex Nicolau.
- "Single Appearance Schedule with Dynamic Loop Count for Minimum Data Buffer from Synchronous Dataflow Graphs," Hyunok Oh, Nikil Dutt, Soonhoi Ha.

CECS affiliates Fadi Kurdahi, Pai Chou, Tony Givargis, and Nikil Dutt served as members of the CASES Program Committee. Tony Girvargis served also as Session Chair for the Architecture Session.

PUBLICATIONS

The following were published by CECS faculty affiliates from September 2005 to December 2005

Focus	Titles, Author, Publication
NISC Design Flow	"Designing a Custom Architecture for DCT Using NISC Design Flow," B. Gorjiara, M. Reshadi, and D. Gajski, Asian South Pacific Design Automation Conference '06 Design Contest, 2006.
Horizontal and Vertical Parallelism	"Utilizing Horizontal and Vertical Parallelism with No-Instruction-Set Compiler for Custom Datapaths ," M. Reshadi, B. Gorjiara, D. Gajski, International Conference on Computer Design (ICCD), October 2005.
Algorithm for Custom Pipelined Datapaths	"A Cycle-Accurate Compilation Algorithm for Custom Pipelined Datapaths ," M. Reshadi, D. Gajski, International Symposium on Hardware/Software Codesign and System Synthesis (CODES+ISSS), September 2005.
DCT Algorithm	"Design Space Exploration of C Programs Using NISC: A Case-Study on DCT algorithm", B. Gorjiara, D. Gajski, IEEE workshop on Embedded Systems for Real-Time Multimedia, 2005.
Energy Reduction in Cache Architectures	"Compilation Techniques for Energy Reduction in Horizontally Partitioned Cache Architectures," Aviral Shrivastava, Ilya Issenin, Nikil Dutt, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, September 24-27, 2005
Arithmetic Expressions using Fast Evaluation	"Equivalence Checking of Arithmetic Expressions using Fast Evaluation," Mohammad Ali Ghodrat, Tony Givargis, Alex Nicolau, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, September 24-27, 2005
Dynamic Loop Count	"Single Appearance Schedule with Dynamic Loop Count for Minimum Data Buffer from Synchronous Dataflow Graphs," Hyunok Oh, Nikil Dutt, Soonhoi Ha, International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, September 24-27, 2005
Architecture Synthesis	"Bus Matrix Communication Architecture Synthesis," S. Pasricha, N. Dutt, and M. Ben-Romdhane, UCI CECS Technical Report 05-13 October 2005 2005.

One More New Grad

Yonghyun Hwang is at UCI, and in America, for the first time this year. He is originally from Seoul, Korea and graduated from the Korea Advanced Institute of Science and Technology with a Bachelor's degree in Computer Science. He comes to UCI from Seoul National University in Korea with a Master's degree in Computer Science. Yonghyun will be researching design and analysis of distributed real-time embedded systems and jogging and swimming in the meanwhile.

Publication, as mentioned on page 2

SPARK: *A Parallelizing Approach to the High-Level Synthesis of Digital Circuits.* Sumit Gupta, R.K. Gupta, N.D. Dutt, A.Nicalou. Kluwer Academic Publishers.

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Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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