



# CECS eNEWS



Volume 5, Issue 1, January 2005

Center for Embedded Computer Systems, University of California, Irvine

## Highlights:

- CECS at ICCAD
- CECS at Cal-(It)<sup>2</sup>
- Gajski Addresses Local IEEE
- Dutt Named Editor-in-Chief
- Briggs Delivers Lecture
- Kurdahi to IEEE Fellow
- Chou Wins CAREER

## Inside this issue:

|                  |   |
|------------------|---|
| Main Story       | 1 |
| News             | 2 |
| Publications     | 4 |
| Editor's Comment | 5 |

## CECS at ICCAD

Research affiliates and graduate students from the Center for Embedded Computer Systems (CECS) at the University of California, Irvine (UCI) presented four technical papers at the International Conference on Computer Aided Design (ICCAD) held at the Double Tree Hotel, San Jose, CA from November 7–11, 2004. Several research affiliates served on conference committees or as session moderators.

### Papers

The following technical papers were presented by CECS research affiliates with the cited pages from the conference proceedings:

- *Optimizing Mode Transition Sequences in Idle Intervals for Component-Level and System-Level Energy Minimization*, Jinfeng Liu, and Pai H. Chou, pp 21–28
- *Code Partitioning for Synthesis of Embedded Applications with Phantom*, André Costi Năcul and Tony Givargis, pp 190–196
- *Frugal Linear Network-Based Test Decompression for Drastic Test Cost Reductions*, Wenjing Rao, Alex Orailoglu, and George Su, pp 721–725
- *Design Space Exploration for Aggressive Test Cost Reduction in Circular Scan Architectures*, Baras Arslan and Alex Orailoglu, pp 726–731

### Session Moderators

Professor Nikil D. Dutt served as moderator of a session titled *Application Specific Memory and Processor Architecture Design Techniques* and Professor Tony Givargis served as a moderator of a session titled *Architectural Is-*

*sues in System Synthesis.*

### Committees

Professor Nikil D. Dutt served on the ICCAD Executive Committee as the ACM/SIGDA representative. Professors Tony Givargis and Alex Orailoglu served as members of the ICCAD Technical Program Committee.

We extend congratulations to these research affiliates and their graduate students who represented CECS at ICCAD.



Abstract Embedded System

*He who never made a mistake never made a discovery.*

Samuel Smiles

## CECS at Cal-(It)<sup>2</sup>

A few photos of CECS affiliates at the dedication of the Cal-(It)<sup>2</sup> building held on November 19, 2004 are shown below.



Pictured above from left: Professor Daniel D. Gajski, Dean Nicolaos G. Alexopoulos, Dr. Henry T. Nicholas, III and Executive Vice Chancellor Michael R. Gottfredson.



Pictured above from left: Professor Masanobu Shinozuka, Chair, Department of Civil and Environmental Engineering, and Professor Pai H. Chou. Professor Chou and his graduate students developed the vibration sensor network and software platform used by Professor Shinozuka to monitor, in real time, the Cal-(It)<sup>2</sup> building's movements in response to earth quakes or other ground activity.

## Gajski Addresses Local IEEE

Professor Daniel D. Gajski addressed the IEEE Orange County Computer Society on October 25, 2005 at the UCI University Club. The title of his presentation was *Extreme Makeover of Design Automation*. An attentive audience of 30 people attend the IEEE event.

Professor Gajski stated that with complexities of System-on-Chip (SoC) rising almost daily, the design community has been searching for new vision that can manage given complexities with increased design productivity and decreased time-to-market. The obvious solution, such as increasing levels of abstraction, introducing a variety of IPs or offering new design languages will not effectively solve the problem but only prolong the present status of inefficiency and confusion. This confusion leads to longer verification times. What is needed is a drastic change in design automation for complex systems that concurrently considers software and hardware. In order to design such systems efficiently, we need a new approach with new design flow, with new models with well defined semantics, and a new formalism that will support system synthesis and verification of software and hardware.

In order to find the solution, we must look at the system gap between software and hardware design and derive requirements for the design flow that includes software as well as hardware. In order to enable new EDA tools for model generation, simulation, synthesis, and verification, the design flow has to be well defined with unique abstraction levels, model semantics, and model transformations corresponding to design decisions made by the designers.

Professor Gajski then discussed the concept of model algebra that supports this approach and can serve as an enabler for the extreme makeover of EDA. He then presented hard data to support this concept and finished with a prediction and a roadmap toward the final goal of increasing designer productivity by several orders of magnitude while reducing the expertise level needed for designing complex systems to the basic principles of design science.

*"I do not fear computers, I fear the lack of them."*

Issac Asimov  
Russian Scientist

## Dutt Named Editor-in-Chief of ACM Transactions

Professor Nikil D. Dutt was recently named Editor-in-Chief of the ACM Transactions on Design Automation of Electronic Systems (TODAES). As such, he is in charge of the publication's Editorial Board and has 13 Associate Editors assisting him in the monthly publication. He has the responsibility to maintain the high editorial standards of this leading technical publication covering all aspects of design automation.

Congratulations are extended to Professor Dutt on this editorial appointment to a leading technical journal devoted to publication of design automation science and technology.

For further details please visit the TODAES web site: [www.acm.org/todaes/](http://www.acm.org/todaes/)

## CECS at RTSS 2004

CECS had a presence at the 25<sup>th</sup> IEEE International Real-Time Systems Symposium (RTSS 2004) held in Lisbon, Portugal on December 5-8, 2004. Professor Nikil D. Dutt served as Vice-Chair of a Special Track titled *Hardware/Software Co-Design*. Professors Rajesh Gupta and Alex Orailoglu served as members of the Hardware/Software Co-Design Track Program Committee.

*"We can't enjoy the benefits of science without confronting the risks."*

Sir Martin Rees



*"Competition brings out the best in products and the worst in people."*

David Sarnoff

## Dr. Briggs Delivers CECS Distinguished Lecture

On December 9, 2004, Dr. Faye A. Briggs, Intel Corporation, delivered a CECS Distinguished Lecture at the McDonnell-Douglas Auditorium. The title of his lecture was *Technological Challenges to Computer Architecture Innovation*. Professor Alexander Veidenbaum hosted Dr. Briggs during his visitation to CECS.

Dr. Briggs discussed the significant evolution of computer architecture over the last 30 years. With a major dependence on technology, we have been able to keep up with Moore's law. We are beginning to face enormous constraints in technology, and these create significant challenges for computer architecture advancement. He then presented an overview of many of the variables and constraints that will challenge traditional computer architecture innovations in the future. He then highlighted these challenges with the expectation of triggering more research and potential breakthroughs to sustain innovation in computer architecture.



Dr. Faye A. Briggs is Senior Principal Engineer and Director of Platform Performance Architecture, Enterprise Products Group, Intel Corporation, Portland, Oregon. Dr. Briggs led the architecture and engineering teams that developed the Intel AE870 for 2-16P Itanium AE servers. He was the cofounder and CTO of Axil Computers. While at Sun Microsystems, he coarchitected the first SPARC-V8, and led the architecture team that developed the SPARCserver2000. Dr. Briggs has served on the faculties at Purdue and Rice Universities. He has co-authored a popular textbook on *Computer Architecture and Parallel Processing*, and published over 40 technical papers. He received his MSEE from Stanford University and a PhD from the University of Illinois.

## Kurdahi Elected IEEE Fellow

The Institute of Electrical and Electronics Engineers (IEEE) Board of Directors announced that Fadi J. Kurdahi, Professor, Department of Electrical Engineering and Computer Science, Henry Samueli School of Engineering, University of California, Irvine, was elected a Fellow for *contributions to design automation of digital systems and to reconfigurable computing*. The designation of Fellow is awarded to no more than 0.1 percent of the voting membership of the IEEE each year for noteworthy contributions to the advancement of engineering, science, or technology. This year the IEEE recognized 268 senior researchers from the private and public sectors to its highest membership level.



Professor Kurdahi received the Bachelor of Engineering degree in Electrical Engineering from the American University of Beirut, Lebanon in 1981. He re-

ceived the MS degree in Electrical Engineering and the PhD degree in Computer Engineering from the University of California, Los Angeles, CA in 1982 and 1987, respectively. He has been a faculty member since 1987.

Professor Kurdahi's research interests are in high-level synthesis, estimation and design methodology of large digital systems. He has published over 100 technical papers, serves as the Associate Editor of the IEEE Transactions on Circuits and Systems, and has served on many conference program committees.

Congratulations Professor Kurdahi on being awarded this distinguished IEEE designation and honor.

## Graduate Student Issenin Interns at IMEC

Graduate student Ilya Issenin has spent the fall semester as a research intern at the Interuniversities MicroElectronics Center (IMEC), Leuven, Belgium. He collaborated with Erik Brockmeyer, IMEC, on research in data management and memory hierarchy customization for multiprocessor SoC systems.

IMEC was founded in 1984 and today is Europe's leading independent research center for the development and licensing of microelectronics, information, and communication technologies. IMEC employs nearly 1,000 people of whom 75 percent are highly qualified scientists and engineers. Its more than \$100,000,000 revenue is derived from agreements and contracts with the Flemish government, the European Community, the European Space Agency, and semiconductor companies worldwide. IMEC's research activities concentrate on design of integrated information and communication systems, silicon process technology, silicon device technology, microsystems, components and packaging, and advanced training in microelectronics.

## Chou Wins NSF CAREER Award

Professor Pai H. Chou has received notification from the National Science Foundation (NSF) of an award under its Faculty Early Career Development (CAREER) Program. His proposal was titled *Design Optimization and Quantitative Evaluation of Wireless Embedded Sensing Systems* and the award is for \$400,000 covering a 5 year duration.

The CAREER award is the NSF's most prestigious award to new faculty members. The CAREER program recognizes and supports the early career-development of those teacher-scholars who are most likely to become academic leaders of the 21<sup>st</sup> century. CAREER awardees are selected on the basis of creative, career-development plans that effectively integrate research and education within the context of the mission of their institution. The CAREER award plans should build a firm foundation for a lifetime of integrated contributions to research and education.

CECS extends congratulations to Professor Chou on receiving this prestigious NSF award and the accompanying recognition.



Shown above from left are: Bart Durinck, IMEC; Erik Brockmeyer, IMEC; Ilya Issenin, CECS; Arnout Vandecappelle, IMEC; Franky Catthoor, IMEC

The following were published by CECS faculty affiliates during the period of October 1, 2004 to December 31, 2004:

| Focus                                      | Title, Authors, Publication  |
|--|--|
| <a href="#">Backlight Adaptation</a>       | <i>Dynamic Backlight Adaptation for Low-Power Handheld Devices</i> , S. Pasricha, M. Luthra, S. Mohapatra, N. Dutt and N. Venkatasubramanian, IEEE Design and Test of Computers, September/October 2004, pp 398–405  |
| <a href="#">Cache Optimization</a>         | <i>Cache Optimization for Embedded Processor Cores: An Analytical Approach</i> , Arijit Ghosh and Tony Givargis, ACM Transactions on Design Automation of Electronic Systems, Volume 9, Number 4, October 2004, pp 419–440   |
| <a href="#">Parallelizing Compiler</a>     | <i>Coordinated Parallelizing Compiler Optimizations and High-Level Synthesis</i> , Sumit Gupta, Rajesh Kumar Gupta, Nikil D. Dutt and Alexandru Nicolau, ACM Transactions on Design Automation of Electronic Systems, Volume 9, Number 4, October 2004, pp 441–470 |
| <a href="#">Mode Transition Sequences</a>  | <i>Optimizing Mode Transition Sequences in Idle Intervals for Component-Level and System-Level Energy Minimization</i> , Jinfeng Liu and Pai H. Chou, Proceedings of the International Conference on Computer Aided Design (ICCAD), November 7-11, 2004, pp 21–28  |
| <a href="#">Code Partitioning</a>          | <i>Code Partitioning for Synthesis of Embedded Applications with Phantom</i> , André Costi Năcul and Tony Givargis, Proceedings of the International Conference on Computer Aided Design (ICCAD), November 7-11, 2004, pp 190–196                                  |
| <a href="#">Test Decompression</a>         | <i>Frugal Linear Network-Based Test Decompression for Drastic Test Cost Reductions</i> , Dexin Wenjing Rao, Alex Orailoglu and George Su, Proceedings of the International Conference on Computer Aided Design (ICCAD), November 7-11, 2004, pp 721–725            |
| <a href="#">Design Space Exploration</a>   | <i>Design Space Exploration for Aggressive Test Cost Reduction in Circular Scan Architectures</i> , Baras Arslan and Alex Orailoglu, Proceedings of the International Conference on Computer Aided Design (ICCAD), November 7-11, 2004, pp 726–731                 |
| <a href="#">Bus Architecture Synthesis</a> | <i>Floorplan-Aware Bus Architecture Synthesis</i> , Sudeep Pasricha, Nikil Dutt, Elaheh Bozorgzadeh and Mohamed Ben-Romdhane, UCI CECS Technical Report 04-27, October, 2004   |
| <a href="#">Power Estimation</a>           | <i>eCACTI: An Enhanced Power Estimation Model for On-Chip Caches</i> , Mahesh Mamidipaka and Nikil Dutt, UCI CECS Technical Report 04-28, October, 2004  |
| <a href="#">Verification</a>               | <i>System Level Verification with Model Algebra</i> , Samar Abdi and Daniel Gajski, UCI CECS Technical Report 04-29, November, 2004  |
| <a href="#">Serializing Compiler</a>       | <i>The Phantom Serializing Compiler</i> , Andre C. Nacul and Tony Givargis, UCI CECS Technical Report 04-30, November, 2004  |
| <a href="#">Slack Reclamation</a>          | <i>Leakage Aware Dynamic Slack Reclamation in Real-Time Embedded Systems</i> , Ravindra Jejurikar and Rajesh Gupta, UCI CECS Technical Report 04-31, November, 2004  |

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**CECS** — *promoting creativity and pursuing discovery!*

*Center for Embedded Computer Systems, University of California, Irvine*



**CECS Mission Statement:**

*To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.*

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**Smart Glove**

I have always said that future personal embedded systems had to be worn around your neck, on your wrist or belt, or in your pocket. Well I now may have to add on your hand. I recently came across information about a smart glove, named CommanderGauntlet, being developed by Network Anatomy, Pleasanton, CA shown below



**Applications**

The initial applications of CommanderGauntlet are targeted at emergency, search, and rescue

operations conducted by military, homeland security, and emergency management personnel. Harsh environments are everywhere and must have an integrated communications solution that can be easily and quickly adapt to change. Integrated communications is the melding of voice, data, video, and messaging with reliable transmission options.

**Features**

The smart glove would be centered around a liquid crystal display mounted on the dorsal side of the glove. An embedded processor would act as a functional manager. The smart glove would feature digital television and radio, video conferencing, GPS locator, e-mail messaging, cellular phone, weather and environmental sensors and a high-powered light. When you order your smart glove over the internet, you would be able to customize the color and fabric to your personal desires.

**Teaching Centerpiece**

The smart glove could be an ideal example for students studying embedded systems design—a teaching example. Students could be structure into design teams with each team member becoming a specialist in sensors, displays, processor, embedded software, etc. They could then construct a crude smart glove and dynamically test its functionality. I think this design topic could be structured into an exciting course for engineering students studying embedded systems.

**Future**

Can you imagine how cool a fashion statement this smart glove could become. The commentators at the Oscar and Emmy award TV shows would be discussing actresses and actors individual tastes in smart glove apparel.

Watch out Michael Jackson, I'm ready to wear a smart glove! Are you?

Bob Larsen