CECS eNEWS

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Center for Embedded Computer Systems, University of California, Irvine

Highlights:

Inside this issue:

CECS at Codesign & System Synthesis Conference

Research affiliates and graduate students of the Center for Embedded Computer Systems (CECS) at the University of California, Irvine played a vital role in the success of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis held at the Marriott Hotel and Tennis Club, Newport Beach, CA on October 1—3, 2003.

Professor Rajesh Gupta served as General Co-Chair and Professors Pai Chou and Alex Orailoglu served as Technical Program Co-Chairs. Professor Tony Givargis served as Finance and Local Arrangements Chair, Professor Frank Vahid served as Publicity Chair and Professor Nikil Dutt served as IFIP Liaison. Professors Daniel Gajski and Fadi Kurdahi served as members of the Technical Program Committee and Professors Pai Chou, Nikil Dutt, and Rajesh Gupta served as members of the Transition Committee.

The following technical papers were presented with the cited pages from the conference proceedings:

- *An Efficient Retargetable Framework for Instruction-Set Simulation*, Mehrdad Reshadi, Nikhil Bansal, Prabhat Mishra, and Nikil Dutt, pp 13—18
- *Transaction Level Modeling: An Overview*, Lukai Cai and Daniel Gajski, pp 19—24
- *RTOS Scheduling in Transaction Level Models*, Haobo Yu, Andreas Gerstlauer and Daniel Gajski, pp 31—36
- *A Fast Parallel Reed-Solomon Decoder on a Reconfigurable Architecture*, Arezou Koohi, Nader Bagherzadeh and Chengzi Pan, pp 59—64
- *A Case Study of Mapping a Software-Defined Radio (SDR) Application on a Reconfigurable DSP Core*, Behzad Mohebbi, Eliseu Filho, Rafael Maestre, Mark Davies and Fadhi Kurdahi, pp 103—108
- *A Codesigned On-Chip Logic Minimizer*, Roman Lysecky and Frank Vahid, pp 109—113
- *First Results with eBlocks: Embedded Systems Building Blocks*, Susan Cotterell, Frank Vahid, Walid Najjar and Harry Hsieh, pp 168—175

Profesor Nikil Dutt was the organizer and moderator of a panel session titled *Driving Agenda for Systems Research*.

These mentioned research affiliates and their graduate students made substantial contributions to the technical program and organization of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis. CECS is expecting to continue its technical and organizational influence of this conference in future years

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You see things, and you say, "Why?"

But I dream things that never were and say, "Why not?"

George Bernard Shaw
Back to Methuselah

Prof. Gajski Delivers Keynote Address

Professor Daniel D. Gajski delivered the Conference Keynote Address at the 2003 5th International Conference on ASIC (ASICON 2003) held at the Central Garden Hotel, Beijing, China on October 21—24, 2003. The title of his keynote address was *SoC Design for the New Millennium*. ASICON 2003 presented 328 technical papers to over 500 attendees.

Professor Gajski discussed the evolution of SoC design starting with the *Design and Simulate* methodology evolving to the *Describe and Synthesize* methodology evolving to the *Specify-Explore-Refine* methodology of today. He then discussed the hierarchy of system level modeling; creating a behavioral model, transforming it to a structural model, transforming it to a physical model; all based on an abstraction algebra and automatic model refinement. He also discussed the importance of modeling semantics which result in the system-level language issues disappearing. This was followed by a discussion of simple and powerful synthesis, verification, and test strategies for SoC designs. He concluded the address by an optimistic discussion of the bright future for SoC design, methodologies, and applications.

Patt Delivers CECS Distinguished Lecture

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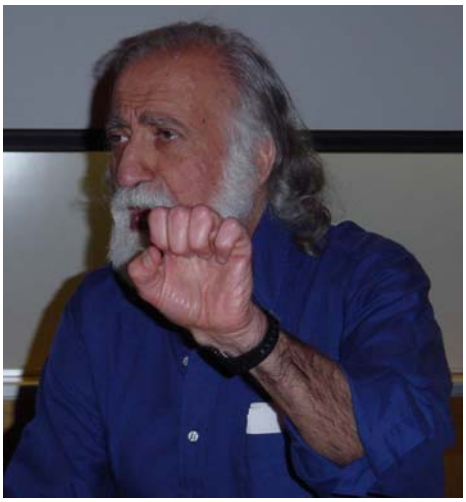
Predicts 3 billion transistor, 10GHz µP

On December 9, 2003, Professor Yale Patt, Professor of Electrical and Computer Engineering and Ernest Cockrell, Jr. Centennial Chair in Engineering at the University of Texas at Austin, delivered a CECS Distinguished Lecture titled *The Fundamentals: Moore's Law, Microarchitecture, and the Microprocessor of the Year 2014* to a near capacity audience at the UCI McDonnell Douglas Auditorium. Professor Jean-Luc Gaudiot, Chair of the Department of Electrical Engineering and Computer Science, introduced Professor Patt and served as his host during his visitation to CECS.



Microarchtecture is alive and well. Professor Patt dispels naysayers!

Professor Patt discussed the promises of Moore's Law that very soon predicts more than a billion transistors on a chip processing at more than 10 GHz. Then he proposed the question: is there anything left to do in microarchitecture to make use of all this processing capability, or should we fold our tents and go home? As usual, Professor Patt tied his comments to the fundamentals because he strongly believes it is always the fundamentals that provide profound insights to new knowledge. He concluded his lecture discussing his vision of the 2014 microprocessor; including the block-structured ISA, stronger use of SSMT, greater use of microcode, dedicated

Gajski & Abdi at VERIFY 2003

Professor Daniel D. Gajski and Graduate Student Samar Abdi alternately served as Keynote Speakers at VERIFY 2003 held at venues worldwide. Their keynote address was titled *System Debugging and Verification: A New Challenge*. The theme of VERIFY 2003 was *Verification Process Automation from ESL to Gates*. This was a verification seminar sponsored by Axis Systems, CoWare, Denali Systems, Novas Software, Sun Microsystems, and Verisity. The one-day educational seminars were held in Austin on October 9, San Jose on October 14, San Diego on October 16, Munich, Germany on October 21, Boston on October 28, Ottawa, Canada on October 30, and Santa Clara on November 4.

These keynote presentations covered the following topics: assertion-based verification, formal methods of logical equivalence checking, hardware-assisted verification, and model checking and theorem proving techniques.

Patt continued

infrequently used functional units, and most importantly, a stronger coupling with the compiler, language, and algorithm technologies.

Professor Patt directs the PhD research of 12 graduate students in computer architecture and teaches a freshmen course titled *Introduction to Computing* and a graduate course in Microarchitecture. He has received the highest honors in his field for his research and teaching, including the 1996 IEEE/ACM Eckert-Mauchly Award for his contributions to high performance microprocessor design and the 2000 ACM Karl V. Karlstrom Outstanding Educator Award for his contributions to education. He has had, for the past 35 years, an active consulting practice, including long term associations with Intel, Digital Equipment, NCR, Motorola, and others. His freshman textbook *Introduction to Computing Systems: From Bits and Gates to C and Beyond* has been adopted by more than 100 universities world-wide. Professor Patt is a Fellow of both the IEEE and ACM.

International Conference on System Design Science

The Center for Embedded Computer Systems (CECS) is inaugurating a new conference devoted to the foundations of system design. Titled the International Conference on System Design Science (ICSDS), it will be held on November 4-5, 2004 at the Westin South Coast Plaza Hotel, Costa Mesa, CA.

Present designs are based on basic algorithms of computer science and principles of computer engineering that were established many years ago. However, there are no solid design foundations for the future complex systems consisting of software, hardware, and multiple nanotechnologies. Without foundations there is no progress! With this in mind, this conference is soliciting papers, tutorials, and other contributions on seminal, novel, and innovative concepts, definitions, doctrines, formulations, and principles underlying the design science of electronic systems including but not limited to the following topics:

Design Science Fundamentals
Design Principles
Formal Representations
Design Styles and Design Algebras
Modeling Formalism and Semantics
Models of Computation
Design Languages
SW/HW Design Methodologies
Fundamental Algorithms for SW/HW Synthesis
Formal Methods for Verification/Test
Application-Specific Theories
Standards/Metrics

Please consider contributing to and attending this new conference. We are planning an environment to encourage discussion and exploration of fundamental issues confronting the design of complex systems. We invite you to attend this exciting, thought provocative, conference and enjoy the Southern California environment. Look for additional information in the coming weeks at the CECS web site. We hope to see you at ICSDS this coming November.

Discovery consists of seeing what everybody has seen and thinking what nobody has thought.

Albert Szent-Gyorgyi
1937 Nobel Laureate in Medicine

Dr. Arinobu Joins Research Advisory Board

CECS is pleased to welcome the newest member of our Research Advisory Board—Dr. Mutsuhiro Arinobu, Corporate Vice President and Director, Corporate Research and Development, Toshiba Corporation, Tokyo, Japan.

Dr. Arinobu received the BSc in Mechanical Engineering from Yokohama National University in 1971, the MSc in 1973 and PhD in 1976, both in Mechanical Engineering from the University of Tokyo, Japan. He is a Councilor of the Japan Society for Software Science and Technology, Japan Society for Science Policy and Research Management, Japan Society of Mechanical Engineers, and the Institute for Future Technology. He is a board member of the Kanagawa Academy of Science and Technology, a Fellow of the Japan Society of Mechanical Engineers, and a member of the Atomic Energy Society of Japan.

Dr. Arinobu joined the Toshiba Corporation in 1976 and was appointed General Manager, Technology Planning Division in 2000. In 2003, he was elected Corporate Vice President and Director, Corporate Research and Development Center.

CECS is extremely pleased that Dr. Arinobu has joined our Research Advisory Board. His extensive international business, managerial, and research experience will benefit the future research directions of CECS.

Gupta Featured in EE Times Article

Post-doctoral Researcher Sumit Gupta was featured in an article titled *Tool Promises Parallelizing Synthesis* by Richard Goering in the EE Times issue dated December 19, 2003. Some of the salient facts mentioned in this article are cited here.

SPARK uses parallelizing compiler technology previously developed for instruction-level parallelism, and "re-instruments" it for synthesis by adding mutual exclusivity of operations, resource sharing and hardware models. According to researchers, the tool yields high-quality results, especially for control-intensive microprocessor functional blocks and multimedia and image-processing applications.

"We believe that this is a new enabling technology that will fulfill the promise of high-level behavioral synthesis," said Sumit Gupta, research specialist at the Center for Embedded Computer Systems. "**SPARK** is a prototype that demonstrates that this technology can be successfully used to produce a high quality of results."

Behavioral synthesis has never really caught on among chip designers. "High-level synthesis has gotten a bad rap despite the claims over two decades. It rarely delivers in terms of expectations on quality of synthesis results," Gupta said. "We are looking to provide a solution that improves the state of the art by bring a new range of code transformations to high-level synthesis."

SPARK differs from previous attempts at behavioral synthesis in two ways, Gupta said. First, it offers more techniques to

Gupta continued

improve quality of results. Second, it's not a pushbutton tool; instead, it gives designers control over transformations applied to the design, so they can experiment with different optimizations.

SPARK takes purely behavioral C code, although it offers a language-independent approach that could easily be adapted to SystemC or SystemVerilog, Gupta said. Following pre-synthesis optimizations, it uses a "toolbox" approach that offers various kinds of code transformations and heuristics. With user input, **SPARK** does scheduling, allocation, resource binding, control synthesis and back-end code generation.

The tool uses an intermediate representation that retains all the information given in the input description. **SPARK** converts C input into a control-data flow graph, and the synthesizes it into an architecture consisting of a data path, memory, control unit and interconnections. "We have gone out of the box of traditional high-level synthesis and developed ways in which the source code is moved through the control flow even as we are carrying out individual synthesis tasks," said Gupta.

Gupta acknowledged that **SPARK** is a prototype, and that it hasn't been used in a production chip design flow. He said, however, that there have been "several inquiries" from commercial companies interested in licensing the technology.

The Center for Embedded Computer Systems is currently offering free downloads of **SPARK** for Linux and Solaris platforms, along with a user manual, a tutorial and an MPEG-1 player design example.

Leadership and management are two different things. You lead people, and you manage projects.

Navy Captain Grace Hopper
1973

The following were published by CECS faculty affiliates during the period of October 1, 2003 to December 31, 2003:

Focus	Title, Authors, Publication
Code Motions	*Dynamically Increasing the Scope of Code Motions During the High-Level Synthesis of Digital Circuits*, Sumit Gupta, Nikil Dutt, Rajesh Gupta, and Alex Nicolau, IEE (British) Proceedings—Computers & Digital Techniques, Volume 150, Number 5, September 2003, pp 330—337
Retargetable Framework	*An Efficient Retargetable Framework for Instruction-Set Simulation*, Mehrdad Reshadi, Nikhil Bansa, Prabhat Mishra and Nikil Dutt, Proceedings of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, October 1-3, 2003, pp 13—18
Transaction Level Modeling	*A Transaction Level Modeling: An Overview*, Lukai Cai and Daniel Gajski, Proceedings of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, October 1-3, 2003, pp 19—24
RTOS Scheduling	*RTOS Scheduling in Transaction Level Models*, Haobo Yu, Andreas Gerstlauer and Daniel Gajski, Proceedings of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, October 1-3, 2003, pp 31—36
Reed-Solomon Decoder	*A Fast Parallel Reed-Solomon Decoder on a Reconfigurable Architecture*, Arezou Koohi, Nader Bagherzadeh and Chengzi Pan, Proceedings of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, October 1-3, 2003, pp 59—64
Software Defined Radio	*A Case Study of Mapping a Software Defined Radio (SDR) Application on a Reconfigurable DSP Core*, Behzad Mohebbi, Eliseu Filho, Rafael Maestre, Mark Davies and Fadi Kurdahi, Proceedings of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, October 1-3, 2003, pp 103—108
Logic Minimizer	*A Codesigned On-Chip Logic Minimizer,* Roman Lysecky and Frank Vahid, Proceedings of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, October 1-3, 2003, pp 109—113
eBlocks	*First Results with eBlocks: Embedded Systems Building Blocks*, Susan Cotterell, Frank Vahid, Walid Najjar and Harry Hsieh, Proceedings of the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis, October 1-3, 2003, pp 168—175
Communication Abstractions	*Communication Abstractions for System-Level Design and Synthesis*, Andreas Gerstlauer, UCI CECS Technical Report 03-30, October 16, 2003
Leakage Power Estimation	*Leakage Power Estimation in SRAMs*, Mahesh Mamidipaka, Kamai Khouri, Nikil Dutt and Magdy Abadir, UCI CECS Technical Report 03-32, October 2003
Bus Models	*Automatic Generation of Bus Functional Models from Transaction Level Models*, Dongwan Shin, Samar Abdi and Daniel Gajski, UCI CECS Technical Report 03-33, November 2003
Cache Reconfiguration	*Dynamic Voltage and Cache Reconfiguration for Low Power Systems*, Andre Nacul and Tony Givargis, UCI CECS Technical Report 03-34, November 2003
Dynamic Voltage Scheduling	*Leakage Aware Dynamic Voltage Scheduling for Real-Time Embedded Systems*, Ravindra Jejurikar, Cristiano Pereira and Rajesh Gupta, UCI CECS Technical Report 03-35, November 2003
Portable Code	*POSIX-Compliant Portable Code Synthesis for Embedded Systems*, Andre Nacul, Siddharth Choudhuri and Tony Givargis, UCI CECS Technical Report 03-36, November 2003
Energy Analysis	*Energy Analysis of Multimedia Watermarking on Mobile Handheld Devices*, Arun Kejariwal, UCI CECS Technical Report 03-37, December 2003
Task Partitioning	*Proxy-based Task Partitioning of Watermarking Algorithms for Reducing Energy Consumption in Mobile Devices*, Arun Kejariwal, UCI CECS Technical Report 03-38, December 2003
Thread Composition	*Petri Net-based Thread Composition for Improved System Level Simulation*, Nick Savoiu, Sandeep Shukla, and Rajesh Gupta, UCI CECS Technical Report 03-39, December 2003
Power Optimization	*FIFO Power Optimization for On-Chip Networks*, Sudarshan Banerjee and Nikil Dutt, UCI CECS Technical Report 03-40, December 2003

CECS—Solving Tomorrow's Problems!

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Wireless Wonders

The reality is that we face a future world without wires. I have recently been pondering an article in the September 18, 2003 issue of Electronic News which reports on a keynote address delivered by Patrick Gelsinger, Intel Senior Vice President at the Intel Developers Forum held in San Jose, CA.

Gelsinger imagines a world where all devices interconnect wirelessly and seamlessly for ubiquitous communications anytime, anywhere. He continues stating that through advances in antenna utilization, wireless networking architecture, network switching when roaming network to network, and radio built into chips, this future network will enable ubiquitous data, video, and voice communications on any device without increasing costs.

I think the root of my problem stems from my 1950's experience with Heath Kits. All engineers then were having fun building oscilloscopes, audio amplifiers, and television receivers. I loved playing with wires when I was a young engineer; bundling wires, stripping insulation, soldering wires, and connecting them to components.

I fondly remember building a Heath Kit audio amplifier that used a pair of matched KT66 pentode tubes in a push-pull amplifier circuit. I coupled this amplifier to a 48 rpm and 33 1/3 rpm record changer and an awesome tweeter and woofer. I enjoyed listening to jazz and swing music on that home-made hi-fi set for about 20 years.

Each Heath Kit came with step-by-step assembly instructions that you followed. The biggest challenge was debugging the system you had constructed. But you had the "hands-on" experience of seeing signals wiggle—today's engineers are missing the fun of building, testing, and enjoying electronic circuits. I'm very thankful I had that experience.

But wires are a thing of the past for today's engineers. The majority of communications, computing and entertainment are being conducted without wires—wireless wonders. I have to admit that wireless communications is dramatically changing our communication habits and infrastructure. Recently, I saw a lady performing an ATM withdrawal, communicating with another lady in line, and talking on a wireless phone simultaneously. Now that's real-time concurrent processing!

Everybody loves the idea of wireless wonders. This is demonstrated by the dramatic worldwide growth in cell phones. My only regret is I can't build one myself; that's the price we pay today for electronic miniaturization.

But I really miss the smell of smoking solder flux!

Bob Larsen