Highlights:

- CECS at ISSS '02
- CECS at ICCAD '02
- Professor Klefstad
- Professor Kurdahi
- Graduate Student Azevedo
- Publications

CECS at ISSS '02

The Center for Embedded Computer Systems (CECS) at the University of California, Irvine continues playing a dominant role at the International Symposium on System Synthesis (ISSS '02) held at Kyoto, Japan on October 2-4, 2002. ISSS is considered the leading international conference addressing the technical issues accompanying system design. CECS faculty affiliates presented 10 of the 40 technical papers composing the conference program, by far the largest total for any research organization.

The following technical presentations were made by CECS faculty affiliates and their graduate students at ISSS '02; the technical papers can be found in the conference proceedings at the cited pages:

- *"Tuning of Loop Cache Architectures to Programs in Embedded System Designs"*, S. Cotterell and F. Vahid, pp 8—13

- *"Combined Functional Partitioning and Communication Speed Selection for Networked Voltage-Scalable Processors"*, J. Liu, P. H. Chou, and N.Bagherzadeh, pp 14—19

- *"Optimal Message Passing for Data Coherency in Distributed Architecture"*, J. Peng and D. Gajski, pp 20—25

- *"A Design Space Exploration Framework for Reduced Bit-Width Instruction Set Architecture (rISA) Design"*, A. Halambi, A. Shrivastava, P. Biswas, N. Dutt, and A. Nicolau, pp 181—186

- *"The Formal Execution Semantics of SpecC"*, W. Mueller, R. Doemer, and A. Gerstlauer, pp 150—155

- *"Efficient Simulation of Synthesis-Oriented System Level Designs"*, N. Saviou, S. K. Shukla, and R. Gupta, pp 168—173

- *"Efficient Power Reduction Techniques for Time Multiplexed Address Buses"*, M. Mamidipaka, N. Dutt, and D. Hirschberg, pp 207—212

- *"Low-Power Data Memory Communication for Application-Specific Embedded Processors"*, P. Petrov and A. Orailoglu, pp 219—224

- *"System-Level Abstraction Semantics"*, A. Gerstlauer and D. Gajski, pp 231—236

- *"Dynamic Common Sub-Expression Elimination During Scheduling in High-Level Synthesis"*, S. Gupta, M. Reshadi, N. Saviou, N. Dutt, and A. Nicolau, pp 261—266

In 2003, the International Symposium on System Synthesis will merge with the Software/Hardware Codesign Symposium to create the premier international conference on system design. CECS's impressive influence at the 2002 conference will continue in 2003 as Professor Rajesh Gupta will serve as Conference General Co-Chair and Professors Pai Chou and Alex Orailoglu will serve as Program Co-Chairs.

CECS is extremely proud of its technical influence at ISSS '02 which reflects the level of technical relevance and international recognition in its collaborative research programs.

CECS at ICCAD '02

The Center for Embedded Computer Systems (CECS) at the University of California, Irvine also had a presence at the IEEE/ACM International Conference on Computer-Aided Design held November 10-14, 2002 in San Jose, CA.

The following technical presentations were made by CECS faculty affiliates and their graduate students at ICCAD '02; the technical papers can be found in the conference proceedings at the cited pages:

- *"Hardware/Software Partitioning of Software Binaries"*, Greg Stitt and Frank Vahid, pp 164—170

- *"A Novel Scan Architecture for Power-Efficient, Rapid Test"*, Ozgur Sinanoglu and Alex Orailoglu, pp 299—303

- *"Efficient Instruction Encoding for Automatic Instruction Set Design of Configurable ASIPS"*, Jong-eun Lee, Kiyoung Choi, and Nikil Dutt, pp 649—654

- *"Synthesis of Customized Loop Caches for Core-Based Embedded Systems"*, Susan Cotterell and Frank Vahid, pp 655—662

Professors Nikil Dutt, Rajesh Gupta, and Frank Vahid served on the ICCAD Technical Program Committee. Professor Frank Vahid sereved as Moderator of a session titled "System-Level Performance and Power Modeling and Optimization" and Professor Rajesh Gupta served as Moderator of a session titled "Advances in Dynamic Voltage Scheduling".

Professor Introduction

The Center for Embedded Computer Systems (CECS) is pleased to introduce Dr. Raymond Klefstad as a new research affiliate. Dr. Klefstad is an Assistant Adjunct Professor in the Department of Electrical Engineering and Computer Science in the Henry Samueli School of Engineering.

Professor Klefstad was born in San Diego, CA and received his BS, *Magna Cum Laude,* in 1981, MS in 1982, and PhD in 1988 all from the University of California, Irvine. He is a member of Phi Beta Kappa honorary society. He is the recipient of numerous teaching awards including the Outstanding Non-Senate Teacher Award in 1999 and 2000.

Professor Klefstad was recently awarded a $803,000 contract from the Boeing Company for a three-year research project, starting January 2003, to develop CORBA middleware for distributed, real-time, embedded systems using real-time Java. He recently was awarded "**Best Paper**" in the Software Technology cluster for a paper titled *"Design and Performance of a Dynamically Configurable, Messaging Protocols Framework for Real-Time CORBA"* by Raymond Klefstad, Sumita Rao, and Douglas Schmidt at the Hawaii International Conference on System Sciences, January 2003.

Professor Klefstad's research interests are in distributed object computing and high performance, real-time object-request brokers (ORBs), design patterns for object-oriented communication systems, object-oriented communication software frameworks, and flexible and adaptive distrib-uted, parallel, concurrent systems. Some of Professor Klefstad's recent publications are:

- *"Design and Evaluation of a Highly Modular CORBA Portable Object Adapter for Distributed, Real-Time, Embedded Systems"*, Raymond Klefstad, Arvind Krishna, and Douglas Schmidt, Department of the Army, 2002
- *"The Design and Performance of a Dynamically Configurable, Messaging Protocols Framework for Real-Time CORBA"*, Raymond Klefstad, Sumita Rao, and Douglas Schmidt, HICSS, 2002
- *"Virtual Component: A Design Pattern for Memory-Constrained Embedded Applications"*, Angelo Corsaro, Douglas Schmidt, Raymond Klefstad, and Carlos O'Ryan, Proceedings of the 9th Annual Conference on the Pattern Languages of Programs, September 2002
- *"Towards Highly Configurable Real-Time Object Request Brokers"*, Raymond Klefstad, Douglas Schmidt, and Carlos O'Ryan, Proceedings of the IEEE/IFIP International Symposium on Object-Oriented Real-Time Distributed

Go Team Go

The Center for Embedded Computer Systems (CECS) at the University of California, Irvine sent a student team to compete in the SIGDA CADathlon contest held at the International Conference on Computer Aided Design on November 10, 2002 in San Jose, CA. The CECS student team consisted of graduate students Aviral Shrivastava and Partha Biswas with Professor Nikil Dutt serving as faculty advisor. The CECS team was one of 18 university teams competing in the CADathlon.

At the contest, each student team was given six problem statements and example test data related to various aspects of computer aided design. Problem solutions were judged on correctness and efficiency. The student team that solved the most problems in the fewest attempts and in the least cumulative time was declared the winner. Incorrect solutions were penalized.

Congratulations to Aviral Shrivastava and Partha Biswas on representing CECS at the SIGDA CADathlon contest .

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Contracts and Gifts

- Professor Alex Nicolau received a $190,000 contract titled "NGS: An Application Development Environment for Complex Heterogeneous Distributed Real-Time Embedded Computing Platforms" from the National Science Foundation

- Professor Nikil Dutt received a contract titled "ADL-Based Exploration of Reconfigurable Coprocessors" from the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan

- Professor Daniel D. Gajski received a gift from Emulex Corporation, Costa Mesa, CA to support the 2003 Southern California Embedded Systems Symposium and for laptop computers

Professor Profile

CECS is proud to profile Professor Fadi J. Kurdahi, Department of Electrical and Engineering and Computer Science, University of California, Irvine (UCI), as an outstanding research affiliate. He received the PhD degree in Computer Engineering from the University of Southern California in 1987. Since 1987, he has been a professor in the Department of Electrical Engineering and Computer Science with a joint appointment in the Information and Computer Science Department.

Professor Kurdahi lives in University Hills with his wife Seta and their two sons, Michael and Christian.

From 1997-2000 he was the lead investigator of a major DARPA sponsored research project to develop a new breed of reconfigurable computing chip. The **M1** chip has over 1.5 million transistors designed to help break new grounds in attacking several *"Grand Challenge"* problems such as real-time video compression, automatic target recognition, and real-time wireless applications. The **M1** chip was conceived, designed, fabricated, and tested as part of this project. This research project was among the most successful projects in DARPA's Adaptive Computing Systems initiative, which funded about 60 research projects nationwide.

From 2000-2002, Professor Kurdahi was on leave from UCI working at Morpho Technologies, Irvine, CA. Morpho Technologies is a start-up company developing reconfigurable computing solutions for wireless communication appliances.

Professor Kurdahi has served on the program committees of ISSS, ED&T, and ISCAS. From 1993-1995, Professor Kurdahi served as Associate Editor of the IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. He is currently serving on the editorial board of IEEE Design and Test magazine. He was Program Chair of the 1999 International Symposium on System Synthesis (ISSS) and the General Chair of ISSS in 2000. He received an NSF Research Initiative Award in 1989, two ACM/SIGDA fellowships in 1991 and 1992, three distinguished paper awards, and the Best Paper Award for the 2002 IEEE Transactions on VLSI.

Professor Kurdahi's research interests are in reconfigurable computing, high-level synthesis of digital circuits, VLSI systems design and layout, and design automation. The following two publications represent significant technical contributions of with the first receiveing a Best Paper Award:

● *"A Formal Approach to Context Scheduling for Multi-Context Re*

Graduate Student Profile

CECS is honored to profile a recent PhD graduate Ana Azevedo who was born in Rio de Janeiro, Brazil, in 1970. She received a B.S. in Electronics Engineering in 1994 and a MS in Computer Engineering in 1995 from the prestigious Universidade Federal do Rio de Janeiro. In 1995 she moved to the U.S. to pursue further graduate education in Computer Science. She received a MS in 1997 and a PhD in 2002 from the University of California, Irvine.

While studying in Brazil, Ana was granted several scholarships for undergraduate and graduate studies due to her excellent academic achievements and at UCI, she has served as a teaching assistant, research assistant and as a consulting engineer for a local company. She was the recipient of the 2002 Joseph Fischer Memorial Fellowship and she has also been assigned a special ICS GSR appointment for the Spring Quarter 2002.

Her research interests are in computer architecture, programming languages, compilers and power-aware computing. In her PhD dissertation she studied mobile code technologies and related issues in dynamic compilation and program interpretation. She proposed an annotation-based compiler technology that caught great attention as reflected in her published papers and invited talks throughout industrial research laboratories. Her research at CECS was jointly supervised by Professors Alex Nicolau and Alex Veidenbaum.

What is next for Ana? There is no doubt market trends toward network-connected embedded systems will require capability to efficiently execute mobile codes. High performance, low power mobile code execution engines will be of great demand. Ana has developed expertise to build such systems. From an industrial point of view, Ana's research dealt with a crucial performance issue. From an academic standpoint, the research she conducted at CECS will better prepare her for introducing mobile code technology to modern programming language courses. She believes that either career path she chooses will be very interesting and technically challenging.

Some of Ana's recent publications are:

● *"Profile-Based Dynamic Voltage Scheduling Using Program Checkpoints*", Ana Azevedo, Radu Cornea, Ilya Issenin, Rajesh Gupta, Nikil Dutt, Alex Veidenbaum and Alex Nicolau, Proceedings of the Design, Automation and Test Conference in Europe (DATE), March, 2002

● *"Architectural and Compiler Strategies for Dynamic Power Management in the COPPER Project*", Ana Azevedo, Radu Cornea, Ilya Issenin, Rajesh Gupta, Nikil Dutt, Alex Veidenbaum and Alex Nicolau, Proceedings of the International Workshop on Innovative Architecture (IWIA), January 2001

● *"An Annotation-Aware Java Virtual Machine Implementation*", Ana Azevedo, Alex Nicolau and Joe Hummel, Journal Concurrency:

The following were published by CECS faculty affiliates during the period of July 1, 2002 to December 31, 2002:

Focus	Title, Authors, Publication
Testability Analysis	"*Multilevel Testability Analysis and Solutions for Integrated Bluetooth Transceivers*", Sule Ozev, Christian V. Olgaard, and Alex Orailoglu, IEEE Design and Test of Computers, September—October 2002, pp 82—91
Tuning Framework	"***Platune***: *A Tuning Framework for System-on-Chip Platforms*", Tony Givargis and Frank Vahid, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 21, No. 11, November 2002, pp 1317—1327
Partitioning	"*Hardware/Software Partitioning of Software Binaries*", Greg Stitt and Frank Vahid, Proceedings of the IEEE/ACM International Conference on Computer-Aided Design, November 10-14, 2002, pp 164—170
Scan Architecture	"*A Novel Scan Architecture for Power-Efficient, Rapid Test*", Ozgur Sinanoglu and Alex Orailoglu, Proceedings of the IEEE/ACM International Conference on Computer-Aided Design, November 10-14, 2002, pp 299—303
Instruction Encoding	"*Efficient Instruction Encoding for Automatic Instruction Set Design of Configurable ASIPS*", Jong-eun Lee, Kiyoung Choi, and Nikil Dutt, Proceedings of the IEEE/ACM International Conference on Computer-Aided Design, November 10-14, 2002, pp 649—654
Loop Caches	"*Synthesis of Customized Loop Caches for Core-Based Embedded Systems*", Susan Cotterell and Frank Vahid, Proceedings of the IEEE/ACM International Conference on Computer-Aided Design, November 10-14, 2002, pp 655—662
Cache Architectures	"*Tuning of Loop Cache Architectures to Programs in Embedded System Designs*", S. Cotterell and F. Vahid, Proceedings of the International Symposium on System Synthesis, October 2-4, 2002, pp 8—13
Partitioning/Speed Selection	"*Combined Functional Partitioning and Communication Speed Selection for Networked Voltage-Scalable Processors*", J. Liu, P. H. Chou, and N. Bagherzadeh, Proceedings of the International Symposium on System Synthesis, October 2-4, 2002, pp 14—19
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Execution Semantics	"*The Formal Execution Semantics of **SpecC***", W. Mueller, R. Doemer, and A. Gerstlauer, Proceedings of the International Symposium on System Synthesis, October 2-4, 2002, pp 150—155
Simulation	"*Efficient Simulation of Synthesis-Oriented System Level Designs*", N. Saviou, S. K. Shukla, and R. Gupta, Proceedings of the International Symposium on System Synthesis, October 2-4, 2002, pp 168—173
Power Reduction	"*Efficient Power Reduction Techniques for Time Multiplexed Address Buses*", M. Mamidipaka, N. Dutt, and D. Hirschberg, Proceedings of the International Symposium on System Synthesis, October 2-4, 2002, pp 207—212
Memory Communications	"*Low-Power Data Memory Communication for Application-Specific Embedded Processors*", P. Petrov and A. Orailoglu, Proceedings of the International Symposium on System Synthesis, October 2-4, 2002, pp 219—224
Abstraction Semantics	"*System-Level Abstraction Semantics*", A. Gerstlauer and D. Gajski, Proceedings of the International Symposium on System Synthesis, October 2-4, 2002, pp 231—236
Sub-Expression Elimination	"*Dynamic Common Sub-Expression Elimination During Scheduling in High-Level Synthesis*", S. Gupta, M. Reshadi, N. Saviou, N. Dutt, and A. Nicolau, Proceedings of the International Symposium on System Synthesis, October 2-4, 2002, pp 261—266

The following were published by CECS faculty affiliates during the period of July 1, 2002 to December 31, 2002:

Focus	Title, Authors, Publication
Instruction Set Design	*"Automatic Instruction Set Design Through Efficient Instruction Encoding for Application-Specific Processors"*, Jong-eun Lee, Kiyoung Choi, and Nikil Dutt, UCI CECS Technical Report 02-23, August 8, 2002
EDF Scheduling	*"Energy Aware EDF Scheduling with Task Synchronization for Embedded Real Time Systems"*, Ravindra Jejurikar and Rajesh Gupta, UCI CECS Technical Report 02-24, August 8, 2002
RTOS Modeling	*"RTOS Modeling in System Level Synthesis"*, Haobo Yu, Andreas Gerstlauer and Daniel Gajski, UCI CECS Technical Report 02-25, August 30, 2002
Cache Organization	*"Optimal Cache Organization Using an Allocation Tree"*, Tony Givargis, UCI CECS Technical Report 02-22, September 11, 2002
Architecture Description Language	*"Architecture Description Language Driven Functional Test Program Generation for Microprocessors Using SMV"*, Prabhat Mishra and Nikil Dutt, UCI CECS Technical Report 02-26, September 2002
Design Space Exploration	*"Analytical Design Space Exploration of Caches for Embedded Systems"*, Arjit Ghosh and Tony Givargis, UCI CECS Technical Report 02-27, September 11, 2002
SCE Environment	*"SCE Environment—Tutorial"*, Daniel Gajski, Samar Abdi, Junyu Peng, Rainer Doemer, Dongwan Shin, Andreas Gerstlauer, Alex Gluhak, Lukai Cai, Qiang Xie, Haobo Yu, and Pei Zhang, UCI CECS Technical Report 02-28, September 24, 2002
Global Code Motions	*"Using Global Code Motions to Improve the Quality of Results for High-Level Synthesis"*, Sumit Gupta, Nick Savoiu, Nikil Dutt, Rajesh Gupta, and Alex Nicolau, UCI CECS Technical Report 02-29, October 25, 2002
System Design	*"C/C++ Based System Design Flow Using **SpecC**, VCC, and SystemC"*, Lukai Cai, D. Gajski, Mike Olivarez, and Paul Kritzinger, UCI CECS Technical Report 02-30, November 14, 2002
System Level Design	*"System Level Design Flow: What is needed and what is not?"*, Daniel Gajski, UCI CECS Technical Report 02-33, November 26, 2002
Mapping Loops	*"Mapping Loops on Coarse-Grain Reconfigurable Architectures Using Memory Operation Sharing"*, Jong-eun Lee, Kiyoung Choi, and Nikil Dutt, UCI CECS Technical Report 02-34, December 5, 2002
Compiler Optimizations	*"Coordinated Parallelizing Compiler Optimizations and High-Level Synthesis"*, Sumit Gupta, Nikil Dutt, Rajesh Gupta, and Alex Nicolau, UCI CECS Technical Report 02-35, December 11, 2002
Static Slowdown Factors	*"Computing Static Slowdown Factors Under EDF Scheduling When Deadline Less Than Period"*, Ravindra Jejurikar and Rajesh Gupta, UCI CECS Technical Report 02-36, December 1, 2002

From page 3, Kurdahi

configurable Architectures", Fadi Kurdahi, Rafael Maestre, Milagros Fernandez, Roman Hermida, Nader Bagherzadeh, and Hartej Singh, IEEE Transactions on VLSI, December 2001

"Morphosys: An Integrated Reconfigurable System for Data-Parallel, Computation-Intensive Applications", F. Kurdahi, H. Singh, M. Lee, N. Bagherzadeh, and E. Filho, IEEE Transactions on Computers, Vol. 49, No. 5, May 2000

From page 3, Azevedo

Practice and Experience, Volume 12, Issue 6, May 2000, pp. 423-444

● *"Java Annotation-Aware Just-In-Time (AJIT) Compilation System"*, Ana Azevedo, Alex Nicolau and Joe Hummel, Proceedings of the ACM Java Grande Conference, June 1999

CECS—Solving Tomorrow's Problems!

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CECS *Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Research ?

"Research is what I'm doing when I don't know what I'm doing."

Wernher von Braun

The great rocket scientist, Wernher von Braun, succinctly shows tremendous insight into research. I have been struggling lately with the relevance of the CECS research program. How can CECS achieve significantly greater impact on new product development that impacts the individual and society? How can we promote and stimulate the creative engineering process to thrust our research program into the highest levels of prominence?

In the last two decades, research has transitioned from a predominately industrial environment to an predominately university environment. This has placed the university in a more responsible role of developing research programs that result in technology transfer to industry.

The university environment incentive and promotion system is primarily based on the generation of technical publications. The profit motives of industry demand continual product innovation that causes increases in system complexity and forces time-to-market reductions. These counteracting motivating forces are not wholesome in promoting technology transfer.

But the struggling issue is: how does the university and industry cooperatively execute research that results in meaningful technology transfer? How do you structure a successful collaborative research paradigm?

"You can observe a lot just by watching."

Yogi Berra

This Berraism is a place to start. The problem is where are the outstanding university research centers to observe and emulate. There are very few today! Therefore, one must develop a research paradigm that is productive in producing outstanding graduates and simultaneously generating effective technology transfer. This is not easy to accomplish!

Since embedded systems is multidiscipline, CECS is struggling to develop strategies for promoting synergy between professors, graduate students, and industrial representatives. The high dependence on people with varying reward systems makes this extremely complicated. We have to succinctly define the research goals and motivate the people to collectively achieve the stated goals. This is easy to visualize, but so very very difficult to achieve. That is why we have to establish collective research goals as the winning strategy over any personal achievements. It has to be a total Herculean team effort!

CECS will continue to refine its research paradigm. In the meantime, CECS will diligently strive to develop a research paradigm that generates outstanding graduates, produces beneficial technology transfer, and promotes technical synergy between industry representatives and CECS research affiliates and graduate students.

Bob Larsen