

# CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

## Highlights

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## CECS at ICCAD

The Center for Embedded Computer Systems (CECS) was well represented at the recent IEEE/ACM International Conference on Computer Aided Design (ICCAD) held November 4–8, 2001 in San Jose, California.



The following faculty affiliates were involved as follows:

- **Tony D. Givargis and Frank Vahid**

Professors Tony D. Givargis and Frank Vahid presented a paper titled “System-Level Exploration for Pareto-Optimal Configurations in Parameterized System-on-Chip” at a session titled “System-Level Exploration and Design.” This paper defined a technique for efficiently exploring the configuration space of a parameterized system-on-chip (SoC) architecture to find all pareto-optimal configurations. These configurations represent the range of meaningful power and performance tradeoffs that are obtainable by adjusting

parameter values for a fixed application mapped onto the SoC architecture. The approach extensively prunes the potentially large configuration space by taking advantage of parameter dependencies. This technique has been successfully incorporated into a parameterized SoC tuning environment (Platune) and applied to a number of applications.

- **Nikil D. Dutt and Rajesh K. Gupta**

Professors Nikil D. Dutt and Rajesh K. Gupta served as members on the Technical Program Committee.

- **Sandeep Shukla**

Visiting Researcher Sandeep Shukla

served as moderator of the session titled “Convergence of Abstractions in High-Level Synthesis”

- **Pai Chou**

Professor Pai Chou served as moderator of the session titled “Real Time Scheduling and Performance Analysis”

- **Nikil D. Dutt**

Professor Nikil D. Dutt served as moderator of the session titled “Power Issues in High Level Synthesis”

- **Tony D. Givargis**

Professor Tony D. Givargis served as moderator of the session titled “Power Saving Techniques for Embedded Proces-

## CECS at ISSS

The Center for Embedded Computer Systems (CECS) was also well represented at the recent IEEE/ACM 14th International Symposium on System Synthesis held September 30–October 3, 2001 in Montreal, Canada. Professor Fadi Kurdahi served on the Steering Committee and Professors Nikil Dutt, Daniel Gajski, and Frank Vahid served on the Technical Program Committee.

The following technical papers were presented:

- “APEX: Access Pattern Based Memory Architecture Exploration”, P. Grun, N. Dutt, and A. Nicolau
- “RTL Semantics and Methodology”, B. Bailey and D. Gajski
- “Interoperability as a Design Issue in C++ Based Modeling Environments”, F. Doucet, R. Gupta, P. Schaumont, S. Shukla, and M. Otsuka
- “Data Cache Energy Minimization Through Programmable Tag Size Matching to Applications”, P. Petrov and A. Orailoglu
- “Conditional Speculation and its Effects on Performance and Area for High Level Synthesis”, S. Gupta, N. Savoiu, N. Dutt, and A. Nicolau
- “A Data Scheduler for Multi-Context Reconfigurable Architectures”, M. Sanchez-Elez, R. Maestre, M. Fernandez, R. Hermida, F. Kurdahi, and N. Bagherzadeh
- “Functional Abstraction Driven Design Space Exploration of Heterogeneous Programmable Architectures”, P. Mishra, N. Dutt, and A. Nicolau

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### Vahid Sabbatical

Professor Frank Vahid recently completed a 3 month research sabbatical at the Technical University of Catalunya (known as UPC) in Barcelona, Spain. UPC is one of the world's premier universities in computer architecture research. Professor Vahid hoped to gain research insights on how innovative computer architectures could be applied to embedded system architecture and design methodologies. Professor Rosa Badia of UPC, who's current research emphasizes reconfigurable computing for embedded systems, was his academic host.

Most computer architecture research focuses on high-performance techniques for desktop and server processors, and numerous advanced techniques exist, many of which were developed at UPC. Modifying those techniques for embedded systems applications can be quite fruitful. For example, caching traditionally has been used to improve performance, but exceptionally small low-power caches can actually reduce



overall power consumption. One result of this research sabbatical was the development of a variety of small-loop caching schemes specifically designed for embedded systems having fixed programs, achieving low power without any degradation in performance. He also began investigations on how binary translation techniques could be applied to platform-based computer designs.

During his sabbatical, Professor Vahid presented a research paper at the Workshop on Compilers and Operating Systems for Low Power (COLP), held in conjunction with the Conference on Parallel Architectures and Compilation Techniques (PACT), both of which were organized by UPC this year and held in Barcelona. His paper on "Propagating Constants Past Software to Hardware Peripherals" was selected for the Best Paper Award, and as such will be published in an upcoming issue of the ACM Computer Architecture (SigArch) Newsletter.

### Visitation

Dr. Wolfgang Müller, Head of Visual Interactive Systems, Cooperative Computing and Communication Laboratory, University of Paderborn, Paderborn, Germany visited CECS from November 26–30, 2001. He has developed formal execution semantics for VHDL and SystemC. During his visit, he collaborated with Research Specialist Dr. Rainer Dömer and Graduate Student Andreas Gerstlauer to write a paper titled "Formal Execution Semantics of SpecC" which will be submitted to the 2002 Design Automation Conference for technical program consideration.

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### Visiting Researcher

Marika Saarela from Stockholm, Sweden will spend November 2001 through May 2002 as a Visiting Researcher at CECS. She is studying for a Master's degree from the Royal Institute of Technology (known as KTH) in Stockholm, Sweden. She will be performing her Master's degree research and thesis under the guidance of Professor Rajesh K. Gupta. She will be developing an advanced graphical user interface for a system level specification simulator.

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### Research Grant

- Professor Rajesh K. Gupta and Visiting Researcher Sandeep K. Shukla received an \$85,413 research grant from the University of California Communications Research Program (CoRe) for the development of a design environment to synthesize single-chip networked embedded systems. This design environment will enable design conceptualization, modeling, and validation through executable system models. Mindspeed Technologies, Inc. is providing \$38,000 of the total industry-university cooperative research grant and Alan Taylor, Director, SOC Development Tools Technology will act as technical advisor.

#### FROM PAGE 1 CECS AT ISSS

Professor Rajesh Gupta served on a panel discussion titled: "New Design Paradigms: What Needs to be Standardized".

## Professor Profile

CECS is proud to profile Professor Nikil D. Dutt, Department of Information and Computer Science, University of California, Irvine (UCI), as an outstanding research affiliate. Professor Dutt received a BE from Birla Institute of Technology and Science, Pilani, India in 1980, an MS from Pennsylvania State University in 1983, and a PhD from the University of Illinois at Urbana-Champaign in 1989. He has been a professor at UCI since 1989 and currently holds a joint appointment in the Department of Electrical and Computer Engineering. He is the recipient of the Distinguished Undergraduate Teaching Award at UCI in 1999, 1999, and 2001. In 2001 he received the ACM SIGDA Distinguished Lecturer Award.



Professor Dutt's research lies at the intersection of compilers, architectures, and computer-aided design, with a specific focus on the exploration, evaluation, and design of domain-specific embedded systems. His research activities have led to the development of EXPRESSION, a novel architectural description language that facilitates rapid exploration of programmable embedded systems, as well as automatic generation of software toolkits supporting embedded systems development. His other research interests include low-power compilation and synthesis, validation and verification of pipelined processors, and memory architecture exploration for embedded systems.

Professor Dutt is coauthor of over 150 technical journal articles, member of several program and organizing conference committees, and the coauthor of the following book:

- "Memory Issues in Embedded Systems-on-Chip", P. R. Panda, N. D. Dutt, and A. Nicolau, Kluwer Academic Publishers, 1998

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## Graduate Student Profile

CECS has selected Andreas Gerstlauer to be profiled as an outstanding graduate student. He was born in Stuttgart, Germany and received a Dipl. Ing. in Electrical and Computer Engineering from the University of Stuttgart, Stuttgart, Germany in 1997. In 1998, he received an MS in Information and Computer Science from UCI. During the academic year 1992/1993 he was a graduate exchange student in electrical engineering at Oregon State University, Corvallis, OR. During his undergraduate studies he served an internship as a Software Engineer in the Böblingen Instruments Division (BID), Hewlett-Packard GmbH, Stuttgart, Germany. He was the recipient of a 2000–2001 Motorola Research Fellowship.

His PhD research is focused on developing, defining, and implementing a system level design methodology with emphasis on modeling of systems and architectures at different levels of abstraction for simulation, synthesis, and analysis. His thesis is titled "Architecture Exploration in the SpecC Environment" and is being supervised by Professor Daniel D. Gajski.

At the Asia South Pacific Design Automation Conference in January 30–February 2, 2001 he was a presenter at a tutorial titled "SpecC Language and Design Methodology". At the 2001 Design Automation and Test Conference in Europe (DATE) in March 13–16, 2001 in Munich, Germany he was a presenter at a tutorial titled "SpecC Language and Design Methodology". At this year's 2002 DATE he will be a presenter at a tutorial titled "System Level Specification Beyond RTL".

Andreas is the coauthor of the following books:

- "SpecC: Specification Language and Methodology", Daniel D. Gajski, Jianwen Zhu, Rainer Dömer, Andreas Gerstlauer, Shuqing Zhao, Kluwer Academic Publishers, 2000
- "System Design: A Practical Guide with SpecC", Andreas Gerstlauer, Rainer Dömer, Junyu Peng, Daniel D. Gajski, Kluwer Academic Publishers, 2001



The following were published by CECS faculty affiliates during the period of October 1, 2001 to December 31, 2001:

Focus	Title, Authors, Publication
<i>Design Space Exploration</i>	"Functional Abstraction Driven Design Space Exploration of Heterogeneous Programmable Architectures", Prabhat Mishra, Nikil Dutt, and Alex Nicolau, Proceedings of the 14th International Symposium on System Synthesis (ISSS), October 1-3, 2001, pp 256-261
	"Architecture Description Language Driven Design Space Exploration in the Presence of Coprocessors", Prabhat Mishra, Frederic Rousseau, Nikil Dutt, and Alex Nicolau, 10th Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI), Nara, Japan, October 18-19, 2001
<i>Automatic Validation</i>	"Automatic Validation of Pipeline Specifications", Prabhat Mishra, Nikil Dutt, and Alex Nicolau, Proceedings of the 6th IEEE International Workshop on High Level Design Validation and Test (HLDVT), November 7-9, 2001, pp 9-13
<i>System Level Exploration</i>	"System-Level Exploration for Pareto-Optimal Configurations in Parameterized System-on-Chip", Tony Givargis, Frank Vahid, and Jörg Henkel, IEEE/ACM Digest of Technical Papers for the International Conference on Computer Aided Design (ICCAD 2001), November 4-8, 2001, pp 25-30
<i>Internal representation</i>	"Internal Representation for RTL Design Methodology", Dongwan Shin and Daniel Gajski, UCI ICS Technical Report #01-66, June 29, 2001
<i>Scheduling</i>	"Scheduling in RTL Design Methodology", Dongwan Shin and Daniel Gajski, UCI ICS Technical Report #01-65, July 1, 2001
<i>Cache Management</i>	"Dynamic LO Cache Management with History Based Prediction", Weiyu Tang, Rajesh Gupta, Alex Nicolau, and Alex Veidenbaum, UCI ICS Technical Report #01-64
<i>Power Savings</i>	"Power Savings in Embedded Processors Through Decode Filter Cache", Weiyu Tang, Rajesh Gupta and Alex Nicolau, UCI ICS Technical Report #01-63
<i>Fetch Adaptation, Stream Buffer</i>	"Fetch Size Adaptation Versus Stream Buffer for Media Benchmarks", Weiyu Tang, Rajesh Gupta, Alex Nicolau, and Alex Veidenbaum, UCI ICS Technical Report #01-62
<i>Predictive Filter Cache</i>	"Design of a Predictive Filter Cache for Energy Savings in High Performance Processor Architectures", Weiyu Tang, Rajesh Gupta and Alex Nicolau UCI ICS Technical Report #01-61
<i>Dynamic Management Strategies</i>	"Competitive Analysis of Dynamic Management Strategies for Systems with Multiple Power Saving States", Sandra Irani, Sandeep Shukla, and Rajesh Gupta, UCI ICS Technical Report #01-60
<i>Execution Semantics</i>	"The Formal Execution Semantics of SpecC", Wolfgang Müller, Rainer Dömer, and Andreas Gerstlauer, UCI ICS Technical Report #01-59, November 30, 2001
<i>Power Management</i>	"Algorithms for Adaptive Dynamic Power Management: An Empirical Competitive Approach", Sandra Irani, Sandeep Shukla and Rajesh Gupta, UCI ICS Technical Report #01-58, December 18, 2001
<i>Threading Structures</i>	"Design for Synthesis, Transform for Simulation: Automatic Transformation of Threading Structures in High-Level Systems Models", Nick Savoie, Sandeep Shukla, and Rajesh Gupta, UCI ICS Technical Report #01-57, December 18, 2001
<i>Validation</i>	"Architecture Description Language Driven Validation of Processor, Memory, and Co-Processor Pipelines", Prabhat Mishra, Nikil Dutt, and Alex Nicolau, UCI ICS Technical Report #01-55, July 2001
<i>Model Checking</i>	"A Model Checking Approach to Evaluating System Level Dynamic Power Management Policies for Embedded Systems", Sandeep K. Shukla and Rajesh K. Gupta, HLDVT, November 2001



*Center for Embedded Computer Systems, University of California, Irvine*

*CECS Mission Statement:*

*To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.*

**CECS Research Advisory Board**

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## Pico-Technology Anyone?

*"Don't try to predict the future, it will always fool you."*



The history of microelectronics engineering, since the 1960's, has been the dramatic

trend of shrinking device geometries and increasing system performance while decreasing system cost. This miniaturization trend has not gone unnoticed by mechanical engineers and researchers. Now we have nanometer-sized circuits, sensors, and mechanical components evolving from a research domain known as *microelectromechanical*

*systems or MEMS*. The next research frontier will center around pico-technology.

In 1965, Gordon Moore predicted that competitive market forces would continue to push semiconductor technology progress at the same rate into the future. Now in 2002, pico-technology must become a reality for Moore's Law to continue its aura.

Pico-technology will challenge the chemistry and physics of materials. Now we need biologist, chemists, and physicists to join the pico-technology crusade. Pico-technology will lead to new architectures, circuits, sensors, activators, motors, displays, and communications technologies. The impact of pico-technology on future embedded systems will be dramatic; stressing our imagination and

creativity.

I believe pico-technology will transform our entire society and its infrastructure. We must start structuring our future research programs to the challenges of pico-technology if America wishes to maintain its world leadership role.

If anyone in industry or government is concerned about pico-technology issues as it relates to future embedded systems applications and desires to become involved in formulating future research issues, please contact me. You will get my immediate attention. Let's communicate!

As that eminent theoretician, Yogi Berra (New York Yankees Catcher 1946-1963), once said, "The future ain't what it used to be."

Bob Larsen