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CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

CECS’ Performance at ASP-DAC 2007

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The 12th Asia and South Pacific Design Automation Conference (ASP-DAC 2007) opened on January 23 at Pacifico Yokohama, with a set of tutorials by well-known research groups around the world.

One of the most visible tutorials was entitled, “Concepts and Tools for Practical Embedded System Design”. The tutorial was organized by Prof. Nikil Dutt from UC Irvine; Prof. Daniel Gajski and Dr. Andreas Gerstlauer from the same university were the speakers.

Prof. Gajski started by listing the issues of present off-the-shelf design methodologies. With current approaches, simulation can be done, but synthesis or verification is impossible. Therefore, it is necessary to establish a system design environment applicable for practical use based on concepts of model algebra. Such a model algebra is at the core of a design methodology which enables design space exploration through refinement from a specification model.

Dr. Gerstlauer pointed out first that, on the one hand, system design is a translation between different degrees of abstractions in the models. It was shown that the degree of abstraction of a model can be separated into two axes, "Communication" and "Computation". Then, the abstraction level of a model de-

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Highlights

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- Miniature Medical Sensors

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AWARDS

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NEWS

Prof. Nikil Dutt and PhD candidate Sudeep Pasricha delivered a very successful tutorial titled "SoC Communication Architectures: Technology, Current Practice, Research and Trends" at the 20th International Conference on VLSI Design held in Bangalore, India, Jan 6-10, 2007. (http://vlsi2007.vlsiconference.com)

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Pictures by Gunar Schirner

Front Page: Yokohama Pacifico by day
Left: Yokohama Pacifico by night

scription can be classified into three points each, "Un-timed", "Approximate-timed" and "Cycle-timed". Based on that, the problems of present ESL modeling approaches were pointed out. Namely, current methods only support a horizontal integration of each model/part on each abstraction level. On the other hand, they are lacking approaches for vertical, synthesis-centric integration between abstraction levels.

As one solution for this problem, Dr. Gerstlauer introduced communication modeling based on the OSI reference model which is commonly used for expressing network architectures. Furthermore, the fact that model generation becomes possible by adding some restrictions on design space exploration was shown. Regarding the order in which certain design steps are performed, these restrictions define when and where each part is synthesized (composition).

By adopting the OSI reference model structure, each design decision becomes equivalent to an increase in the level of detail when introducing additional layers of the OSI model. Since layers are synthesized corresponding to decisions and since there is a close match, debugging becomes possible.

These ideas were included into the ELEGANT system which was commissioned by the Japanese Aerospace Exploration Agency (JAXA) and which is currently under evaluation.

Next, Prof. Gajski pointed out the problematic points with present synthesis and verification solutions. As systems grow in complexity, logic-level simulations can not complete within limited amounts of time and model checking approaches grow exponentially in terms of memory requirements. In addition, in mixed HW/SW systems problems related to their interfaces become more complicated. Furthermore, formal verification methods for proving equivalence of higher-level models are not available. Current LEC (Logic Equivalence Checking) and SEC (Sequential Equivalence Checking) techniques are not applicable to higher levels above RTL.

As possible candidates for solutions, unified models of HW and SW and a methodology which includes model formalizations and automatic model generation were suggested. In terms of hardware synthesis, problems with the capacity and quality of existing, commercially available HW synthesis tools were pointed out. These tools are limited in the size of the logic they can handle, and they can not synthesize HW

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EVENTS

AWARD

Nikil Dutt, professor of computer science, has been awarded the title of Chancellor's Professor effective November 1. The title recognizes scholars who have demonstrated unusual academic merit and whose continued promise for scholarly achievement makes them of exceptional value to the university. Dutt's research areas include compilers, architectures and computer-aided design, with a specific focus on the exploration, evaluation and design of domain-specific embedded systems that span research issues in hardware, software, networked, and ubiquitous systems.

CHECK OUT CECS's SEMINARS, COLLOQUIUM, & DISTINGUISHED LECTURE SERIES::

Some past lectures have included:

Research Challenges in High Performance VLSI/SoC Circuits and Systems
Professor Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester

Automatic Parallelization with Hybrid Analysis
Dr. Lawrence Rauchwerger
Parasol Lab
Department of Computer Science
Texas A&M University

From Service Composition to Gadget Composition: Enabling Process-oriented Web
Dr. Sinisa Srbljic
School of Electrical Engineering and Computing
University of Zagreb, Croatia

Arithmetic Optimizations for System Design
Dr. Farzan Fallah
Fujitsu Laboratories

Embedded Control Software Engineering Methods and Tools Research at ISL, Bangalore
Dr. S. Ramesh
Technical Fellow, India Science Lab., GM R&D Labs, Bangalore, INDIA

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and SW simultaneously.

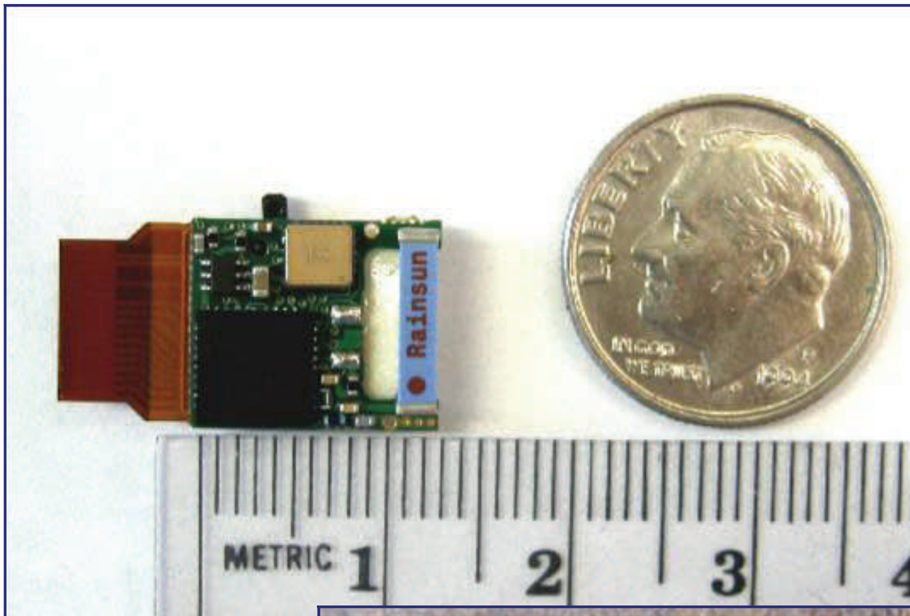
Prof. Gajski explained that in the future there is no need to design or verify RTL models when using NISC (No Instruction Set Computer) technology. Furthermore, using NISC as proposed by Prof. Gajski, productivity improvements of up to 1000 times were shown. Such gains have already been achieved in experiments using FPGAs.

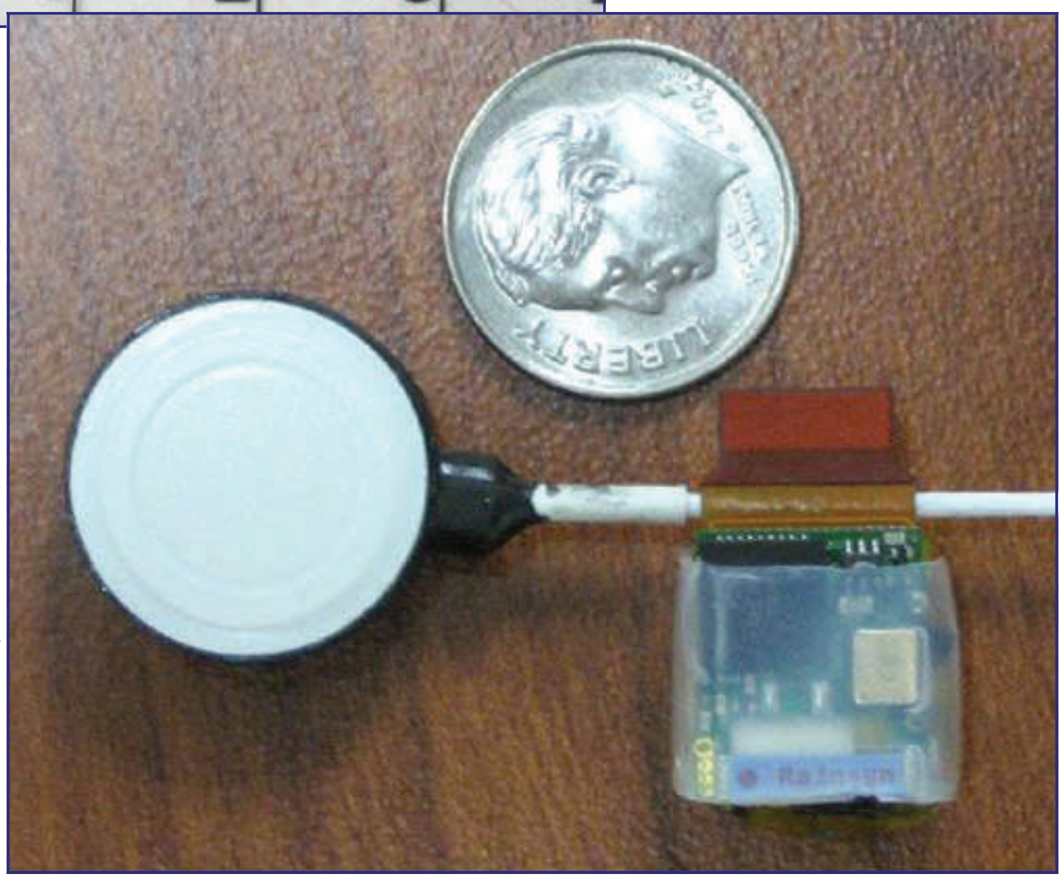
Finally, Prof. Gajski summarized the tutorial by concluding that any design methodology can be formed using three models (system specification model, transaction-level model, pin/cycle-accurate model), any design can be implemented using four components (processors, memory, transducers/bridges, arbiters), and any design methodology can be realized using two types of tools for TLM generation and RTL synthesis.

Hiroyuki Yagi, Semiconductor Technology Research Center (STARC)
Tsuneo Kinoshita, Center for Embedded Computer Systems (CECS)

PROJECT PROFILE

Fast, Reliable, Wireless Links for Miniature Medical Sensors





Professor Pai H. Chou's group is working on a UC Discovery project to enable fast, reliable wireless communication links for wearable medical sensors. The industry sponsor is QUASAR, Inc., in San Diego, CA (http://www.quasarusa.com/). QUASAR is the maker of new types of ECG, EEG, and many other novel medical sensors.

Currently, medical sensors rely on wires for carrying data signals and power, but wires are cumbersome. The emergence of low-cost, high-performance radio frequency integrated circuits (RFICs) will not only make it more convenient but will also enable mobility of the subject. However, it is very challenging to make these small wireless interfaces work well. Solutions have been developed for wireless sensor networks, but they predominantly assume low duty cycled operation and very low communication bandwidth. Although high-speed wireless interfaces are also available, they are either too large, consume too much power, or cannot deliver the required bandwidth or meet the latency constraints. This problem is particularly challenging for miniature sensors with small batteries and antennas.

The approach taken by the UCI group is twofold. First, QUASAR's sensors are interfaced with Eco, an ultra-compact wireless sensor platform previously developed at Prof. Chou's lab. It is among the world's smaller, if not the smallest, wireless sensor platform, fitting in a 1 cubic-cm volume including the antenna and battery. Second, new real-time communication protocols and system scheduling techniques are being developed to optimize the entire communication path.

The work will be the first of its kind in producing affordable, versatile, robust, wireless biosensing devices with high-impact applications. It will advance the state of the art in both the biomedical devices community and in wireless sensor networks by demonstrating real, working prototypes.

Profiles

Student Profile

Lochi Yu

This is Lochi Yu, he is from Costa Rica. He has been working with Dr. Gajski since September '06 on how to automatically generate Transaction Level Models of Embedded Systems. These models should be an executable SystemC model, which would enable designers to quickly test out their code in any platform they like, and see it execute. Also, part of his research is to make the platforms verifiable. The overall contribution would be the shortening of the design cycle (since systems are getting more complex every day) by building high-level simulatable and verifiable transaction level models.

Lochi got his Master's degree in Stanford University and completed his previous studies in his home country. He was born in Taiwan, but grew up and has lived all of his life in Costa Rica (he speaks Spanish better than he does Chinese), where he studied medicine at the University of Costa Rica. After a few years of medical practice, Lochi went back and got his BS in Electrical Engineering. After that, he came to the US. He would like to go back to Costa Rica and teach at the University of Costa Rica after getting his PhD.

Visitor Profile

Yoshinori Takeuchi

Yoshinori Takeuchi is visiting CECS from the Graduate School of Information Science and Technology at Osaka University in Japan. He is working here on a System-on-Chip exploration method that considers memory configuration, for which he hopes to develop an efficient SoC exploration method with memory synthesis.

Yoshinori has been enjoying his time at CECS and says everyone is very friendly, "especially Professor Dutt and the ACE lab people, who treated me like a real member of their lab." He sees that the CECS faculty members work hard to accomplish their research and willingly join together with graduate students, and he feels that the sincere discussions he is able to engage in with the CECS faculty and staff, and the frequent distinguished lectures that the department often offers are greatly helpful to him.

Takeuchi is also enjoying the California atmosphere and the nearby coasts. He says, "There are many people from all over the world gathered here in order to pursue the American dream and work hard. I envy the people in CECS because they enjoy their research and their life in such a good place like here. If I have another chance to take a sabbatical, I would like to come again to CECS at UCI."

PUBLICATIONS

The following were published by CECS faculty affiliates from December 2006 to March 2007

Focus	Titles, Author, Publication
Platform Modeling	**"Transaction Level Platform Modeling in SystemC for Multi-Processor Designs,"** Lochi Yu, Samar Abdi, Daniel Gajski, TR 06-15, January 2007.
Dynamically Reconfigurable Architectures	**"Selecting Granularity of Parallelism for Tasks executing on Dynamically Reconfigurable Architectures,"** S. Banerjee, E. Bozorgzadeh, N. Dutt, TR 06-14, December 2006.
System Prototype Program Interface	**"Iterative System Tuning for Proactive Systems by Formal Verification and System Prototype: System Prototype Program Interface,"** Minyoung Kim, Mark-Oliver Stehr, Carolyn Talcott, Kyoungwoo Lee, Nikil Dutt, Nalini Venkatasubramanian, TR 07-02, January 2007.
Multifaceted Modeling	"**Abstract, Multifaceted Modeling of Embedded Processors for System-Level Design**", G. Schirner, A. Gerstlauer, R. Dömer, ASP-DAC'07 , January 2007.
Interactive Recoding	**"Creating Explicit Communication in SoC Models Using Interactive Re-Coding"**,P. Chandraiah, J. Peng, R. Dömer, S. Pasricha, N. Dutt, M. Ben-Romdhane, ASP-DAC'07, January 2007.
ESE Front End	**"ESE Front End,"** D. Gajski, A. Gerstlauer, R. Doemer, S. Abdi, J. Peng, D. Shin, R. Ang, University of California, Irvine, March, 2006.
ESE Back End	**"ESE Back-End,"** D. Gajski, S. Abdi, R. Ang, A. Gerstlauer, J. Peng, D. Shin, R. Doemer, University of California, Irvine, March, 2006.
AMBA Bus	**"Quantitative Analysis of Transaction Level Models for the AMBA Bus,"** G. Schirner and R. Doemer, University of California, Irvine, March 2006.
VLSIDAT	**"VLSIDAT Keynote: New Strategies for System Level Design,"** D. Gajski, University of California, Irvine, May 2006.

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Center for Embedded Computer Systems, University of California, Irvine

CECS *Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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