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CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Special Text-Heavy Project Issue!

Highlights

- Dr. Gajski's honorary doctorate
- Pasricha and Dutt take ASPDAC 2006 Best Paper Award
- Project Profiles

Inside this Issue:

Dr. Gajski Receives Honorary Doctorate

Professor Daniel Gajski has been presented with an Honorary Doctorate from the University of Oldenburg, Germany in recognition of his contributions in the areas of Embedded Systems and Design Science. In the early 1980s, Dr. Gajski invented key concepts for the design of custom processors which are now widely used in the EDA industry. Later, he made seminal contributions for the synthesis and verification of multi-processor embedded systems. Dr. Gajski is currently the Henry Samueli "Turing" Endowed Chair and Director of the Center for Embedded Computer Systems at the University of California, Irvine.

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Dutt, Pasricha Receive ASPDAC Best Paper Award

A research paper by CECS graduate student Sudeep Pasricha and Professor Nikil Dutt was selected for the Best Paper Award at the prestigious Asia and South Pacific Design Automation Conference (ASPDAC) held in Yokohama, Japan from January 24 - 27, 2006. The research paper, titled "Constraint-Driven Bus Matrix Synthesis for MPSoC" proposes novel techniques to reduce the cost and development time of communication architectures used in the design of high-performance electronic systems built into next-generation electronic devices, including mobile phones, video game consoles and high-speed networking equipment. The paper was selected out of 424 submitted papers from 27 countries. The research is supported by the Semiconductor Research Corp., a non-profit consortium of semiconductor companies, and was done in collaboration with Conexant Systems, Newport Beach.

"The efficient synthesis of on-chip communication architectures during the design of complex Systems-on-Chips (SoCs) is a critical bottleneck in the efficient realization of complex applications mapped onto silicon platforms," said Dutt. "This award underscores the potential impact of the work on the design process for next-generation

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PROJECT PROFILES

No-Instruction-Set Computer (NISC) :: http://www.cecs.uci.edu/~nisc

Using processors and high-level languages is necessary for tackling complexity of increasing larger building blocks in today's System-on-a-Chip designs. However, meeting performance and power constraints demands customization of processors towards a specific application. The instruction-set of a processor is an abstraction layer that separates the software compilation from actual execution in hardware. Historically, in order to improve the efficiency and flexibility of processor generations, the trend has always been to simplify the instruction-set and give the compiler more control over the execution in hardware. Two examples of such trend are migration from CISC (Complex-Instruction-Set Computer) to RISC (Reduced-Instruction-Set Computer), and from superscalar computers to VLIW (Very Large Instruction Word) computers.

On the other hand, since developing a compiler is a very complex and time-consuming task, enabling processor customizations requires a compiler technology that is instruction-set independent and, ideally, can be used for all types of processors.

The NISC technology offers a new approach for design of custom processors and IPs. It removes instructions to enable faster execution and better customization. Without instructions, the NISC compiler has full control of all the components and connections in a given datapath. The full compiler-level control helps in achieving better resource utilization. Additionally, the NISC technology significantly improves time-to-market of custom processors by eliminating instruction-set design phase.

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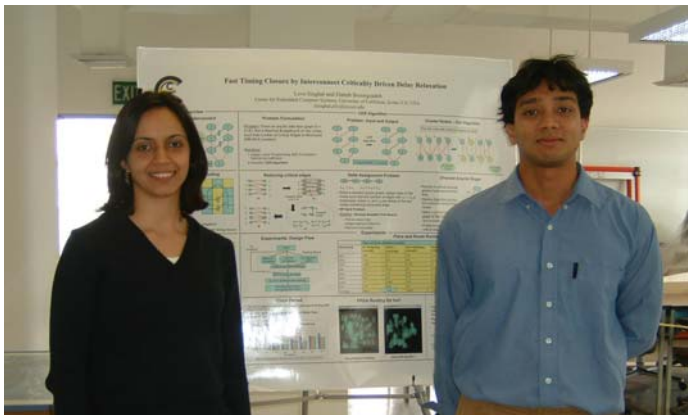
Time Budgeting :: Submitted by Love Singal

Design complexity requires optimization techniques to be applied in multiple stages, starting from high level abstraction and ranging to gate level and physical design. In order to reduce the complexity, each design is decomposed into a set of sub-designs or sub-tasks.. The sub-designs along the critical paths are the most constrained components. However, timing constraint can be loose on other sub-designs and, therefore, the allowable delay allocated to such sub-design can be greater than actual/intrinsic delay of the sub-design. This excess delay is referred to as *delay budget* (or *timing budget*). The delay budget can be used to improve design quality such as area and power. A slower design can take less device area. For example, a slower ripple carry adder can be implemented in less area than a faster carry look ahead adder. Researchers have tried to find the algorithms to improve the delay budget allocation. In ICCAD 2004, Dr. Eli Bozorgzadeh and her collaborators found a polynomial time algorithm to maximize the total delay budget allocation. .



When the delay budget is maximized, however, the timing dependency between the components can increase; ultimately, this increases the number of critical edges in the design. Critical edges are interconnects with zero timing slack, and they can have major impact on design quality at various design levels. For example, critical wires determine clock period in a design. If a design has strict timing constraint, critical interconnects could make the routing of the wires very complicated or could violate the timing constraints. The interconnect delay is very significant in field programmable gate arrays (FPGA). In FPGA devices, wires are connected to each other through programmable switches. These switches provide configurability to the interconnect but in-

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Student Profile

Aviral Shrivastava

Originally from India, Aviral Shrivastava joined CECS in June of 2000. He completed his undergraduate studies in computer Science and Engineering at the Indian Institute of Technology in Delhi and has found much success at UC Irvine, having collaborated with several people within CECS, Prahbat Mishra from the University of Florida, Gainesville, and Eugene Earlie from Strategic CAD labs in Intel.

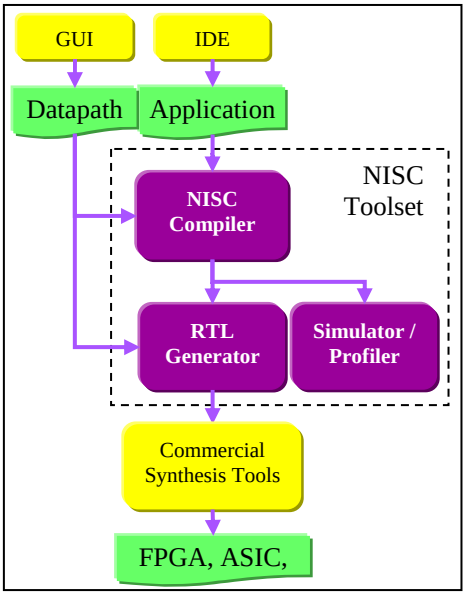
Currently, Aviral is working with Professor Nicolau and Professor Dutt on introducing the role of the compiler when utilizing architectural features. Aviral and collaborators observed was that the compiler has significant impact on the eventual power and performance of the processor. As a result, the processor designer should include compiler effects while designing a processor. Until the compiler is modified to exploit the architectural feature, the true usefulness of the architectural feature cannot be measured. Aviral has proposed a systematic approach, called "Compiler-in-the-Loop Architecture Exploration" which weaves in the compiler effects while exploring the architectural feature. His group has shown that traditional evaluation (without considering compiler effects) can lead to sub-optimal design decisions. Using Aviral's technique, it is possible to meet all the design constraints and design optimized embedded systems.

Aviral's work paves the way for building high performance, low-power electronic devices. His work enables building lighter cell phones and laptops with longer lasting batteries that will require only infrequent charging. His work also opens up opportunities for higher levels of integrations in electronic devices.

NISC Project, cont'd from page 2

Moreover, one NISC tool-set is sufficient for all possible datapaths. Therefore, NISC is the ultimate processing element for custom IP design.

The NISC toolset consists of a NISC Compiler and an RTL Generator. The inputs of the compiler are the application C code, and the processor datapath captured in NISC Generic Netlist Representation (GNR). The output of the compiler is a stream of control words that can control all the units at each clock cycle. The inputs of RTL Generator are the processor description and the control words generated by the compiler. The RTL Generator produces synthesizable Verilog code of the processor along with synthesizable control and data memory cores. Using NISC, different custom IPs have been designed and prototyped demonstrating significant performance and power savings. The demo version of NISC toolset is available online at: http://www.cecs.uci.edu/~nisc.



The NISC project started in year 2003 under supervision of Professor Daniel Gajski. This research has been partially funded by the Semiconductor Research Corporation (SRC). PhD candidate Mehrdad Reshadi has been working on defining the architectural details of NISC, and has developed the NISC compiler. PhD candidate Bita Gorjiara has developed the RTL Generator for FPGA prototyping of NISC. She has been also working on power optimization and communication interface design for multi-NISC systems. To capture NISC architecture and the components of the library, Gorjiara and Reshadi have developed the NISC GNR that is an XML-based language. NISC-GNR and the application C code are used as inputs in their online NISC toolset. PhD candidate Jelena Trajkovic is developing algorithms that in future will be used to automatically generate NISC architectures for a given application domain.

Time Budgeting, cont'd from page 2

crease the wire delay.

To improve interconnect criticality, Love Singhal and Dr. Eli Bozorgzadeh proposed in ICCAD 2005 a problem of minimizing the number of critical edges in a graph while keeping the budgets in the graph maximal. This formulation ensures that the design takes advantage of budgets allocated on sub-designs while maintaining a minimum number of critical interconnects. This proposed problem is new. To solve the problem, we used both integer linear programming (ILP) solution and a heuristic algorithm. We applied a graph-based transformation algorithm (critical edge reduction (CER) algorithm) that is able to remove significant number of critical edges in the graph. The algorithm runs in multiple iterations and each iteration of algorithm reduces zero or more critical edges to non-critical edges. The algorithm also converges to a stable state in bounded number of iterations.

One interesting feature of our algorithm is that it allows incremental optimizations in the graph. Any sub-graph of a data flow graph can be picked up and optimized to reduce the critical edges. This provides designers with a way to create design specific optimization and exchange budget between the nodes in a deterministic way.

We showed the effect of this interesting problem on FPGA devices. FPGA architectures have significant wire delays, and critical edges have an important role in final placement and routing. If there are many critical interconnects, the sub-designs have to be placed close to each other. This adds to the congestion in the design. We used Synplicity Synplify 7.1 for synthesizing designs and Xilinx ISE 6.2 for placement and routing of designs. We found that designs that have fewer critical edges as found by our algorithm are consistently routed in much less time than designs that simply use maximum budgeting. On average the place and route runtimes were improved by 2.8 times. The figure shows the final implementation of a benchmark using two techniques. The second implementation has much less congestion and better placement.

In this work on delay budgeting, we proposed a problem of minimizing critical edges while assigning maximal delay budgets on nodes. Our algorithm effectively reduced the number of critical edges in data flow graphs and enabled incremental optimizations on the design. Our experiments show that designs with fewer critical edges have better design quality than designs with more critical edges. For future work, we will continue to study the effect of timing critical edges in designs.

More information about the work is available at http://www.ics.uci.edu/~lsinghal/res.html. For questions, comments, or feedback, contact Love Singhal (lsinghal@ics.uci.edu).

ARTIST 2 will now be publishing a newsletter to inform the larger embedded systems research and industrial community about important events of interest (workshops, summer schools, high level events, selected publications for a wide audience, etc.). The format of the newsletter will be refined over time.

For more information about the Artist2 European Network of Excellence on Embedded Systems Design, please see: http://www.artist-embedded.org/FP6/

Best Paper Award, continued from page 1

SoCs."

Sudeep Pasricha and Prof. Nikil Dutt also gave a half day tutorial titled **"**SoC Communication Architectures: Current Practice, Research and Trends" at the same conference. The tutorial presented in detail the current research efforts and future trends in the increasingly critical area of communication architecture design for contemporary system-on-chip designs.

The Asia and South Pacific Design Automation Conference (ASPDAC) is a premier conference held annually, for researchers and engineers from all over the world to learn and discuss state of the art technologies for electronic system design, electronic design automation (EDA) and design methodologies.

Sudeep Pasricha is a fourth year PhD candidate at CECS, whose current research topics include system-on-chip (SoC) communication architecture exploration and synthesis, system-level modeling languages and methodologies, and computer-aided design for embedded systems.

Prof. Nikil Dutt, who has been awarded "best paper" honors five previous times at various conferences, is also affiliated with the Center for Embedded Computer Systems and the Center for Pervasive Communications and Computing. He is the author of five books and nearly 50 professional journal articles. He is the editor-in-chief of ACM Transactions on Design Automation of Electronic Systems and an associate editor of ACM Transactions on Embedded Computer Systems. He was an ACM SIGDA distinguished lecturer during 2001-2002, and an IEEE Computer Society distinguished visitor for 2003-2005.

EVENTS

New Technology in Japan by Sudeep Pasricha

Recently while visiting Japan to attend the ASPDAC conference in Yokohama, I found some time to slip away to Tokyo for a day. There I visited Akihabara, Tokyo's renowned electronics district, and was absolutely blown away by what I saw. I had heard tales of stores specializing in selling nothing but little robots, of shops full of tiny cameras, music players and kitchen gizmos, and it was all true! Thinking about all the tiny embedded systems in these tiny funky looking gadgets on display was enough to almost bring a tear to the eye – what great fortune to be doing research in such a vibrant area! Like a kid searching for a sugar-fix who'd just stumbled upon an all-you-can-eat candy buffet, I made my way through the brightly lit streets and byways of this technological Mecca.

No matter where you travel in Japan, you will reach an inescapable conclusion – the Japanese love their cell phones. You rarely see a person on the street or the subway without one. Almost all of the cell phones sold in Japan have an impressive array of features – high quality digital cameras which can shoot both still images and video, and the ability to watch TV shows and high quality video clips on the move are almost ubiquitous. One very interesting feature that I noticed in some of the cell phones was the ability to use smart chips embedded in them to pay for purchases in convenience stores, train ticket counters and even some vending machines. RFID chips in phones also allow parents, schools, and hospitals to monitor children, the elderly, and patients, sending out an email alert to the user

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Dr. Gajski's Honorary Doctrine Celebration


Nordwest-Zeitung Samstag 11.02.2006

„Held der Informatik" macht Handys flott

UNI Dr. Daniel Gajski ist Ehrendoktor

OLDENBURG/LS – Die Universität Oldenburg hat den amerikanischen Informatiker Professor Dr. Daniel G. Gajski gestern mit der Ehrendoktorwürde „Doktor-Ingenieur honoris causa" ausgezeichnet. Sie würdigte damit seine „außerordentlichen wissenschaftlichen Leistungen im Gebiet der Entwurfsmethodik und -automatisierung eingebetteter mikroelektronischer Systeme". Sie sind ein wesentlicher Beitrag dafür, dass heute komplexe IT-Systeme wie Handys und Computer entwickelt werden können. Gajskis Arbeiten und Lehrbücher hätten einen wesentlichen Einfluss auf Forschung und Lehre, sagte Professor Dr. Claus Möbius, Direktor des Departments für Informatik der Uni. Professor Dr. Franz Josef Rammig (Uni Paderborn) charakterisierte Gajski in seiner Laudatio als „Genie" und „Helden der Informatik".

PUBLICATIONS

The following were published by CECS faculty affiliates from October 2005 to March 2006

Focus	Titles, Author, Publication
Queue Design with Speculative Pre-Execution	"A Low-Complexity Issue Queue Design with Speculative Pre-Execution," W.W Ro and J-L Gaudiot, International Conference on High Performance Computing (HiPC 2005), December 18-21, 2005.
Strassen and ATLAS's DGEMM	"Adaptive Strassen and ATLAS's DGEMM: A Fast Square-Matrix Multiply for Modern High-Performance Systems," P.D'Alberto and A. Nicolau, International Conference on High Performance Computing in Asia Pacific Region (HPC Asia), November 30-December 3, 2005.
Fast Timing Closure	"Fast Timing Closure Through Interconnect Criticality Driven Delay Relaxation," L. Singhal and E. Bozorgzadeh, International Conference on Computer-Aided Design (ICCAD) , November 2005.
Real-World Wireless Sensing Applications	"Energy Efficient Platform Designs for Real-World Wireless Sensing Applications," P. Chou and C. Park, International Conference on Computer Aided Design (ICCAD), November 2005.
DuraNode	"DuraNode: Wireless Networked Sensor for Structural Health Monitoring," C. Park, P. Chou, and M. Shinozuka, IEEE International Conference on Sensors, Oct. 31 - Nov. 1, 2005.
Multi-Threading Microarchitectures	"Static Partitioning vs Dynamic Sharing of Resources in Simultaneous Multi-Threading Microarchitectures," C. Liu and J-L Gaudiot, International Workshop on Advanced Parallel Programming Technologies (APPT 2005), October 27-28, 2005.
Automatic Identification	"Automatic Identification of Application-Specific Funtional Units with Architecturally Visible Storage," P. Biswas and N. Dutt, Design Automation Test in Europe '06, March 2006.
Software Annotation on Mobile Devices	"Software Annotations for Power Optimization on Mobile Devices," R. Cornea, A. Nicolau, N. Dutt, Design Automation Test in Europe '06, March 2006.
COSMECA	"COSMECA: Application Specific Co-Synthesis of Memory and Communication Architectures for MPSoC," S. Pasricha and N. Dutt, Design Automation Test in Europe '06, March 2006.
Quantitative Analysis of Transaction Level Models	"Quantitative Analysis of Transaction Level Models for the AMBA Bus," G. Schirner and R. Doemer, Design Automation Test in Europe '06, March 2006.
Fast Exploration of Bypasses in Embedded Processors	"Automatic Generation of Operation Tables for Fast Exploration of Bypasses in Embedded Processors," S. Park, A. Shrivastava, N. Dutt, E. Earlie, A. Nicolau, Y. Paek, Design Automation Test in Europe '06, March 2006.
Custom Architecture for DCT	"Designing a Custom Architecture for DCT Using NISC Design Flow," B. Gorjiara, M. Reshadi, D. Gajski, ASP-DAC'06 Design Contest, January 2006.
Matrix Synthesis	"Constraint-Driven Bus Matrix Synthesis for MPSoC," S. Pasricha, N. Dutt, M. Ben-Romdhane, ASP-DAC'06, January 2006.
PARLGRAN	"PARLGRAN: Parallelism Granularity Selection for Scheduling task chains on dynamically reconfigurable architectures," S. Banerjee, E Boszorgzadeh, N. Dutt, ASP-DAC'06

CECS—*promoting creativity and pursuing discovery!*

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

Primary Contact
Leila Mironova
Center for Embedded Computer Sciences
University of California, Irvine
Email: Lmironov@uci.edu

Technology in Japan, cont'd from page 5

when the trackee travels beyond a predetermined boundary. Another cool feature available with some cell phones was the ability to read barcodes (more specifically a QR code which is a 2D bar code) – advertisements and even business cards with QR codes can be quickly scanned by cell phone, which uploads necessary contact information to the phone.

Portable media players (PMPs) seem to be selling like hotcakes in Japan. Drool-inducing handheld PMPs such as the Sorell SV-15 that had a crisp LCD screen with startling clarity even in broad daylight, and an integrated swivel-enabled 1.3MP camera to shoot images and video had me reaching for my wallet more than once. Other features in some of the fancier PMPs included wireless support to download content from your PC or the internet and the TiVo-like ability to record TV shows. The variety of PMP players that I came across in shops there easily put the displays at Best Buy, Circuit City and WalMart to shame.

While robots in the household are not yet commonplace here (except for the few of us who shelled out for the Roomba robot vacuum), the Japanese seem to be right at home with an amazing array of household robots at their beck and call. I came across Tmsuk's new household robot called *Roborior* (from the combination of "robot" and "interior"), which has the ability to monitor your house for intruders and give you a call on your cell phone if it detects any suspicious activity. Then there was *ifbot*, which is a communications robot with the ability to respond to words, ask questions and display several emotions using its LED facial expressions and subtle eye movements. My favorite was the *Asahi* bartender robot, which could open a can of beer and pour it into a chilled glass, guaranteeing a perfect head every time. The robot's body also has a fridge to hold a six-pack!

There was loads more to see – gigapixel digital cameras, ultra-suave watches with flexible displays that curve all the way around your wrist, laptops so sleek that you'd mistake them for a table mat and USB drives shaped like bottles of sake (you know .. for times when you need a quick nip on the go). It's a pity that most of these gadgets are only available exclusively for the Japanese market. American technophiles in the meantime can stoke their gadget envy by visiting http://www.akihabaranews.com/en/