CECS eNEWS

Volume 5, Issue 2, April 2005

Center for Embedded Computer Systems, University of California, Irvine

Highlights:

Inside this issue:

CECS at DATE 05

*** * * 11+ papers presented * * ***

Research affiliates and graduate students from the Center for Embedded Computer Systems (CECS) at the University of California, Irvine (UCI) presented eleven technical papers and one interactive presentation at Design, Automation and Test in Europe (DATE 05) Conference held at ICM, Messe Munich, Germany from March 7—11, 2005. Other research affiliates served as session moderators or on conference committees.

Papers

The following technical papers were presented by CECS research affiliates with the cited pages from the conference proceedings:

- *A Study of the Speedups and Competitiveness of FPGA Soft Processor Cores Using Dynamic Hardware/Software Partitioning*, Roman Lysecky, and Frank Vahid, pp 18—23
- *LORD: A Localized, Reactive and Distributed Protocol for Node Scheduling in Wireless Sensor Networks*, Arijit Ghosh and Tony Givargis, pp 190—195
- *Functional Validation of System Level Static Scheduling*, Samar Abdi and Daniel D. Gajski, pp 542—547

- *Defining an Enhanced RTL Semantics*, Shuqing Zhao and Daniel D. Gajski, pp 548—553
- *Functional Coverage Driven Test Generation for Validation of Pipelined Processors*, Prabhat Mishra and Nikil Dutt, pp 678—683
- *Lightweight Multitasking Support for Embedded Systems Using the Phantom Serializing Compiler*, Andre C. Nacul and Tony Givargas, pp 742—747
- *Generic Pipelined Processor Modeling and High Performance Cycle-Accurate Simulator Generation*, Mehrdad Reshadi and Nikil D. Dutt, pp 786—791
- *FORAY-GEN: Automatic Generation of Affine Functions for Memory Optimizations*, Ilta Issenin and Nikil D. Dutt, pp 808—813
- *System Synthesis for Networks of Programmable Blocks*, Ryan Mannion, Harry Hsieh, Susan Cotterell and Frank Vahid, pp 888—893
- *ISEGEN: Generation of High-Quality Instruction Set Extensions by Iterative Improvement*, Partha Biswas, Sudarshan Banerjee, Nikil Dutt, Laura Pozzi and Paolo Ienne, pp 1246—1251
- *PBEXPLORE: A Framework for Compiler-in-the-Loop Exploration of Partial Bypassing in Embedded Processors*, Aviral Shrivastava, Nikil D. Dutt, Alex Nicolau and Eugene Earlie, pp 1264—1270

Interactive Presentations

The following interactive presentation was made by a CECS research affiliate with the cited pages from the conference proceedings:

- *A Decomposition Approach to Partitioning Software for Microprocessor/FPGA Platforms Minimization*, Greg Stitt and Frank Vahid, pp 396—397

Session Moderators

Professor Fadi J. Kurdahi served as moderator of a session titled *Scheduling and Synthesis for Reconfigurable Computing.*

Committees

Professor Nikil D. Dutt served on the DATE 05 Executive Committee as the ACM/SIGDA representative. Professors Tony Givargas and Alex Orailoglu served as members of the DATE 05 Technical Program Committee.

Workshops

Professor Ian G. Harris served as organizer/moderator of a one day workshop titled *System Level Verification and Validation.* Professor Daniel D. Gajski presented a paper titled *SW/HW Co-Verification Through Model Formalization.*

We deeply appreciate the efforts and extend congratulations to these CECS research affiliates and their graduate students who so ably represented CECS at DATE 05. Their participation greatly contributes to promoting and maintaining our international research profile.

CECS at ASP-DAC

* * * 13 papers presented * * *

Many CECS research affiliates and their graduate students attended the Asia and South Pacific Design Automation Conference (ASP-DAC 2005) held in Shanghai, China on January 18-21, 2005. A total of 13 technical papers were presented at this highly attended Asian conference.

Papers

The following technical papers were presented by CECS research affiliates with the cited pages from the conference proceedings:

- *System-Level Communication Modeling for Network-on-Chip Synthesis*, Andreas Gerstlauer, Dongwan Shin, Rainer Domer and Daniel Gajski, pp 45—48
- *A Formalism for Functionality Preserving System Level Transformations*, Samar Abdi and Daniel D. Gajski, pp 139—144
- *Forward Discrete Probability Propagation Method for Device Performance Characterization Under Process Variations*, Rasit Onur Topaloglu, and Alex Orailoglu, pp 220—223
- *Fault Tolerant Nanoelectronic Processor Architectures*, Wenjing Rao, Alex Orailoglu and Ramesh Karri, pp 311—316
- *An Efficient Control-Oriented Coverage Metric*, Shireesh Verma, Kiran Ramineni and Ian G. Harris, pp 317—322
- *Automated Throughput-Driven Synthesis of Bus-Based Communication Architectures*, Sudeep Pasricha, Nikil D. Dutt and Mohamed Ben-Romdhane, pp 495—498
- *A Unified Transformational Approach for Reductions in Fault Vulnerability, Power, and Crosstalk Noise and Delay on Processor Buses*, Raid Ayoub and Alex Orailoglu, pp 729—734
- *Dynamic Power Management Using On-Demand Paging for Networked Embedded Systems*, Yuvraj Agarwal, Curt Schurgers and Rajesh Gupta, pp 755—759
- *A Generalized Technique for Energy-Efficient Operating Voltage Set-Up in Dynamic Voltage Scaled Processors*, Jaewon Seo and Nikil D. Dutt, pp 836—841
- *Multi-Metric and Multi-Entity Characterization of Applications for Early System Design Exploration*, Lukai Cai, Andreas Gerstlauer, and Daniel D. Gajski, pp 944—947
- *A Clustering Technique to Optimize Hardware/Software Synchronization*, Junyu Peng, Samar Abdi and Daniel D. Gajski, pp 965—968
- *On Combining Iteration Space Tiling with Data Space Tiling for Scratch-Pad Memory Systems*, Chunhui Zhang and Fadi J. Kurdahi, pp 973—976
- *Fault Tolerant Quantum Cellular Array (QCA) Design Using Triple Modular Redundancy with Shifted Operands*, Tongquan Wei, Kaijie Wu, Ramesh Karri and Alex Orailoglu, pp 1192—1195

Committees

Professor Nikil D. Dutt served on the ASP-DAC Steering Committee as the ACM/SIGDA representative. Professor Alex Orailoglu served as a member of the ASP-DAC Technical Program Committee on the Test and Design for Testability Subcommittee.

Again, CECS representatives presented a variety of technical topics to an extremely diverse international audience. We greatly appreciate their efforts in keeping CECS research programs and accomplishments visible worldwide.

"Prediction is hard, especially when it involves the future!"

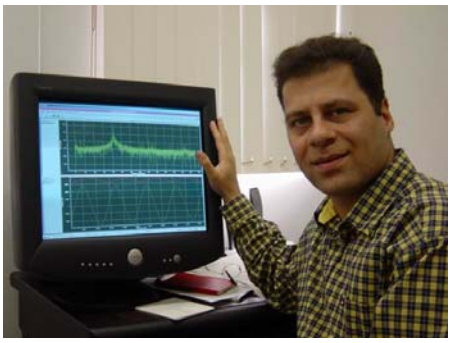
Yogi Berra

"Competition brings out the best in products and the worst in people."

David Sarnoff

Heydari Wins NSF CAREER Award

Professor Payam Heydari, Department of Electrical Engineering and Computer Science, The Henry Samueli School of Engineering, has received notification from the National Science Foundation (NSF) of an award under its Faculty Early Career Development (CAREER) Program.



His proposal was titled *Analysis and Design of Silicon-Based Performance-Optimized Integrated Circuits for High-Frequency Wideband Wireless Communication Systems* and the award is for $400,000 covering a 5 year duration. The research objective is to design novel silicon-based integrated circuits that will be widely employed in the front-end of high-performance ultra wideband (UWB) wireless communication systems. Integrating the proposed circuit topologies into next-generation high data-rate wireless communication systems will have a significant impact on law enforcement, rescue operations, and personal area networks.

The CAREER award is the NSF's most prestigious award to new faculty members. The CAREER program recognizes and supports the early career-development of those teacher-scholars who are most likely to become academic leaders of the 21st century. CAREER awardees are selected on the basis of creative, career-development plans that effectively integrate research and education within the context of the mission of their institution. The CAREER award plans should build a firm foundation for a lifetime of integrated contributions to research and education.

CECS extends congratulations to Professor Heydari on receiving this prestigious NSF award and the richly deserved accompanying recognition.

Bozorgzadeh Joins CECS

Elaheh (Eli) Bozorgadeh, Assistant Professor, Department of Computer Science, Donald Bren School of Information and Computer Science, University of California, Irvine, recently joined CECS as a Research Affiliate. Professor Bozorgzadeh was born in Tehran, Iran and received her BSEE from Sharif University of Technology, Tehran, Iran in 1998, a MS from Northwestern University in 2000, and a PhD from University of California, Los Angeles in 2003. She has been on the UCI faculty since receiving her PhD.

Professor Bozorgzadeh's research interests include design automation and synthesis of reconfigurable embedded systems, architectural synthesis and design of hybrid reconfigurable computing systems, and VLSI CAD for FPGAs and ASICs. She has authored two book chapters and 25 technical papers. She is a member of ACM and IEEE.

Professor Bozorgzadeh's most recent publications are:

- *HARP: Hard-wired Routing Pattern FPGAs*, S. Sivaswamy, G. Wang, C. Ababei, K. Bazargan, R. Kaster and E. Bozorgzadeh, Proceedings of ACM International Symposium on Field-Programmable Gate Arrays (FPGA), February 2005, pp 21-29

- *A Unified Theory for Timing Budget Management*, S. Giasi, S. Choudhuri, E. Bozorgzadeh, and M. Sarrafzadeh, ACM/IEEE International Conference on Computer-Aided Design, November 2004, pp 653-659

- *Optimal Integer Delay Budget Assignment on Directed Acyclic Graphs*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD),

Vol. 23, No. 8, August 2004, pp 1184-1199

We welcome Professor Bozorgzadeh as a CECS Research Affiliate and look forward to her contributions in enriching our research program in embedded systems.

Mishra Wins Dissertation Award at DATE 05

Assistant Professor Prabhat K. Mishra (PhD '04), Department of Computer and Information Science and Engineering, College of Engineering, University of Florida, Gainesville, FL was presented with the EDAA Outstanding Dissertation Award at the Design, Automation and Test in Europe (DATE 05) Conference held at ICM, Messe Munich, Germany from March 7—11, 2005. This award was given by the European Design and Automation Association (EDAA). Professor Mishra's thesis advisor was Professor Nikil D. Dutt.

Professor Mishra's PhD dissertation was titled *Specification-driven Validation of Programmable Embedded Systems*. The dissertation abstract follows.

"Validation of programmable embedded systems, consisting of processor cores, co-processors, and memory subsystems, is one of the major bottlenecks in current System-on-Chip (SOC) design methodology. One of the most important problems in validation of such systems is the lack of a golden reference model. As a result, many existing validation techniques employ bottom-up approach to design verification, where the functionality of an existing architecture is, in essence, reverse-engineered from its implementation. This thesis presents a top-down validation methodology that complements the existing bottom-up approaches. It leverages the system architect's knowledge about the behavior of the design through architecture specification. We have developed validation techniques to ensure that the static and dynamic behaviors of the specified architecture is well formed. The validation methodology is the ability to generate executable models from the specification for a wide variety of programmable architectures. We have developed a functional abstraction technique that enables specification-driven model generation for simulation, hardware generation, and property checking. The generated simulator and hardware models are used for design space exploration of programmable architectures. We have explored two top-down validation scenarios: design validation and test generation. First, the generated hardware is used as a reference model to verify the hand-written implementation using a combination of symbolic simulation and equivalence checking. Second, we have proposed a functional coverage based test generation technique for validation of pipelined processor architectures. The experiments demonstrate the utility of the specification-driven validation methodology for programmable embedded systems."

CECS extends congratulations to Professor Mishra on receiving this prestigious dissertation award from EDAA and the accompanying recognition.

Testing, Testing, Testing!

* * * * *

At-Speed Embedded Test

Testing system-on-chip (SoC) devices today is becoming a challenging nightmare. With SoC pin counts exceeding 1000, clock frequencies exceeding 20 GHz, and transistor counts exceeding 10 million, automatic test pattern generation (ATPG) and automatic test equipment (ATE) are being stressed to the limit. Under these stresses, testing costs are increasing at an alarming rate while striving to achieve acceptable test coverage and yields. Not to mention the first cost of ATE that exceeds $1,000,000 per machine. The answer to this alarming testing trend is At-Speed Embedded Test (ASET) for SoC devices. ASET is a custom design for test approach that utilizes boundary scan and self-test techniques to perform at-speed testing of an SoC device.

B-SCAN

Boundary Scan (B-SCAN) is a testing technique that has been under development for many years. B-SCAN has been an IEEE 1149.1 standard since 1990. B-SCAN provides each input/output bonding pad of an SoC device with a shift-register, encapsulated as a B-SCAN cell, which is coupled to the associated core logic. These B-SCAN cells are controlled by a test controller that manages the testing from a single IEEE standard 5 pin Test Access Port (TAP). The TAP controls all testing stimuli and responses from external ATE to the SoC under test.

BIST

Built-in-Self Test (BIST) uses a pseudo random stimuli generator to exercise the logic. This results in a signature pattern that produces acceptable controllability and observability metrics of all logic nodes or fault coverage criteria. The major advantage of BIST is that all testing is performed at-speed. If a custom test pattern is desired, data compression of the stimuli and corresponding response patterns can be implemented without severe real estate overhead.

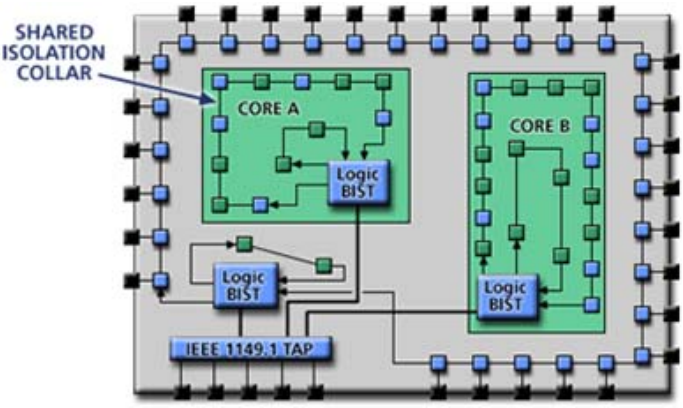
DFT

Design for Test (DFT) is a structured hierarchical testing strategy for B-SCAN-compliant and BIST-compliant blocks that eliminates the need for external testing of the SoC device using conventional ATE. That means that in the test mode, all logic must be fully synchronous and composed of scannable D-type flip-flops. Multiple clocking of functional blocks is permissible. All of the functional blocks of an SoC are connected to the B-SCAN TAP to allow for simple external programmability and controllability. The additional logic required for DFT can be implemented at the RTL level to enable cost effective design synthesis and verification.

ASET

At-Speed Embedded Test (ASET) is a hierarchical DFT strategy that is predicated on at-speed testing of an SoC device utilizing a TAP controller for very minimal external testing. Since ASET is a customized testing approach for each SoC device, it must be implemented at the RTL design level to allow for economical design synthesis and verification. Each SoC device needs a set of design rules which the designer must follow to assure compliance in implementing a successful ASET strategy.

Since a hierarchical test strategy is utilized, each block must be fully synchronous and B-SCAN and/or BIST compliant. These design constraints allows for easy coupling to the test controllers and device TAP. This generally means that the block logic must be composed of combinational logic and scannable D-type flip-flops. The memory blocks can be tested using BIST-compliant architectures.



The challenging aspect of ASET is the design effort required in integrating ASET techniques into the evolution of the SoC design. The ASET strategies must be developed concurrently with the high-level design effort. The design team must be continually aware of the potential testing problems. However, high-level design languages, simulators, and synthesis tools can be cost-effectively applied to minimize the ASET impact on scheduling. As in any custom design approach, the skill levels of the design team are most important in accomplishing the total design task in a timely manner.

ASET Advantages

Some of the benefits of ASET testing of SoC devices are:

1. At-speed testing invalidates any need for performance extrapolation.
2. Minimal ATE requirements.
3. Test coverage (controllability/observability) is improved since the design of each functional block is ASET-compliant.
4. Synchronous logic requirements simplify design and verification.
5. Testing is concurrently considered with device architecture, design, and software.

ASET Disadvantages

Unfortunately there are some disadvantages associated with ASET. They are:

1. A quasi custom design approach must be practiced integrating ASET into the SoC design methodolgy.
2. Similarly, SoC design cost/time increases slightly, but overall SoC device cost decreases.

This overview of ASET is an idea only at this time. We need a formal research project to concisely define the concept and apply it to some industrial-grade examples. We know testing costs and complexity derivatives are increasing. So a dramatic new testing approach is desperately needed. B-SCAN, BIST, and DFT concepts have existed for some time. But they have not had the dramatic cost/time impact that is needed. I think ASET can be formalized as a radically new testing strategy for SoC devices and embedded systems.

This ASET overview is authored by Bob Larsen.

PUBLICATIONS

The following were published by CECS faculty affiliates during the period of January 1, 2005 to March 31, 2005:

Focus	Title, Authors, Publication
Dynamic H/S Partitioning	*A Study of the Speedups and Competitiveness of FPGA Soft Processor Cores Using Dynamic Hardware/Software Partitioning*, Roman Lysecky, and Frank Vahid, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 18-23
Node Scheduling	*LORD: A Localized, Reactive and Distributed Protocol for Node Scheduling in Wireless Sensor Networks*, Arijit Ghosh and Tony Givargis, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 190-195
Functional Validation	*Functional Validation of System Level Static Scheduling*, Samar Abdi and Daniel D. Gajski, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 542-547
RTL Semantics	*Defining an Enhanced RTL Semantics*, Wenjing Rao, Shuqing Zhao and Daniel D. Gajski, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 548-553
Test Generation	*Functional Coverage Driven Test Generation for Validation of Pipelined Processors*, Prabhat Mishra and Nikil D. Dutt, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 678-683
Phantom Serialized Compiler	*Lightweight Multitasking Support for Embedded Systems Using the Phantom Serialized Compiler*, Andre C. Nacul and Tony Givargas, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 742-747
Modeling/Simulation Generation	*Generic Pipelined Processor Modeling and Cycle-Accurate Simulation Generation*, Mehrdad Reshadi and Nikil D. Dutt, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 786-791
Affine Functions	*FORAY-GEN: Automatic Generation of Affine Functions for Memory Optimizations*, Ilya Lssenin and Nikil D. Dutt, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 808-813
System Synthesis	*System Synthesis for Networks of Programmable Blocks*, Ryan Mannion, Harry Hsieh, Susan Cotterell and Frank Vahid, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 888-893
Instruction Set Extensions	*ISEGEN: Generation of High-Quality Instruction Set Extensions by Iterative Improvement*, Partha Biswas, Sudarshan Banerjee, Nikil Dutt, Laura Pozzi and Paolo Ienne, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 1246-1251
Compiler-in-the-Loop	*PBEXPLORE: A Framework for Compiler-in-the-Loop Exploration of Partial Bypassing in Embedded Processors*, Aviral Sheivastava, Nikil D. Dutt, Alex Nicolau and Eugene Earlie, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 1264-1270
Partitioning Software	*A Decomposition Approach to Partitioning Software for Microprocessor/FPGA Platforms Minimixzation* , Greg Stitt and Frank Vahid, Proceedings of the Design, Automation and Test in Europe Conference (DATE 05), Messe Munich, Germany, March 7-11 2005, pp 396-397
Encoding Scheme	*PBPAIR: Probability Based Power Aware Intra Refresh, A New Energy-Efficient Error-Resilient Encoding Scheme*, Minyoung Kim, Hyunok Oh, Nikil Dutt, Alex Nicolau and Nalini Venkatasubramanian, UCI CECS Technical Report 05-01, February 2005
HW-SW Partitioning	*HW-SW Partitioning for Architectures with Partial Dynamic Reconfiguration*, Sudarshan Banerjee, Elaheh Bozorgzadeh and Nikil Dutt, UCI CECS Technical Report 05-02, March 2005

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Communication Modeling	*System-Level Communication Modeling for Network-on-Chip Synthesis*, Andreas Gerstlauer, Dongwan Shin, Rainer Domer and Daniel D. Gajski, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 45-48
Functionality Formalism	*A Formalism for Functionality Preserving System Level Transformations*, Samar Abdi and Daniel D. Gajski, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 139-144
Discrete Probability Method	*Forward Discrete Probability Propagation Method for Device Performance Characterization Under Process Variations*, Rasit Onur Topaloglu and Alex Orailoglu, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 220-223
Fault Tolerant Architecture	*Fault Tolerant Nanoelectronic Processor Architectures*, Wenjing Rao, Alex Orailoglu and Ramesh Karri, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 311-316
Coverage Metric	*An Efficient Control-Oriented Coverage Metric*, Shireesh Verma, Kiran Ramineni and Ian G. Harris, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 317-322
Throughput-Driven Synthesis	*Automated Throughput-Driven Synthesis of Bus-Based Communication Architectures*, Sudeep Pasricha, Nikil D. Dutt and Mohamed Ben-Romdhane, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 495-498
Transformational Approach	*A Unified Transformational Approach for Reductions in Fault Vulnerability, Power, and Crosstalk Noise and Delay on Processor Busses*, Raid Ayoub and Alex Orailoglu, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 729-734
Power Management	*Dynamic Power Management Using On-Demand Paging for Networked Embedded Systems*, Yuvraj Agarwal, Curt Schurgers and Rajesh Gupta, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 755-759
Energy-Efficient Voltage	*A Generalized Technique for Energy-Efficient Operating Voltage Set-Up in Dynamic Voltage Scaled Processors*, Jaewon Seo and Nikil D. Dutt, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 836-841
Metric-Entity Characterization	*Multi-Metric and Multi-Entity Characterization of Applications for Early System Design Exploration,* Lukia Cai, Andreas Gerstlauer and Daniel D. Gajski, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 944-947
Clustering Technique	*A Clustering Technique to Optimize Hardware/Software Synchronization,* Junyu Peng, Samar Abdi and Daniel D. Gajski, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 965-968
Space-Data Tiling	*On Combining Iteration Space Tiling with Data Space Tiling for Scratch-Pad Memory Systems,* Chunhui Zhang and Fadi J. Kurdahi, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 973-976
QCA Design	*Fault Tolerant Quantum Cellular Array (QCA) Design Using Triple Modular Redundancy with Shifted Operands,* Tongquan Wei, Kaijie Wu, Ramesh Karri and Alex Orailoglu, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC 2005), Shanghai, China, January 18-21 2005, pp 1192-1195

CECS — promoting creativity and pursuing discovery!

Center for Embedded Computer Systems, University of California, Irvine

***CECS** Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Home Smart Home

I have been reading a lot lately about radio frequency identification (RFID) tags. RFID tags use a communication protocol based on the current Electronic Product Code (EPC) or bar codes and transmits to electronic readers. The present cost of RFID tags is a major impediment to wide-scale adoption.

These RFID tags are attached to every product in a store. This allows tracking the product from manufacturer to consumer. It's a fascinating means of minimizing inventories while gaining economies and shopper dynamics.

Shopping Frustrations

Two things I really hate to do; go to the Post Office and the grocery store. While I stand in line at the Post Office, they invariably close down one station which further delays being serviced. When I go to the grocery store, I waste a lot of time running up and down the aisles trying to find food products I desire. They too have the tendency to shut down checkout stations further increasing the checkout queues. Oh, how I hate to go shopping!

Here Comes RFID

Walmart have been pioneering RFID tagging of its merchandise as a means of monitoring its gigantic supply-chain inventory. Walmart has been dreaming of achieving tremendous efficiencies in its supply chain. Walmart is BIG: 5,139 stores with 1.3 million employees serving 138 million shoppers per week. Some even say Walmart should now be classified as a technology company because of its pioneering RFID efforts. Add Walmart to Intel and Microsoft as technology companies?

RFID Hope

Now if every food product you buy has an RFID tag, it seems like you would be able to compute its consumption rate within the home. When product A goes below a predetermined threshold, your home computer would automatically place an order for product A with the grocery store. Then the grocery store would deliver it to your home in a timely manner. Hurray! No more weekly visits to the grocery store. Sounds familiar; remember the demise of HomeGrocer.com about 3 years ago?

Until this RFID technology becomes reality, I will have to be happy with my *Home Sweet Home*. But I eagerly look forward to my *Home Smart Home* in the future. In the meantime, see you at the Post Office and the grocery store—I'm the shopper with the gloomy face!

Bob Larsen