CECS eNEWS

Center for Embedded Computer Systems, University of California, Irvine

Highlights:

- CECS at ASP-DAC
- CECS Goes to DATE
- Arvind Distinguished Lecture
- Bergamaschi Distinguished Lecture
- Haigh-Wilkerson Industrial Speakers
- Gupta Elected IEEE Fellow
- Best Paper Award
- Publications

CECS at ASP-DAC

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9 Papers Presented!

Research affiliates and graduate students from the Center for Embedded Computer Systems (CECS) at the University of California, Irvine played a significant role in the success of the Asia and South Pacific Design Automation Conference (ASP-DAC) held at the Pacifico Yokohama Conference Center, Yokohama, Japan from January 27-30, 2004.

Professor Nikil Dutt served as Co-

Chair of the Technical Program Committee that evaluated 291 submitted technical papers and accepted 147 for presentation at the conference. Professors Pai Chou and Alex Orailoglu served as members of the Technical Program Committee.

The following technical papers were presented with the cited pages from the conference proceedings:

- *High-Frequency Noise in RF Active CMOS Mixers*, Payam Heydari, pp 57—61

- *On Mismatch in the Deep Sub-Micron Era—From Physics to Circuits*, Rasit Onur Topaloglu and Alex Orailoglu, pp 62—67

- *Efficient RT-Level Fault Diagnosis Methodology*, Ozgur Sinanoglu and Alex Orailoglu, pp 212—217 *** This paper was nominated as a Best Paper Candidate!

- *On Deriving Equivalent Architecture Model from System Specification*, Samar Abdi and Daniel Gajski, pp 322—327

- *Embedded Software Generation from System-Level Design Languages*, Haobo Yu, Rainer Doemer and Daniel Gajski, pp 463—468

- *Energy Efficient Code Generation Exploiting Reduced Bit-Width Instruction Set Architectures (rISA)*, Aviral Shrivastava and Nikil Dutt, pp 475—477

- *Fast and Efficient Voltage Scheduling by Evolutionary Slack Distribution,* Bita Gorji-Ara, Pai Chou, Nader Bagherzadeh, Mehrdad Reshadi and David Jensen, pp 659—662

- *Automatic Generation of Bus Functional Models from Transaction Level Models,* Dongwan Shin, Samar Abdi and Daniel Gajski, pp 756—758

- *A Novel Memory Size Model for Variable-Mapping in System Level Design,* Lukai Cai, Haobo Yu and Daniel Gajski, pp 813—818

Professor Pai Chou served as Co-Chair of a session titled *Behavioral Synthesis* and a ware. Graduate Student Samar Abdi served as Co-Chair of a session titled *Design Verification and Simulation*. Professor Alex Orailoglu served as Co-Chair of a session titled *System-Level Architecture*. Professor Daniel Gajski was the organizer and speaker at a one day tutorial titled *System-Level Design Methodology for SoC Design*.

Yokohama Landmark Tower—Minato Mirai 21

These mentioned research affiliates and their graduate students made substantial contributions to the technical program and organization of this year's Asia and South Pacific Design Automation Conference (ASP-DAC). CECS is expecting to continue its significant technical and organizational influence of next year's conference.

Waterfront View of Yokohama

CECS goes to DATE '04

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CECS maintains European influence!

From February 16—20, 2004, several CECS professors and graduate students attended the Design, Automation and Test in Europe Conference (DATE '04) held at the CNIT La Defense, Paris, France.

The following technical presentations were made and can be found in the conference proceedings:

- *Loop Shifting and Compaction for the High-Level Synthesis of Designs with Complex Control Flow*, Sumit Gupta, Nikil Dutt, Alexandru Nicolau, and Rajesh Gupta, pp 114-119

- *A Self-Tuning Cache Architecture for Embedded Systems*, Chuanjun Zhang, Frank Vahid, and Roman Lysecky, pp 142-147

- *Graph-Based Functional Test Program Generation for Pipelined Processors*, Prabhat Mishra and Nikil Dutt, pp 182-187

- *Automatic Tuning of Two-Level Caches to Embedded Applications*, Ann Gordon-Ross, Frank Vahid, and Nikil Dutt, pp 208-213

- *Low Static-Power Frequent-Value Data Caches*, Chuanjun Zhang, Jun Yang, and Frank Vahid, pp 214-219

- *Using a Victim Buffer in an Application-Specific Memory Hierarchy*, Chuanjun Zhang and Frank Vahid, pp 220-225

- *Scan Power Minimization Through Stimulus and Response Transformations*, Ozgur Sinanoglu and Alex Orailoglu, pp 404-409

- *Network Topology Exploration of Mesh-Based Coarse-Grain Reconfigurable Architectures*, Nikhil Bansal, Sumit Gupta, Nikil Dutt, Alex Nicolau, and Rajesh Gupta, pp 474-479

- *A Configurable Logic Architecture for Dynamic Hardware/Software Partitioning*, Roman Lysecky and Frank Vahid, pp 480-485

- *Circular-Scan: A Scan Architecture for Test Cost Reduction*, Baris Arslan and Alex Orailoglu, pp 1290-1295

The following interactive presentations were made:

- *Energy-Efficient Design for Highly Associative Instruction Caches in Next-Generation Embedded Processors*, Juan Luis Aragon, Dan Nicolaescu, Alex Veidenbaum, and Ana-Maria Badulescu, pp 1374-1375

- *Dynamic Voltage and Cache Reconfiguration for Low Power*, Andre Nacul and Tony Givargas, pp 1376-1377

Professor Rajesh Gupta served as Technical Program Chair for HW/SW CoDesign and Professors Nikil Dutt, Payam Heydari, Alex Orailoglu, and Frank Vahid sereved as members of the Technical Program Committee.

As you can see, these CECS authors enjoyed a hot DATE in Paris! Congratulations to these authors on keeping the CECS image visible within the European technical community.

Professor Gupta Elected IEEE Fellow

The Institute of Electrical and Electronics Engineers (IEEE) Board of Directors announced that Rajesh K. Gupta, Professor and Qualcomm Endowed Chair, Department of Computer Science and Engineering, University of California, San Diego was elected a Fellow *for contributions to high-level synthesis and computer-aided design of digital circuits and systems* in January 2004.

Professor Gupta's current research interests are: embedded system specification, modeling, and synthesis, system-level

Veidenbaum Edits IEEE Monograph

Professor Alex Veidenbaum served as Chairman of the 2003 International Workshop on Innovative Architecture for Future Generation High-Performance Processors and System (IWIA'03) held at the Sheraton Hotel, Kauai, HI on January 27-29, 2003. Professor Alex Orailoglu served on the Program Committee. The Center for Embedded Computer Systems (CECS) was the primary sponsor of the 2003 International Workshop on Innovative Architecture for Future Generation High-Performance Processors and Systems (IWIA'03).

A total of 24 researchers from the United States and Japan, representing academia and industry, presented their current research and discussed future technology directions.

Professor Veidenbaum coedited an IEEE Computer Society Monograph with Kazuki Joe, Nara Women's University, Japan, titled *Innovative Architecture for Future Generation High-Performance Processors and Systems* which is a collection of twelve reviewed papers resulting from workshop presentations. One paper included in the monograph is *Dynamically Adaptive Fetch Size Prediction for Data Caches*, Weiyu Tang, Alex Veidenbaum, and Alex Nicolau, pp 40-44.

Professor Veidenbaum also attended IWIA'04 which was held at the Maui Prince Hotel, Maui, HI from January 12-13, 2004.

Gupta continued

power management, algorithms for VLSI design automation, and design abstractions.

Professor Gupta serves as the Editor-in-Chief of IEEE Design and Test of Computers, Associate Editor of IEEE Transactions on Computer Aided Design (TCAD), and Associate Editor of IEEE Transactions on Mobile Computing (TMC).

The designation of Fellow is awarded to no more then 0.1 percent of the voting membership of the IEEE each year for noteworthy contributions to the advancement of engineering, science, or technology. Congratulations Professor Gupta on being awarded this distinguished designation and honor.

Dr. Bergamaschi Delivers Distinguished Lecture

* * *

Argues radical new approaches needed!

On January 16, 2004, Dr. Reinaldo Bergamaschi, T. J. Watson Research Center, IBM, Yorktown Heights, NY, delivered a CECS Distinguished Lecture titled *System-Level Design: Only the Radical Will Survive,* to a near capacity audience at the UCI McDonnell Douglas Auditorium.

Dr. Bergamaschi predicts: at 90 nm architectural effort will dominate physical layout!

Dr. Bergamaschi stated that the term "system-level design" has been defined, used and abused countless times by designers, CAD developers and most of all, tools sales people. By now we all know what is supposed to be, and it 'ain't pretty' despite claims made by CAD vendors. He argued that for the past five years we have tried to develop system-level tools by fattening the already beaten up ASIC design methodology, by exaggerating the advantages of high-level languages, by over blowing the benefits of software-related methodologies for designing hardware, among other very incremental approaches. The design methodologies and tools currently used for system-on-chip design are an evolution of ASIC and board-level design tools. Such an incremental approach has been ineffective in closing the productivity gap. He further analyzed the current push to use high-level languages and software approaches for hardware design, and tried to

Bergamaschi continued

convince the audience that such attempts, while in the right direction, are far from sufficient. He argued that radical new approaches for system design are needed if we want to be able to design new products in shorter time-to-market.

Dr. Reinaldo Bergamaschi graduated in Electronics Engineering from the Aeronautics Institute of Technology, Sao Jose dos Campos, Brazil, in 1982, and in 1984 he received the MEE degree from the Philips International Institute, Eindhoven, The Netherlands. In 1989 he obtained the PhD degree in Electronics and Computer Science from the University of Southampton, Southampton, England and joined the T. J. Watson Research Center, IBM, Yorktown Heights, NY. He has worked extensively on RTL, behavioral and system-level design tools and methodologies. He was the main architect of IBM's high-level synthesis system and is currently developing system-level modeling and synthesis tools for core-based, platform-based designs. He has participated in numerous conference committees and given several tutorials and lectures on high-level and system-level design issues and tools.

Professor Daniel Gajski, CECS Director, hosted Dr. Bergamaschi during his visit to CECS.

CECS Web Site Redesigned

CECS is premiering a totally redesigned web site: *www.cecs.uci.edu* . The redesigned web site features user friendly site navigation, pictorial pages, frequent event updates, and simplified selection options.

Some of the improved features are:

- Simplified page navigation

- More pictures in CECS settings to enhance viewing of pages

- Pictorial research projects overview

- News and coming events highlighted on home page

- Acknowledgement of our sponsors

- Publications archive; ie., *eNEWS* and CECS Technical Reports accessible for downloading

Our web site redesign and development has been managed and executed by Quoc-Viet Dang, a UCI senior majoring in Computer Science who expects to graduate in June 2004. Thanks Quoc-Viet for all your creative efforts.

Hope you all enjoy visiting our redesigned web site and keeping up to date with our research programs and informative events.


Which one is the UCI mascot?

Professor Arvind Delivers Distinguished Lecture

*   *   *

High-level synthesis is ready for exploitation!

Professor Arvind, Johnson Professor of Computer Science and Engineering at the Massachusetts Institute of Technology, Cambridge, MA delivered a CECS Distinguished Lecture titled *Why Chip Design Can't be Left to EE's* at the UCI McDonnell Douglas Auditorium on March 22, 2004. Professor Daniel Gajski hosted Professor Arvind during his visitation to CECS.
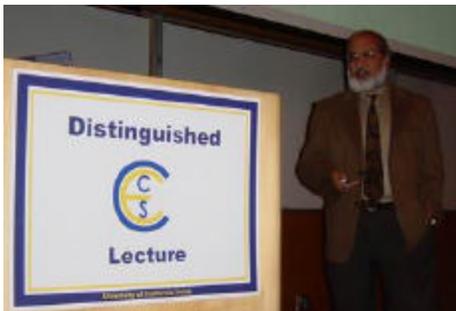
Professor Arvind discusses problems of the small and problems of the large.

Professor Arvind stated that hundred million gate ASIC's are possible by the end of the decade. However, numerous problems related to processing technology and design methodology need to be solved before such large chips will become commonplace. These are: *problems of the small*—electrical engineering in IC design and *problems of the large*—computer science in IC design. The paramount challenge is closing the semantics gap existing between conventional software languages and hardware. Computer scientists are much better equipped to solve these new challenging problems related to the design-in-the-large.

Bluespec is a language/methodology that promotes correctness-by-construction. Its underlying execution model is based on atomic actions on state elements such as flip-flops, registers, ...; i.e., any legal behavior is explainable in terms of a sequence of atomic actions on the state. Expressiveness of Bluespec is achieved by keeping its static semantics orthogonal to its hardware execution semantics. The source program

is turned into a flat interconnection of modules by "static elaboration" during the compilation phase.

Professor Arvind's current research at MIT is focused on high-level specification, modeling, synthesis and verification of architectures and protocols using Term Rewriting Systems (TRSs) which laid the foundations for two companies he founded: Sandburst Corp., Andover, MA and more recently Bluespec, Inc., Waltham, MA. Previously, he contributed to the development of dynamic dataflow architectures and together with Dr. R. S. Nikhil published the book *Implicit Parallel Programming in pH*. Professor Arvind is an IEEE Fellow and was awarded the Charles Babbage Outstanding Scientist Award in 1994. He has received Distinguished Alumni Awards from the Indian Institute of Technology, Kanpur, and the University of Minnesota.

Greatness is not where we stand, but in what directions we are moving, we must sail with the wind and sometimes against it, but sail we must, not drift, nor lie in anchor.

Oliver Wendell Homes

Haigh & Wilkerson Industrial Speakers

Jonathan R. Haigh and Michael W. Wilkerson, engineers with Intel Corporation, Pheonix, AZ delivered a presentation titled *Embedded Microprocessor Cache and Translation Lookaside Buffer (TLB) Low Power Circuit Techniques for 90nm and Beyond* on February 6, 2004 at the McDonnell Douglas Auditorium. They stated that optimizing power consumption is a primary goal in the design of embedded processors even as the push for higher performance continues unabated. Managing the microprocessor's power dissipation while still striving to push the design into GHz speeds provides a significant technology challenge. As designs move to 90nm and beyond, device scaling has reduced oxide thickness and V_T to the point where standby leakage power is on the same magnitude as active power. Today's successful designs need to

Best Paper Award

Professor Nikil Dutt and graduate students Mehrdad Reshadi, Prabhat Mishra, and Nikhil Bansal, pictured below, left to right, proudly display their Best Paper Awards received at the First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS 2003) held at the Marriott Hotel and Tennis Club, Newport Beach, CA on October 1-3, 2003.

Their award winning technical paper was titled *An Efficient Retargetable Framework for Instruction-Set Simulation*. They also received a $1,000 award in addition to their plaques. CECS extends congratulations to these outstanding researchers on receiving this prestigious technical paper award!

Man is still the most extraordinary computer of all.

John F. Kennedy

Haigh & Wilkerson continued

aggressively manage both active and standby currents.

Jonathan R. Haigh received a BSEE from the University of Cincinnati in 1996. He joined Intel Corporation in 2000 and was previously employed by General Electric Company and Digital Semiconductor.

Michael W. Wilkerson received the BSEE in 1991 and the MSEE in 1997 from the University of Florida. He Joined Intel Corporation in 1998 and served in the U. S. Navy from 1983 to 1996.

Professor Alex Veidenbaum served as their host during their visit to CECS.

The following were published by CECS faculty affiliates during the period of January 1, 2004 to March 31, 2004:

Focus	Title, Authors, Publication
Test of Digital Components	*Seamless Test of Digital Components in Mixed-Signal Paths*, Sule Ozev, Ismet Bayraktaroglu, and Alex Orailoglu, IEEE Design & Test of Computers, January-February 2004, pp 44—55
Fetch Size Prediction	*Adaptive Fetch Size Prediction for Data Caches*, Weiyu Tang, Alex Veidenbaum, and Alex Nicolau, Innovative Architecture for Future Generation High-Performance Processors and Systems Techniques, IEEE Computer Society, pp 40—44
HF Noise	*High-Frequency Noise in RF Active CMOS Mixers*, Payam Heydari, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), January 27-30, 2004, pp 57—61
Mismatch	*On Mismatch in the Deep Sub-Micron Era—From Physics to Circuits*, Rasit Onur Topaloglu and Alex Orailoglu, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), January 27-30, 2004, pp 62—67
Fault Diagnosis	*Efficient RT-Level Fault Diagnosis Methodology*, Ozgur Sinanoglu and Alex Orailoglu, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), January 27-30, 2004, pp 212—217
Architecture Model	*On Deriving Equivalent Architecture Model from System Specification*, Samar Abdi and Daniel Gajski, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), January 27-30, 2004, pp 322—327
Software Generation	*Embedded Software Generation from System-Level Design Languages*, Haobo Yu, Rainer Doemer and Daniel Gajski, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), January 27-30, 2004, pp 463—468
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Voltage Scheduling	*Fast and Efficient Voltage Scheduling by Evolutionary Slack Distribution,* Bita Gorji-Ara, Pai Chou, Nader Bagherzadeh, Mehrdad Reshadi and David Jensen, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), January 27-30, 2004, pp 659—662
Bus Models	*Automatic Generation of Bus Functional Models from Transaction Level Models,* Dongwan Shin, Samar Abdi and Daniel Gajski, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), January 27-30, 2004, pp 756—758
Memory Size Model	*A Novel Memory Size Model for Variable-Mapping in System Level Design,* Lukai Cai, Haobo Yu and Daniel Gajski, Proceedings of the Asia and South Pacific Design Automation Conference (ASP-DAC), January 27-30, 2004, pp 813—818
Loop Shifting/Compaction	*Loop Shifting and Compaction for the High-Level Synthesis of Designs with Complex Control Flow*, Sumit Gupta, Nikil Dutt, Alex Nicolau, and Rajesh Gupta, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 114-120
Self-Tuning Cache	*A Self-Tuning Cache Architecture for Embedded Systems*, C. Zhang, Frank Vahid, and Roman Lysecky, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 142-147
Test Program Generation	*Graph-Based Functional Test Program Generation for Pipelined Processors*, Prabhat Mishra and Nikil Dutt, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 182-187
Two-Level Caches	*Automatic Tuning of Two-Level Caches to Embedded Applications*, A. Gordon-Ross, Frank Vahid, and Nikil Dutt, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 208-213

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Data Caches	*Low Static-Power Frequent-Value Data Caches*, C. Zhang, J. Yang, and Frank Vahid, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 214-219
Victim Buffer	*Using a Victim Buffer in an Application-Specific Memory Hierarchy*, C. Zhang and Frank Vahid, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp
Scan Power Minimization	*Scan Power Minimization Through Stimulus and Response Transformations*, Onur Sinanoglu and Alex Orailoglu, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 404-409
Network Topology Exploration	*Network Topology Exploration of Mesh-Based Coarse-Grain Reconfigurable Architectures*, Nikhil Bansal, Sumit Gupta, Nikil Dutt, Alex Nicolau, and Rajesh Gupta, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 474-479
Configurable Architecture	*A Configurable Logic Architecture for Dynamic Hardware/Software Partitioning*, Roman Lysecky and Frank Vahid, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 480-485
Circular Scan	*Circular-Scan: A Scan Architecture for Test Cost Reduction*, B. Arslan and Alex Orailoglu, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 1290-1295
Associative Caches	*Energy-Efficient Design for Highly Associative Instruction Caches in Next-Generation Embedded Processors*, J. Aragon, D. Nicolaescu, Alex Veidenbaum, and A. Badulescu, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 1374-1375
Cache Reconfiguration	*Dynamic Voltage and Cache Reconfiguration for Low Power*, A. Nacul and Anthony Givargas, Proceedings of the Design, Automation and Test in Europe Conference (DATE '04), February 16-20, 2004, pp 1376-1378
Non-preemptive Scheduling	*Energy Aware Non-preemptive Scheduling for Hard Real-Time Systems*, Ravindra Jejurikar and Rajesh Gupta, UCI CECS Technical Report 04-01, January 2004
Threshold Scheduling	*Integrating Processor Slowdown and Preemption Threshold Scheduling for Energy Efficiency in Real Time Embedded Systems*, Ravindra Jejurikar and Rajesh Gupta, UCI CECS Technical Report 04-03, February 2004
Retargetable Profiling	*Retargetable Profiling for Rapid, Early System-Level Design Space Exploration*, Lukai Cai, UCI CECS Technical Report 04-04, February 2004
Design Space Exploration	*High Level Design Space Exploration of Shared Bus Communication Architectures*, Sudeep Pasricha, Mohamed Ben-Romdhane and Nikil Dutt, UCI CECS Technical Report 04-06, March 2004
No Instruction Set Computer (NISC)	*NISC Modeling and Simulation*, Mehrdad Reshadi and Daniel Gajski, UCI CECS Technical Report 04-08 March 2004

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CECS—*Solving Tomorrow's Problems!*

Center for Embedded Computer Systems, University of California, Irvine

CECS *Mission Statement:*

To conduct leading-edge interdisciplinary research in embedded systems, emphasizing automotive, communications, and medical applications, and to promote technology and knowledge transfer for the benefit of the individual and society.

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Got CECS?

Is The Worst Over
With the economic climate improving in 2004, CECS is hoping the level of industrial support for its core and domain research programs will increase substantially. As you know, the last three years have been extremely taxing in raising industrial funding to support our research. We sustained our research programs primarily through government grants and contracts. But now we are expanding our horizon and targeting industrial support.

Collaborative Research
Our research model is founded on collaborative research. We need to develop partnerships that provide us with leading-edge technology drivers that can only be generated by industry. Our graduate students need to be challenged with more than text book examples. They need to experience defining "tough" problems and developing innovative solutions.

We are seeking collaborative research projects that result in win-win partnerships with meaningful bilateral technology transfer!

Student Interns
As part of our graduate student education program, we are seeking industrial companies that are interested in giving our students the opportunity to experience the challenges associated with industrial design problems during the 2004 summer months. If you are desirous of affording an opportunity to our students, please feel free to contact any professor or staff member and we will assist in working out the details.

Industrial Support Appeal
Industry is being confronted for support of many worthy charitable organizations. CECS is striving to be different by developing a paradigm of collaborative research based on a win-win partnership. This can only be realized with the help of industry. If you are an

engineer, manager, or executive with an industrial organization, we appeal for your financial support. Won't you become proactive in being our advocate in funding appropriate research projects that will benefit your company. I assure you the rewards will be long lasting. Please contact us anytime and I guarantee we will be delighted to respond with an outstanding proposal.

Got CECS? I certainly hope so!

Bob Larsen